

PS5268

DATA SHEET

1/2.7" Full-HD 1080p HDR CMOS IMAGE SENSOR

Aug. 2019

Version 1.0

PS5268 Full-HD 1080p HDR CMOS IMAGE SENSOR

General Description

The **PS5268** is a low power, highly integrated CMOS image sensor that output of **1920x1080 (Full HD-1080p)** pixels with rolling shutter readout. It embedded the new FinePixel™ and HDR sensor technology to perform the excellent image quality and single-shot high dynamic range synthesized image output. **PS5268** outputs linear 14-bit or local tone mapped 12-bit raw data through MIPI CSI-2 interface with very low power consumption. It is available in **CSP** package.

The **PS5268** can be programmed to set the exposure time for different luminance condition via I2C™ serial control bus. Embedded HDR image synthesis with local tone mapping to deliver high performance, cost effective and time to market for high resolution HDR application. By programming the internal register set, it performs on-chip black level correction and high temperature image quality control.

Features

- **Image size : 1928 x 1088 pixels with Bayer-RGB color filter array and micro-lens**
- **Output format:**
 - **14bit Linear HDR-RAW RGB**
 - **12bit HDR + Local Tone Mapped**
- **RAW RGB**
 - **10bit Linear RAW RGB**
- **Output interface**
 - **12bit parallel DVP output**
 - **2-lane MIPI output (up to 800Mbps per lane)**
- **I2C™ Interface with two kinds of Slave_ID**
- **Low Power consumption**
- **High sensitivity**
- **Support on-chip HDR synthesis**
- **Image sensor processor functions :**
 - **Automatic black-level calibration**
 - **Embedded Local Tone Mapping**
 - **Black sun cancellation**
- **Support sensor frame synchronization**
- **On-chip PLL (input_clock / PLL_m >= 1MHz)**
- **On-chip column A/D converter**
- **On-chip manual analog gain control**
- **Continuous variable frame time & exposure time**
- **Support WOI and subsampling**
- **Support dummy line & pixel timing**
- **Support output Hsync at Vsync**
- **Support 1.7V~3.3V I/O**
- **Support Fast Auto Exposure (FAE) function**

Specifications

Parameter	Typical Value
Active array size	1928(H) x 1088(V)
Pixel size	3.0um (H) x 3.0um (V)
Shutter type	Electronic rolling shutter (ERS)
Optical format	1/2.7-inch
Lens chief ray angle	17 degree
ADC	10-bit
Sensitivity	5800 mV/Lux-sec
SNRmax	41 dB
Dynamic range	85 dB
Scan mode	Progressive scan
Input clock	Max 50MHz
Pixel clock	Max 148.5MHz
Max. frame rate	1080p: 1920x1080 Linear@ 60fps 1080p: 1920x1080 HDR+LTM @30fps
Supply voltage	Analog: 3.3 V Digital: 1.2 V I/O: 1.8V / 3.3V
Power consumption	75mW@1080p30 (MIPI) 54.5mW@1080p30 (DVP w/o I/O) 124mW@HDR-LTM1080p30 (MIPI) 107mW@HDR-LTM 1080p30 (DVP w/o I/O)
Operating temperature	-30°C ~ 85°C

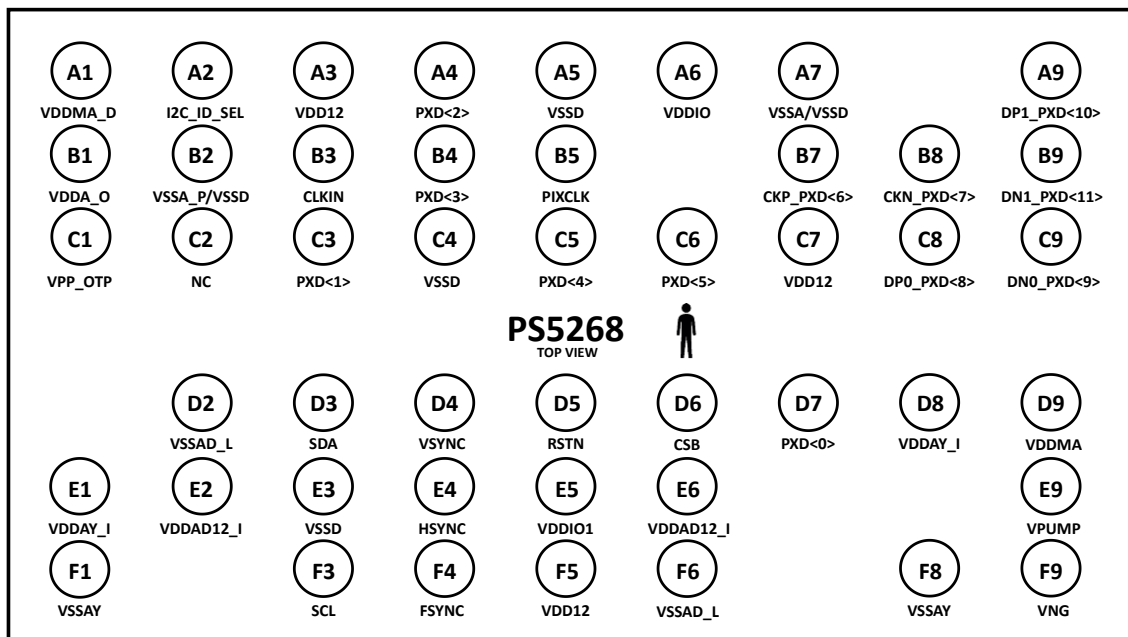
Applications

- **Surveillance HD-CCTV Camera**
- **Surveillance IP Camera**
- **Car Video Recorder**
- **Video Door Phone**

Ordering Information

Part Number	Description
PS5268LT	47-ball CSP

1. Pin Assignment



Pin No.	Name	Type	Description
A1	VDDMA_D	Power	Analog power : 3.3V
A2	I2C_ID_SEL	Input	I2C address selection High: Slave_ID = 0x98 Low: Slave_ID = 0x90 (Default)
A3	VDD12	Power	Digital power : 1.2V
A4	PXD<2>	Output	Pixel data output
A5	VSSD	GND	GND
A6	VDDIO	Power	I/O power : 1.8V ~ 3.3V
A7	VSSD/VSSA	GND	GND
A9	DP1 PXD<10>	Output	Pixel data output ; MIPI digital data output_1 positive terminal
B1	VDDA_O	Power	VDDA LDO output voltage(2.7-3.0V)
B2	VSSD/VSSA_P	GND	GND
B3	CLKIN	Input	Master clock input
B4	PXD<3>	Output	Pixel data output
B5	PIXCLK	Output	Pixel clock output
B7	CKP PXD<6>	Output	Pixel data output ; MIPI output clock positive terminal
B8	CKN PXD<7>	Output	Pixel data output ; MIPI output clock negative terminal
B9	DN1 PXD<11>	Output	Pixel data output ; MIPI digital data output_1 negative terminal
C1	VPP_OTP	Power	External voltage for OTP device
C2	NC	--	Reserved

C3	PXD<1>	Output	Pixel data output
C4	VSSD	GND	GND
C5	PXD<4>	Output	Pixel data output
C6	PXD<5>	Output	Pixel data output
C7	VDD12	Power	Digital power : 1.2V
C8	DP0 PXD<8>	Output	Pixel data output ; MIPI digital data output_0 positive terminal
C9	DN0 PXD<9>	Output	Pixel data output ; MIPI digital data output_0 negative terminal
D2	VSSAD_L	GND	GND
D3	SDA	I/O	I2C data, open drain type
D4	VSYNC	Output	Asserted when frame data is valid
D5	RSTN	Input	Reset signal, active low, internal pull high , The RSTN should meet the power sequence requirements.
D6	CSB	Input	Suspend control, "1" : suspend, "0" : normal function
D7	PXD<0>	Output	Pixel data output
D8	VDDAY_I	Power	Sensor power input
D9	VDDMA	Power	Analog power : 3.3V
E1	VDDAY_I	Power	Sensor power input
E2	VDDAD12_I	Power	Analog power input voltage(1.2V)
E3	VSSD	GND	GND
E4	HSYNC	Output	Asserted when line data is valid
E5	VDDIO	Power	I/O power : 1.8V ~ 3.3V
E6	VDDAD12_I	Power	Analog power input voltage(1.2V)
E9	VPUMP	Power	Positive pump output voltage
F1	VSSAY	GND	GND
F3	SCL	I/O	I2C clock, open drain type
F4	FSYNC	Input	Frame sync signal
F5	VDD12	Power	Digital power : 1.2V
F6	VSSAD_L	GND	GND
F8	VSSAY	GND	GND
F9	VNG	Power	Reference voltage

2. Specifications

Absolute Maximum Ratings					
Operating Temperature (sensor junction temperature)			-30°C ~ 85°C		
Ambient Storage Temperature			-40°C ~ 125°C		
Supply Voltage (with respect to ground)	V _{DDA}	4.5V			
	V _{DDD}	3.0V			
	V _{DDIO}	4.5V			
All Input / Output Voltage (with respect to ground)			-0.3V to V _{DDIO} + 0.5V		
Lead-free temperature, Surface-mount process			245°C		
ESD rating, Human Body model			2000V		
DC Electrical Characteristics (Ta = -30°C ~ 85°C)					
Symbol	Parameter	Min.	Typ.	Max.	Unit
Type : POWER					
V _{DDA}	DC supply voltage – Analog	3.14	3.3	3.47	V
V _{DDD}	DC supply voltage – Digital core	1.14	1.2	1.26	V
V _{DDIO}	DC supply voltage – I/O	1.71	1.8	3.47	V
I _{DDA}	Operating Current – Analog (DVP)		12.1		mA
	Operating Current – Analog (MIPI)		12.5		mA
I _{DDD}	Operating Current – Digital (DVP)		51.5		mA
	Operating Current – Digital (MIPI)		61.7		mA
I _{DDIO}	Operating Current – IO 1.8V (DVP)		8.5		mA
Type : IN & I/O					
V _{IH}	Input Voltage HIGH	V _{DDIO} * 0.7			V
V _{IL}	Input Voltage LOW			V _{DDIO} * 0.3	V
Type : OUT & I/O					
V _{OH}	Output Voltage HIGH	V _{DDIO} * 0.9			V
V _{OL}	Output Voltage LOW			V _{DDIO} * 0.1	V
AC Operating Condition					
Symbol	Parameter	Min.	Typ.	Max.	Unit
f _{sysclk}	System clock frequency		27	50	MHz
t _{sysclk_dc}	System clock duty cycle	45		55	%
Sensor Characteristics					
Parameter		Typ.		Unit	
Sensitivity		5800		mV/Lux-Sec	
Maximum Signal to Noise Ratio		41		dB	
Dynamic Range		85		dB	

†: Sensor function works in the ambient operating temperature range. However, the image quality may change at high temperature condition.

†: The power consumption is measured with 4X analog gain in HDR + LTM 1080p 30fps.

3. I²C™ Bus

PS5268 supports I²C bus transfer protocol and acts as slave device. The 7-bits unique slave address can be “1001000” or “1001100”, choose by I2C_ID_SEL pin, and supports receiving / transmitting speed as maximum 400 kHz.

I²C Bus Overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pulled high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition : A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Figure 3.1.
- Valid data : The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure 3.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge : The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

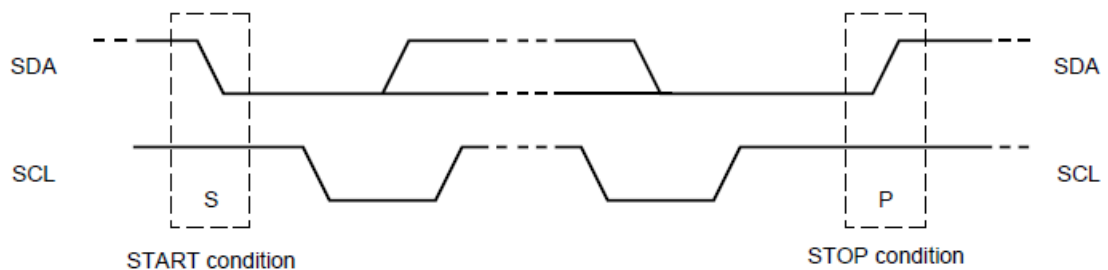


Fig.3.1 Start and Stop Condition

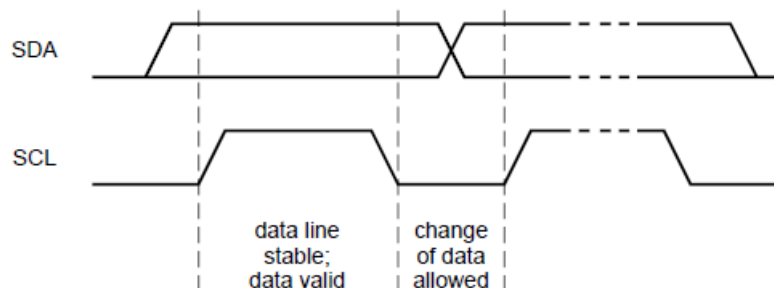


Fig.3.2 Valid Data

Data Transfer Format

Master transmits data to slave (write cycle)

- S : Start.
- A : Acknowledge by slave.
- P : Stop.
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle.
RW = 1 – Read cycle, RW = 0 – Write cycle.
- SUBADDRESS : The address values of **PS5268** internal control registers. (Please refer to **PS5268** register description)

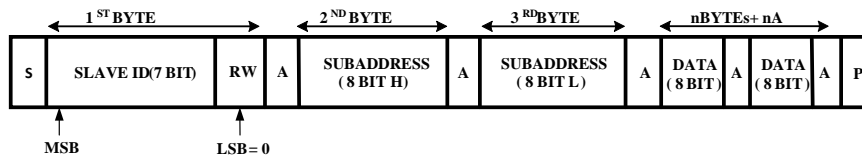


Fig.3.3 Master-transmitter transmits to slave-receiver for multi-write command

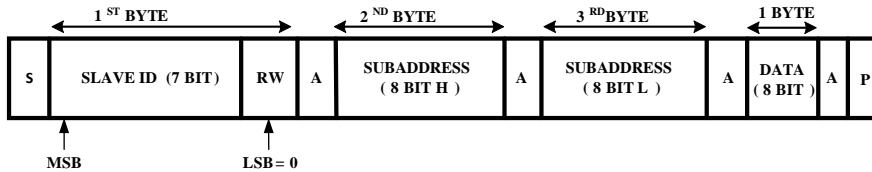


Fig.3.4 Master-transmitter transmits to slave-receiver for single-write command

During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After slave (**PS5268**) issues acknowledgment, the master places 2nd byte & 3rd byte (Sub Address) data on SDA line. Again follow the **PS5268** acknowledgment, the master places the 8 bits data on SDA line and transmit to **PS5268** control register (address was assigned by 2nd byte & 3rd byte). After **PS5268** issues acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi byte write, the **PS5268** Sub Address is automatically increment after each DATA byte transferred. The data and A cycles is repeat until last byte write. Every control registers value inside **PS5268** can be programming via this way.

Slave transmits data to master (read cycle)

- The sub-address was taken from previous write cycle.
- The sub-address is automatically increment after each byte read.
- Am : Acknowledge by master.
- Note there is no acknowledgment from master after last byte read.

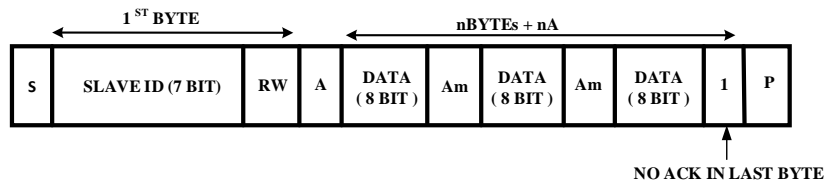


Fig.3.5 Slave-transmitter transmits to master-receiver for multi-read command

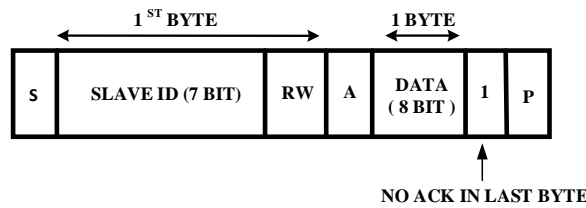


Fig.3.6 Slave-transmitter transmits to master-receiver for single-read command

During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by **PS5268**. The 8 bits data was read from **PS5268** internal control register that address was assigned by previous write cycle. control register that address was assigned by previous write cycle. Follow the master acknowledgment, the **PS5268** place the next 8 bits data (address is increment automatically) on SDA line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (**PS5268**) must releases SDA line to master to generate STOP condition.

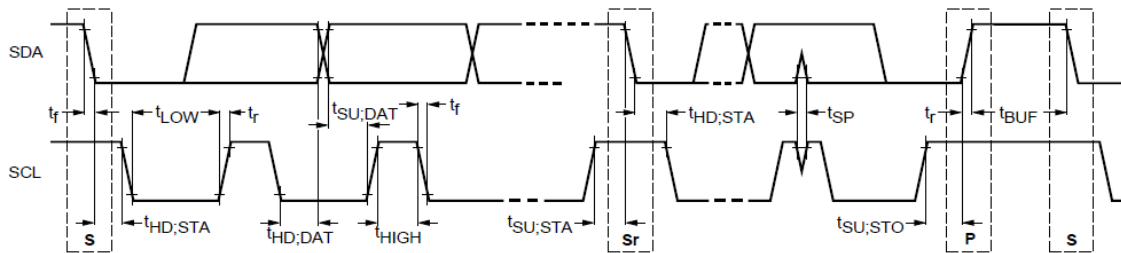
I²C™ Bus Timing


Fig.3.5 Definition of timing for F/S mode devices on the I2C-bus

I²C™ Bus Timing Specification						
Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency.	f_{scl}	10	100	0	400	KHz
Hold time (repeated) Start condition. After this period, the first clock pulse is generated.	$t_{HD;STA}$	4.0	-	0.6	-	μ s
Low period of the SCL clock.	t_{LOW}	4.7	-	1.3	-	μ s
High period of the SCL clock.	t_{HIGH}	4.0	-	0.6	-	μ s
Set-up time for a repeated START condition.	$t_{SU;STA}$	4.7	-	0.6	-	μ s
Data hold time. For I2C-bus device.	$t_{HD;DAT}$	5.0	3.45	0	0.9	μ s
Data set-up time.	$t_{SU;DAT}$	250	-	100	-	ns
Rise time of both SDA and SCL signals.	t_r	-	1000	-	300	ns (note 1)
Fall time of both SDA and SCL signals.	t_f	-	300	-	300	ns (note 1)
Set-up time for STOP condition.	$t_{SU;STO}$	4.0	-	0.6	-	μ s
Bus free time between a STOP and START.	t_{BUF}	4.7	-	1.3	-	μ s
Capacitive load for each bus line.	C_b	-	400	-	400	pF
Noise margin at LOW level for each connected device. (Including hysteresis)	V_{nL}	0.1 VDD	-	-	0.1 VDD	V
Noise margin at HIGH level for each connected device. (including hysteresis)	V_{nH}	0.2 VDD	-	-	0.2 VDD	V

Note: It depends on the “high” period time of SCL.

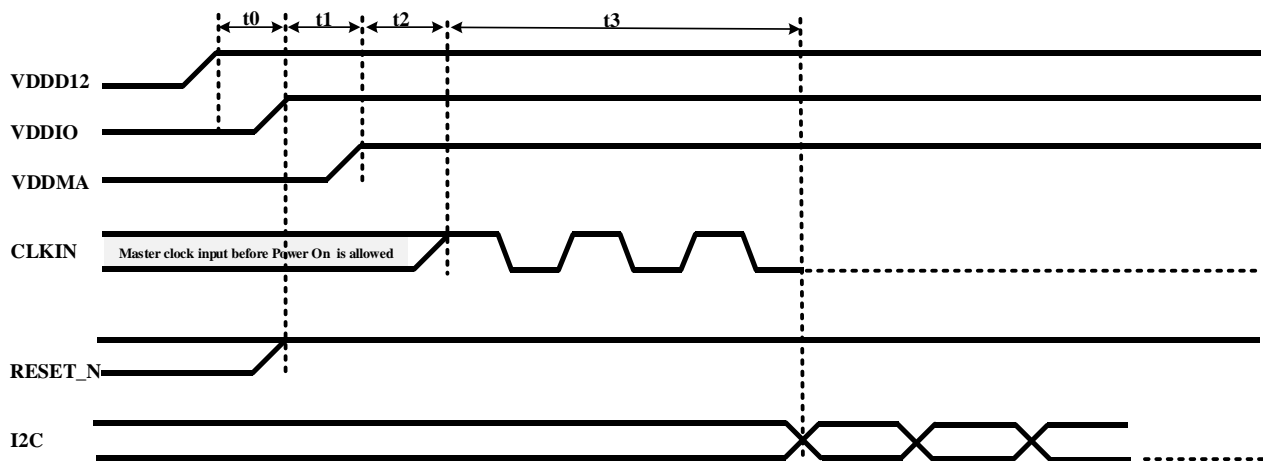
4. Power Sequence

Power-Up Sequence

The recommended power-up sequence for the PS5268 is shown as the following figure. The available power supplies must have the separation specified below.

1. Turn on VDDD12 power supply.
2. Wait at least 100 μ s (t_0), Turn on VDDIO and RESET_N must go high level.
3. Wait at least 100 μ s (t_1), Turn on VDDMA.
4. Wait at least 100 μ s (t_2), Enable CLKIN. [Note 1]
5. Wait at least 52.5ms (t_3) [Note 2], I2C starts to write sensor initial commands.

Power up Sequence



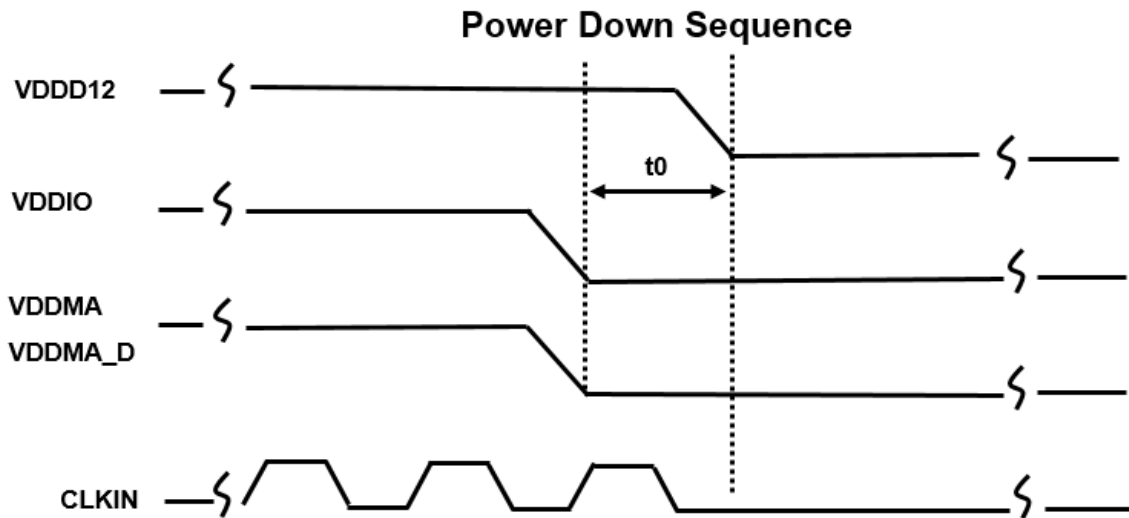
Note:

1. CLKIN enable before Power On is allowed
2. The 2.5ms of t_3 is waiting for internal POR finished, and the 50ms of t_3 is waiting for Power-up FAE finished,

Power-Down Sequence

The recommended power-down sequence for the PS5268 is shown as the following figure. The available power supplies must have the separation specified below.

1. Turn off VDDMA, VDDMA_D and VDDIO power supply simultaneously.
2. Wait at least 100 μ s (t_0), turn off VDDD12 power supply.



Software Suspend Sequence

The recommended Software Suspend sequence for the PS5268 is shown as the following description.

Address (Hex)	Bit	Name	R/W	Description
0106	[2]	SW_TG_RSTN	R/W	Soft Rst for TG circuit, Auto clear
010C	[0]	Cmd_Sw_PwrDn	R/W	CHIP Power Down
010F	[0]	Sensor_EnH	R/W	Sensor Enalbe control signal. 1 : Sensor Active
022D	[0]	T_spll_enh	R/W	CHIP Power Down

Normal → Software Suspend :

1. I2C must write Sensor_EnH = 0 to stop Digital module.
2. I2C must write Cmd_Sw_PwrDn = 1 to enter CHIP Power Down.
3. I2C must write T_spll_enh = 0 to disable SPLL.

Software Suspend → Normal:

1. I2C must write T_spll_enh = 1 to enable SPLL.
2. I2C must write Cmd_Sw_PwrDn = 0 to exit CHIP Power Down.
3. I2C must write SW_TG_RSTN = 0 to soft reset TG circuit. Then delay at least 4ms.
4. I2C must write Sensor_EnH = 1 to start Digital module.

Hardware (CSB pin) Suspend Sequence

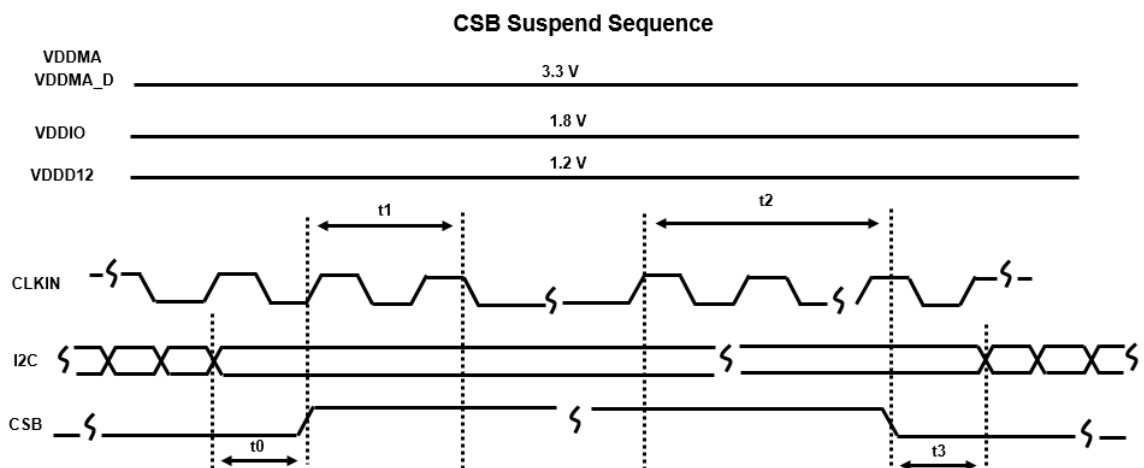
The recommended Hardware Suspend sequence for the PS5268 is shown as the following figure. The available power supplies must have the separation specified below.

Normal → Hardware Suspend :

1. I2C must write Sensor_EnH = 0 to stop Digital module.
2. I2C must write T_spll_enh = 0 to disable SPLL.
3. Wait at least 100μs (t_0), CSB pin must go high level to enter Hardware Suspend.
4. If CLKIN want to turn off due to Power consumption, wait at least 100μs (t_1)

Hardware Suspend → Normal:

1. If needed, CLKIN turn on first.
2. Wait at least 100μs (t_2), CSB must go low level to exit Hardware Suspend.
3. I2C must write T_spll_enh = 1 to enable SPLL.
4. I2C must write SW_TG_RSTN = 0 to soft reset TG circuit. Then delay at least 4ms.
5. I2C must write Sensor_EnH = 1 to start Digital module.



5. Register Table

Address (Hex)	Bit	Name	R/W	Description
0100	[7:0]	PartID[15:8]	R	Sensor ID
0101	[7:0]	PartID[7:0]	R	Sensor ID
0104	[3:0]	VersionID[3:0]	R	Sensor ID
0104	[3:0]	SubID[3:0]	R	Sensor ID
0108	[2:0]	R_PxclkO_dly[2:0]	R/W	Timing Delay for Pxclk
0109	[2:0]	R_HsyncO_dly[2:0]	R/W	Timing Delay for Hsync
010A	[2:0]	R_VsyncO_dly[2:0]	R/W	Timing Delay for Vsync
010B	[1]	Cmd_Sw_TriState	R/W	Parallel IO triState
010C	[0]	Cmd_Sw_PwrDn	R/W	CHIP Power Down
010F	[0]	Sensor_EnH	R/W	Sensor Enable control signal. 1 : Sensor Active
0111	[0]	UpdateFlag	R/W	Update flag signal.
0114	[4:0]	Cmd_LineTime [12:8]	R/W	HDR Image, Line Time = Cmd_LineTime * 0.5 clock cycles Non-HDR Image, Line Time = Cmd_LineTime * 1 clock cycles This value must be even. Note : This bit is updated with update flag
0115	[7:0]	Cmd_LineTime [7:0]	R/W	HDR Image, Line Time = Cmd_LineTime * 0.5 clock cycles Non-HDR Image, Line Time = Cmd_LineTime * 1 clock cycles This value must be even. Note : This bit is updated with update flag
0116	[7:0]	Cmd_Lpf [15:8]	R/W	Line per frame = Cmd_Lpf+ 1 Note : This bit is updated with update flag
0117	[7:0]	Cmd_Lpf [7:0]	R/W	Line per frame = Cmd_Lpf+ 1 Note : This bit is updated with update flag
0118	[7:0]	Cmd_OffNy1[15:8]	R/W	Exposure Control $2 \leq \text{Cmd_OffNy1} \leq (\text{Cmd_Lpf} - 1)$ Note : This bit is updated with update flag
0119	[7:0]	Cmd_OffNy1[7:0]	R/W	Exposure Control $2 \leq \text{Cmd_OffNy1} \leq (\text{Cmd_Lpf} - 1)$ Note : This bit is updated with update flag
0128	[0]	Cmd_SGHD	R/W	High/Low Sensitivity Selection : 0: High Sensitivity Mode 1: Low Sensitivity Mode Note : This bit is updated with update flag
012A	[6:0]	Cmd_DG_gain_idx[6:0]	R/W	Sensor Digital Gain index $0 \leq \text{Cmd_DG_gain_idx} \leq 64$
012B	[6:0]	Cmd_gain_idx[6:0]	R/W	Sensor Analog Gain index $0 \leq \text{Cmd_gain_idx} \leq 80$
0140	[0]	Cmd_Hflip	R/W	Horizontal Flip
0141	[0]	Cmd_Vflip	R/W	Vertical Flip

0142	[2:0]	Cmd_VFlip_SubBase[10:8]	R/W	When VFlip=1, Vertical readout SubBase
0143	[7:0]	Cmd_VFlip_SubBase[7:0]	R/W	When VFlip=1, Vertical readout SubBase
0144	[1:0]	Cmd_Askip_V[1:0]	R/W	Vertical Skip
0145	[2:0]	Cmd_Hsize_e1[10:8]	R/W	Raw Image Horizontal Size
0146	[7:0]	Cmd_Hsize_e1[7:0]	R/W	Raw Image Horizontal Size
0147	[2:0]	Cmd_Vsize[10:8]	R/W	Raw Image Vertical Size
0148	[7:0]	Cmd_Vsize[7:0]	R/W	Raw Image Vertical Size
0149	[2:0]	Cmd_Vstart[10:8]	R/W	Raw Image Vertical Offset
014A	[7:0]	Cmd_VStart[7:0]	R/W	Raw Image Vertical Offset
014B	[2:0]	Cmd_ISP_VSize[10:8]	R/W	ISP Image Vsize, This signal is clamping Image vertical size for LTM function and must be set with even value. Note : This bit is updated with update flag. Cmd_ISP_Vsize & Cmd_Vsize must update at same frame
014C	[7:0]	Cmd_ISP_VSize[7:0]	R/W	ISP Image Vsize, This signal is clamping Image vertical size for LTM function and must be set with even value. Note : This bit is updated with update flag. Cmd_ISP_Vsize & Cmd_Vsize must update at same frame
0162	[3:0]	Cmd_Np[3:0]	R/W	Cmd_Np = 0~15 Np_divider vs. Cmd_Np is mapping table
0177	[2]	R_FrameSyncMaster	R/W	0: Normal Mode. 1: Master Mode: Output one pulse trigger signal.
	[1]	R_FrameSyncWait	R/W	0: Continuous output after one pulse trigger signal. 1: One frame output after one pulse trigger signal.
	[0]	R_FrameSyncMode	R/W	0: Normal Mode. 1: Frame Sync Mode.
0178	[7:0]	R_FirmReg0[7:0]	R/W	Firmware test Register
0179	[7:0]	R_FirmReg1[7:0]	R/W	Firmware test Register
022B	[0]	T_spll_div2_enH	R/W	SPLL clock divider2 selection sppll_divider=1 when T_spll_div2_enH=0 sppll_divider=2 when T_spll_div2_enH=1
022C	[5:4]	T_spll_modedivider [1:0]	R/W	SPLL mode selection modedivider=1 when T_spll_modedivider=0 modedivider=2 when T_spll_modedivider=1 modedivider=4 when T_spll_modedivider=2
022D	[0]	T_spll_enh	R/W	0 : SPLL disable 1 : SPLL enable
022E	[5:0]	T_spll_predivider[5:0]	R/W	SPLL clock divider, sppll_predivider= T_spll_predivider+2
022F	[5:0]	T_spll_postdivider [5:0]	R/W	SPLL clock scalar sppll_postdivider= T_spll_postdivider+2

0246	[4]	T_digclk_div2	R/W	PixelClock divider2 selection digclkdivider=1 when T_digclk_div2=0 digclkdivider=2 when T_digclk_div2=1
024C	[2:0]	T_mipi_vtx_trim[2:0]	R/W	Fine tune the MIPI CK/DP swing
0252	[5:0]	T_pll_predivider[5:0]	R/W	MIPI pll clock divider, pll_predivider= T_pll_predivider+2
0253	[5:0]	T_pll_postdivider[5:0]	R/W	MIPI pll clock scalar pll_postdivider= T_pll_postdivider+2
0254	[0]	T_pll_enh	R/W	0 : MIPI PLL disable 1 : MIPI PLL enable
0255	[4]	T_pll_div2_EnH	R/W	MIPI pll clock divider2 selection pllclkdivider=1 when T_pll_div2_EnH =0 pllclkdivider=2 when T_pll_div2_EnH =1
0259	[4]	T_SR[4]	R/W	IO slew control
	[1:0]	T_OPDRV_GPIO[1:0]	R/W	IO driving Strength
0501	[4:0]	R_ISP_TestMode[4:0]	R/W	Test Image Control
0502	[7:0]	R_ISP_TestValueLo[7:0]	R/W	Test Image Control
0503	[7:0]	R_ISP_TestValueHi[7:0]	R/W	Test Image Control
0700	[0]	Cmd_ColorGain_Bypass	R/W	Color Gain function bypass Note : This bit is updated with frame base
0701	[7]	Cmd_ColorGainB[8]	R/W	Internal Color Gain – Blue channel
0702	[7:0]	Cmd_ColorGainB[7:0]	R/W	
0703	[7]	Cmd_ColorGainG[8]	R/W	Internal Color Gain – Green channel
0704	[7:0]	Cmd_ColorGainG[7:0]	R/W	
0705	[7]	Cmd_ColorGainR[8]	R/W	Internal Color Gain – Red channel
0706	[7:0]	Cmd_ColorGainR[7:0]	R/W	
0856	[0]	temp_save[8]	R/W	Report the temp_save
0857	[7:0]	temp_save[7:0]	R/W	Report the temp_save
0903	[0]	Cmd_DigDac_Minus_Uniformity	R/W	ABC minus high temp digdac
0905	[2:0]	R_DLNU_ABC_Modify1[10:8]	R/W	ABC Shift DigDac reference value
0906	[7:0]	R_DLNU_ABC_Modify1[7:0]	R/W	ABC Shift DigDac reference value
0907	[2:0]	R_DLNU_FDC_Modify1[10:8]	R/W	FDC Shift DigDac reference value
0908	[7:0]	R_DLNU_FDC_Modify1[7:0]	R/W	FDC Shift DigDac reference value
090E	[2:0]	R_DLNU_ABC_Modify2[10:8]	R/W	ABC Shift DigDac reference value
090F	[7:0]	R_DLNU_ABC_Modify2[7:0]	R/W	ABC Shift DigDac reference value
0910	[2:0]	R_DLNU_FDC_Modify2[10:8]	R/W	FDC Shift DigDac reference value
0911	[7:0]	R_DLNU_FDC_Modify2[7:0]	R/W	FDC Shift DigDac reference value
0C00	[1]	Cmd_DG_EnH	R/W	Digital Gain function enable Note : This bit is updated with frame base
	[0]	Cmd_DG_Bypass	R/W	Digital Gain function Bypass Note : This bit is updated with frame base

0C01	[5:0]	Cmd_DG_Offset_1X[5:0]	R/W	AutoOffset after DG : AG1X ~ AG2X
0C02	[5:0]	Cmd_DG_Offset_2X[5:0]	R/W	AutoOffset after DG : AG2X ~ AG4X
0C03	[5:0]	Cmd_DG_Offset_4X[5:0]	R/W	AutoOffset after DG : AG4X ~ AG8X
0C04	[5:0]	Cmd_DG_Offset_8X[5:0]	R/W	AutoOffset after DG : AG8X ~ AG16X
0C05	[5:0]	Cmd_DG_Offset_16X[5:0]	R/W	AutoOffset after DG : AG16X ~ AG32X
0C06	[5:0]	Cmd_DG_Offset_32X[5:0]	R/W	AutoOffset after DG : AG32X
0C07	[7:0]	Cmd_DG_Offset_RGain[7:0]	R/W	When ColorGain is set behind the DG_Offset module, Cmd_DG_Offset_RGain = ColorGainR Note : This bit is updated with frame base
0C08	[7:0]	Cmd_DG_Offset_GGain[7:0]	R/W	When ColorGain is set behind the DG_Offset module, Cmd_DG_Offset_GGain = ColorGainG Note : This bit is updated with frame base
0C09	[7:0]	Cmd_DG_Offset_BGain[7:0]	R/W	When ColorGain is set behind the DG_Offset module, Cmd_DG_Offset_BGain = ColorGainB Note : This bit is updated with frame base
0D00	[7:0]	R_ImgSyn_SGHD_EnH	R/W	HDR Image use SGHD
0E00	[4]	Cmd_Pxclk_Inv	R/W	PxClk inverse Out Note : This bit is updated with update flag If SubSampling = 1 and use MIPI_OUT, then Cmd_Pxclk_Inv must be 1
	[3]	Cmd_Vsync_Inv	R/W	Vsync inverse Out Note : This bit is updated with update flag
	[2]	Cmd_Hsync_Inv	R/W	Hsync inverse Out Note : This bit is updated with update flag
0E02	[4:0]	Cmd_TrimV_Back_Num1[12:8]	R/W	TrimV Blanking, When 0, if $x \leq$ Cmd_TrimV_Back_Num1 Note : This bit is updated with update flag
0E03	[7:0]	Cmd_TrimV_Back_Num1[7:0]	R/W	TrimV Blanking, When 0, if $x \leq$ Cmd_TrimV_Back_Num1 Note : This bit is updated with update flag
0E04	[4:0]	Cmd_TrimV_Back_Num2[12:8]	R/W	TrimV Blanking, When 1, if $\text{Cmd_TrimV_Back_Num1} < x \leq$ Cmd_TrimV_Back_Num2 Note : This bit is updated with update flag
0E05	[7:0]	Cmd_TrimV_Back_Num2[7:0]	R/W	TrimV Blanking, When 1, if $\text{Cmd_TrimV_Back_Num1} < x \leq$ Cmd_TrimV_Back_Num2 Note : This bit is updated with update flag
0E0A	[0]	Cmd_Askip_H	R/W	Horizontal Skip
0E0B	[4:0]	Cmd_WOI_VOffset[12:8]	R/W	Vertical offset of output image
0E0C	[7:0]	Cmd_WOI_VOffset[7:0]	R/W	Vertical offset of output image
0E0D	[4:0]	Cmd_WOI_VSize[12:8]	R/W	Vertical size of output image

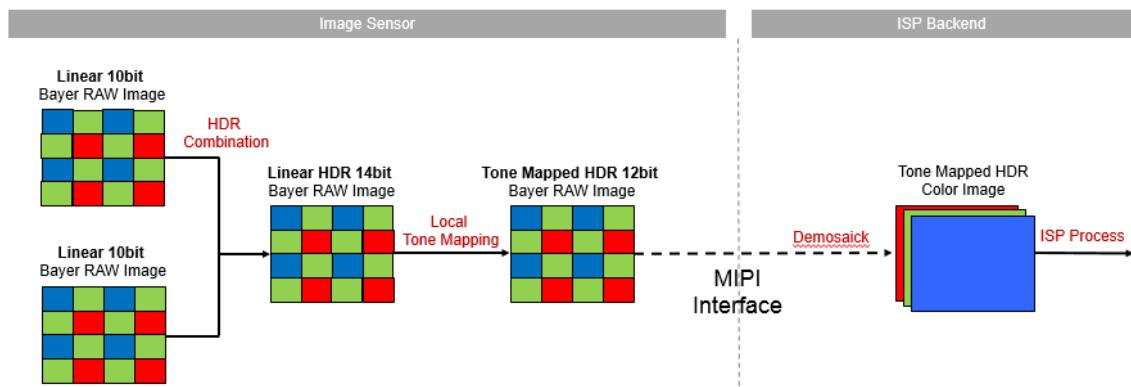
0E0E	[7:0]	Cmd_WOI_VSize[7:0]	R/W	Vertical size of output image
0E0F	[4:0]	Cmd_WOI_HOffset[12:8]	R/W	Horizontal offset of output image
0E10	[7:0]	Cmd_WOI_HOffset[7:0]	R/W	Horizontal offset of output image
0E11	[4:0]	Cmd_WOI_HSize[12:8]	R/W	Horizontal size of output image
0E12	[7:0]	Cmd_WOI_HSize[7:0]	R/W	Horizontal size of output image
0F37	[6]	AE_FW_READY	R	FAE operation done
0F37	[2]	AE_LOW_LIGHT_RPT	R	If AE_GEP > 0x200, this bit would be 1
1200	[0]	Cmd_ImgSyn_Bypass	R/W	HDR Image Synthesis Data Bypass Enable
1201	[0]	Cmd_ImgSyn_EnH	R/W	HDR High/Low Gain Image Synthesis Enable while Cmd_ImgSyn_Bypass =0 and Cmd_ImgSyn_EnH =1 Note : This bit is updated with frame base
1300	[0]	R_LTM_Bypass	R/W	LTM Data Bypass Enable Note : This bit is updated with frame base
1301	[0]	R_LTM_EnH	R/W	LTM Enable while R_LTM_Bypass =0 and R_LTM_EnH =1 Note : This bit is updated with frame base
1303	[0]	Cmd_LTM_Patch_Manual	R/W	0 : LTM patch manual disable 1 : LTM patch manual enable
1304	[0]	Cmd_LTM_Limit[5:0]	R/W	Limit LTM gain, let lowlight image don't too noisy
1306 ~ 1308	[3:0]	Cmd_LTM_Brightness_XX[3:0]	R/W	LTM Brightness parameter setting
1309 ~ 130B	[3:0]	Cmd_LTM_DeHaze_XX[3:0]	R/W	LTM DeHaze parameter setting
130C ~ 1311	[3:0]	Cmd_LTM_BackLight_XX[7:0]	R/W	LTM BackLight parameter setting
1406	[2:0]	R_data_format[2:0]	R/W	Data Type: R_data_format =3, RAW8 R_data_format =4, RAW10(Default) R_data_format =5, RAW12 R_data_format =6, RAW14
1409	[7:0]	R_tx_data_settle_prd[7:0]	R/W	MIPI timing control
140A	[7:0]	R_tx_data_sp_blank_prd[7:0]	R/W	MIPI timing control
140C	[7:0]	R_phyclk_lps_prd[7:0]	R/W	MIPI timing control
140F	[0]	R_CSI2_enable	R/W	0 : MIPI digital module stop 1 : MIPI digital module start
1410	[2:0]	R_tx_lane_num[2:0]	R/W	MIPI Lane Number R_tx_lane_num=1, 1Lane R_tx_lane_num=2, 2Lane
1411	[0]	R_phyclk_cont_mode	R/W	MIPI CKP/CKN signal mode selection: 0 : LP / HS mode switch 1 : Always HS mode
1415	[7:0]	R_LPX_prd[7:0]	R/W	MIPI timing control
1417	[7:0]	R_HsPrep_prd[7:0]	R/W	MIPI timing control
1418	[7:0]	R_HsEoT_prd[7:0]	R/W	MIPI timing control
141B	[7:0]	R_ckln_HsPrep_prd[7:0]	R/W	MIPI timing control

141C	[7:0]	R_ckln_HsEoT_prd[7:0]	R/W	MIPI timing control
141E	[7:0]	R_ckln_zero_prd[7:0]	R/W	MIPI timing control
1425	[0]	Cmd_CSI2_Stall	R/W	MIPI timing control
1482	[1]	tx_sram_full_error_flag	R	SRAM full error, overflow
1482	[0]	tx_sram_empty_error_flag	R	SRAM empty error, underflow
14B0	[0]	R_MIPI_skip_line_sp	R/W	MIPI data lane if skip LS/LE short packet : 0 : don't skip LS/LE packet 1 : skip LS/LE packet

6. HDR Image Control

The sensor perform single exposure with dual sensitivity image data and on-chip combine dual image data line-by-line as a linear high dynamic range 14bit data. Then sensor perform local tone mapping from higher data bits (14bits) to lower data bits (12bit) for suppressing data range and enhancing local contrast during the process.

Finally, the sensor output tone mapped RAW 12bit or 10bit data via MIPI interface. Backend chip received the tone mapped RAW data without complex HDR timing and combination while using staged HDR sensor.



- **Local Tone Mapping**

Local Tone Mapping is a function used to map one set of data to another to approximate the appearance of high-dynamic-range images in a medium that has a more limited dynamic range. Tone mapping addresses the problem of strong contrast reduction from the scene radiance to the displayable range while preserving the image details and color appearance important to appreciate the original scene content.

PS5268 provides three kinds parameters can fine-tune LTM performance. (ie. Brightness、DeHaze、BackLight)

7. FAE (Fast Auto Exposure)

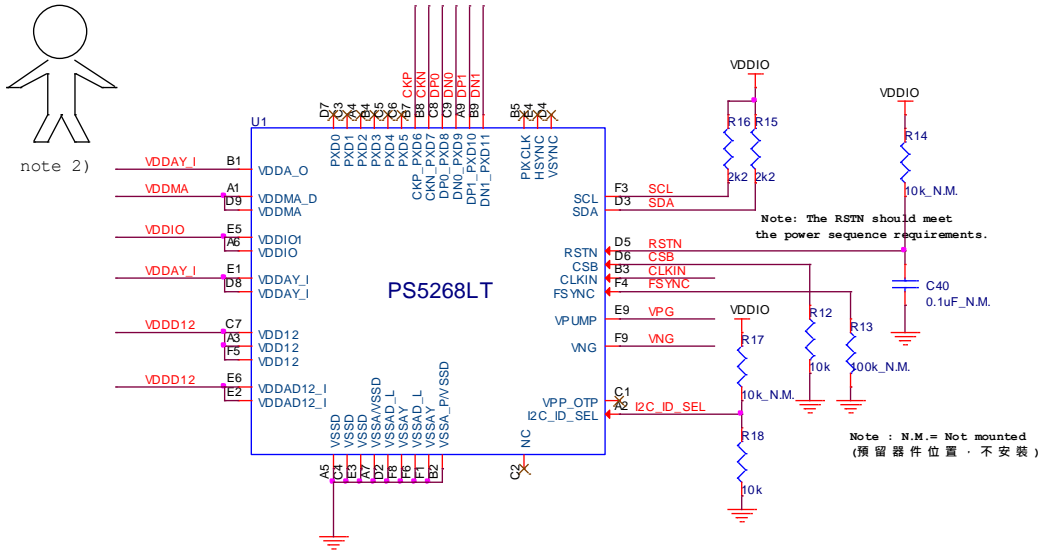
FAE 是透過畫面的 Yavg，快速的將曝光收斂至期望區間，並產生對應的 Exposure_LineNumber, High/Low Sensitivity Selection, Analog Gain, Digital Gain 值，以便提供 Cmd_OffNy、Cmd_sghd、

Cmd_gain_idx、Cmd_DG_gain_idx 予客戶收到第一張影像時，ISP AE 收斂第一張影像的參考。

需注意：PS5268 FAE 的運作時機只會發生在重新上電的過程，同時必須搭配上電時序，請參考 DataSheet “Power-Up Sequence” 章節描述。Hardware Reset (RSTN pin)、Hardware CSB (CSB pin)、Software PowerDown (Cmd_Sw_PwrDn) 的操作並不會執行 FAE。

8. Reference Circuit Schematic

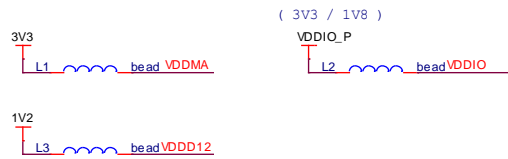
MIPI Interface:



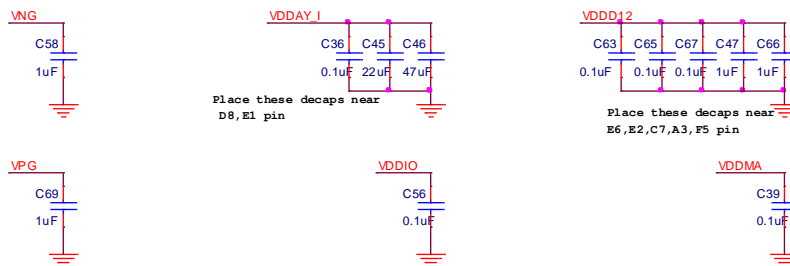
Sensor Interface



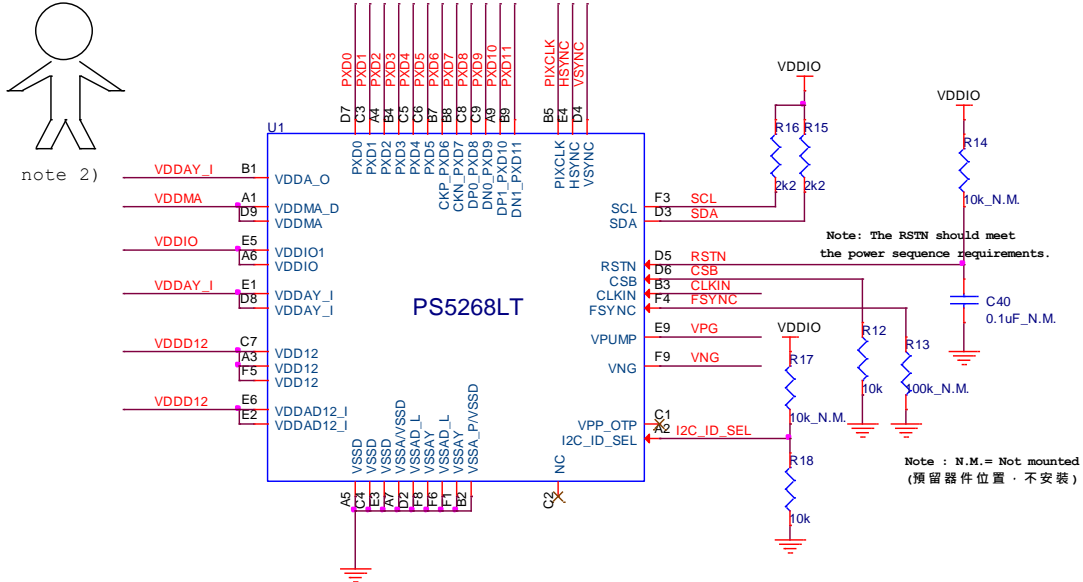
Main Power



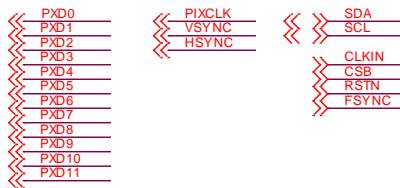
Bypass caps should be placed as close to the power pins as possible



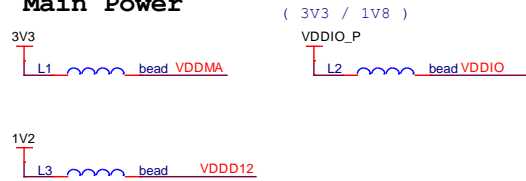
Parallel Interface:



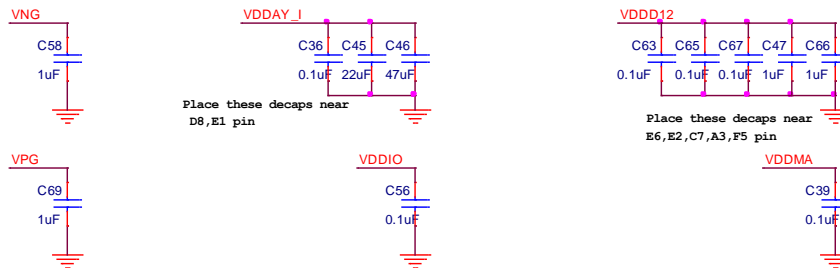
Sensor Interface



Main Power



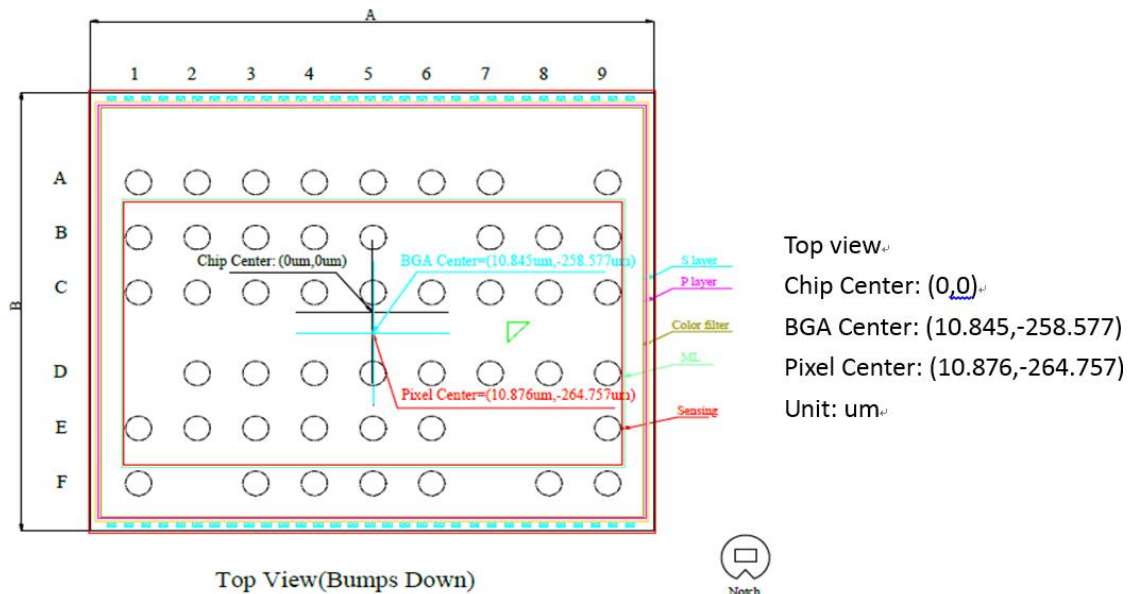
Bypass caps should be placed as close to the power pins as possible

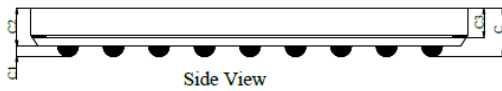
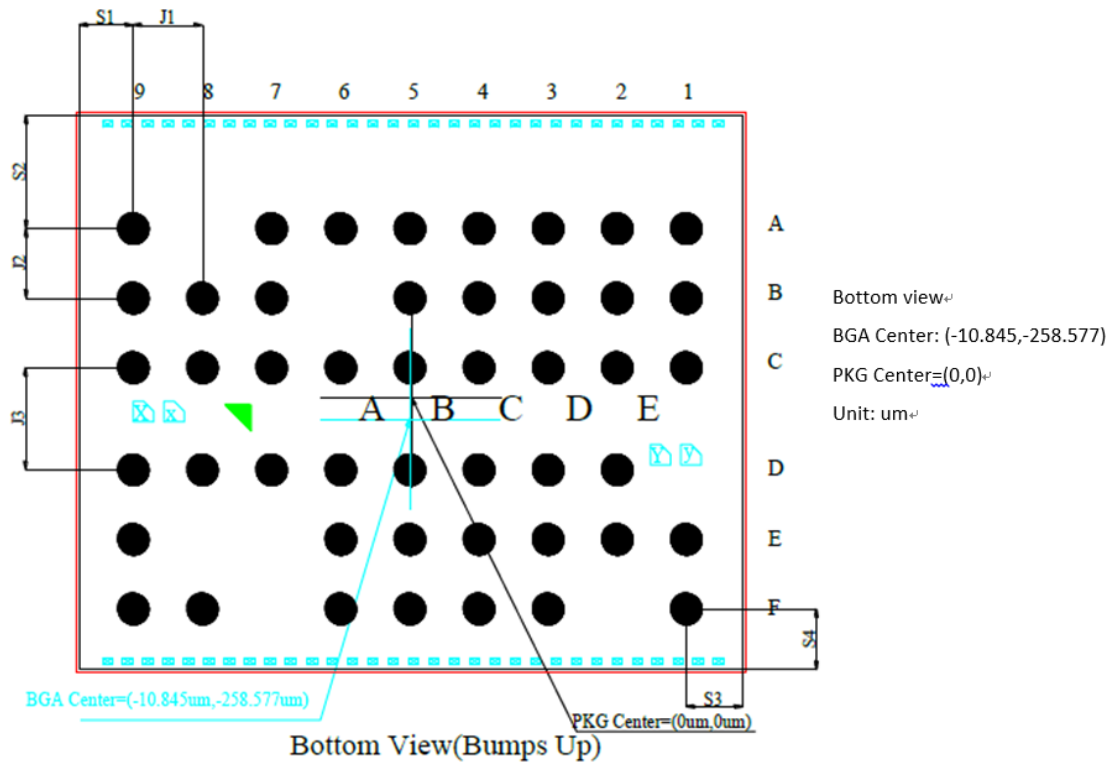


Package Information

 ● **Package Outline Dimension**

	Symbol	Nominal	Min	Max	Nominal	Min	Max	
		Millimeters			Inches			
Package Body Dimension X	A	6.524	6.499	6.549	0.25685	0.25587	0.25783	
Package Body Dimension Y	B	5.419	5.394	5.444	0.21335	0.21236	0.21433	
Package Height	C	0.820	0.760	0.880	0.03228	0.02992	0.03465	
Ball Height	C1	0.160	0.130	0.190	0.00630	0.00512	0.00748	
Package Body Thickness	C2	0.660	0.625	0.695	0.02598	0.02461	0.02736	
Thickness from top glass surface to wafer	C3	0.445	0.425	0.465	0.01752	0.01673	0.01831	
Ball Diameter	D	0.300	0.270	0.330	0.01181	0.01063	0.01299	
Total Ball Count	N	47 (1NC)						
Pins pitch X axis	J1	0.680						
Pins pitch Y axis	J2	0.680						
Pins pitch Y axis	J3	1.000						
Edge to Pin Center Distance along X	S1	0.5311550	0.5011550	0.5611550	0.020912	0.019731	0.022093	
Edge to Pin Center Distance along Y	S2	1.1080770	1.0780770	1.1380770	0.043625	0.042444	0.044806	
Edge to Pin Center Distance along X	S3	0.5528450	0.5228450	0.5828450	0.021766	0.020584	0.022947	
Edge to Pin Center Distance along Y	S4	0.5909230	0.5609230	0.6209230	0.023265	0.022084	0.024446	

Mechanical Drawing




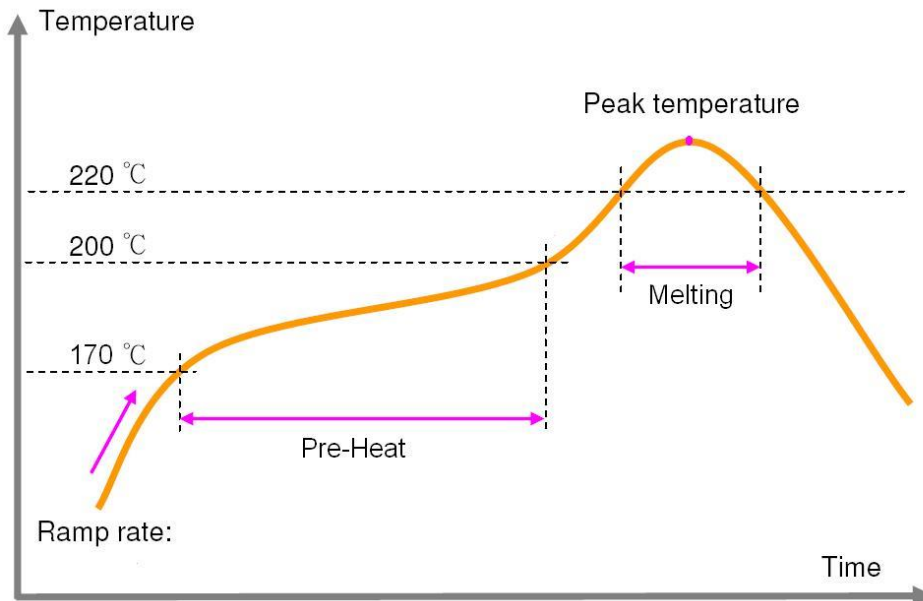
Laser Mark:
 ABCD: 4 digit datecode provide by PXI along with PO
 E: Wafer ID, A-Y represent #01-#25

● **Recommended Guideline for PCB Assembly**

- I. Recommended vender and type for Pb-free solder paste
 - 1 Almit LFM-48W TM-HP
 - 2 Senju M705-GRN360-K

II. IR Reflow Soldering Profile:

Temperature profile is the most important control in reflow soldering. It must be fine-tuned to establish a robust process. The typical recommended IR reflow profile is showed in figure below.

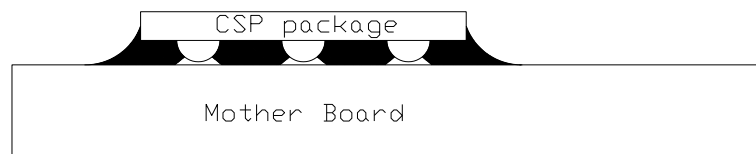


- **Reflow Profile**

1. Average Ramp-up Rate (30°C to preheat zone): 1.5~ 2.5 Degree C/ Sec
2. Preheat zone:
 - 2.1 Temp ramp from 170~ 200 degree C
 - 2.2 Exposure time: 90 +/- 30 sec
3. Melting zone:
 - 3.1 Melting area temp > 220 degree C for at least 30 ~ 50 sec
 - 3.2 Peak temperature: 245 degree C.

III. Others

- **Epoxy under-filled process is required post IC mounting process.**



- **Peek tweezers or plastic tweezers is required post IC manual handling for pick and place.**



9. Revision History

Revision	Description	Date
V0.9	Preliminary data sheet released	Jul. 31, 2019
V1.0	2 nd data sheet released	Aug. 18, 2019
V1.1	Change the default part number	Sep. 24, 2019