Crystal Image through
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PIXELPLUS

Datasheet

1/4 inch VGA Single Chip
CMOS Image Sensor with NTSC/PAL Transmitter

PC7080D

Rev 1.1

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Table of Contents

List of Figures

List of Tables

Features

- 648 x 488 effective pixel array with RGB bayer color filters and micro-lens
- Interface
  - Composite Output
    - CVBS(NTSC/PAL)
  - Digital Output
    - YCbCr422 / RGB565 / RGB444 / Bayer
  - Analog / Digital Output
    - ITU-R. BT6565 / CVBS
- Image processing on chip : lens shading compensation, gamma correction, defect correction, color correction, NR(2D noise reduction), color interpolation, edge enhancement, brightness, contrast, de-color, auto black level compensation, auto white balance, auto exposure control, back light compensation
- Programmable frame size, window size and position
- Free scaling (scale down)
- Horizontal/Vertical mirroring
- Automatic flicker cancellation
- I2C master included
- Chip address selection PAD
- Software reset
- On chip regulator for core
- Crystal input support

General Description

The PC7080D is a 1/4-inch CMOS image sensor with NTSC/PAL Transmitter. It's a single chip with effective pixel array of 648 (width) x 488 (height). The PC7080D can generate analog/digital/composite outputs at maximum frame rate of 60. On-chip sensor functions are controllable through I2C interface.

Table 1 Key Performance Parameter

Parameter	Typical value
Pixel size	5.6 [um] x 5.6 [um]
Effective pixel array	648 (H) x 488 (V)
Effective image area	3.63 [mm] x 2.73 [mm]
Optical format	1/4 [inch]

Parameter	Typical value
Input clock frequency	27 [MHz]
Output interface	10/8-bit parallel with ITU-R. BT656 (CSP Package Only)
	CVBS (NTSC/PAL)
Max. frame rate	60 fps : ITU-R. BT656 @ 27[MHz] (for NTSC)
	50 fps : ITU-R. BT656 @ 27[MHz] (for PAL)
	60fields/sec NTSC(CVBS) @ 27[MHz]
	50fields/sec PAL(CVBS) @ 27[MHz]
	60 fps : YCbCr422/RGB565/RGB444 @ 54[MHz]
	60 fps : Bayer @ 27[MHz]
Dark signal	14.5 [mV/sec] @ 60 [°C]
Sensitivity	13.2 [V/Lux.sec]
Power supply	AVDD : 3.3 [V]
	HVDD : 3.3 [V]
	CVDD : 3.3 [V]
	DVDD : 1.5 [V]
Power consumption	129 [mW] @ dynamic (DVP)
	254 [mW] @ dynamic (CVBS)
	519 [uW] @ standby
Operating Temp. (Fully Functional Temp.)	-40~85 [°C] (Ambient)
Dynamic range	65.8 [dB]
SNR	48.6 [dB]
Package Type	40CSP / 40CLCC / 40PLCC

Chip Architecture

The PC7080D has a 652 x 504 total pixel array and includes column/row driver circuits for reading out pixel data progressively. CDS circuit reduces noises generated from various sources, which mainly are resulted from process variations. The fixed errror signal level caused by pixel process variation can be reduced by sampling the defference between the output and the reset level of the pixel. Each of R, G, and B pixel output can be multiplied by different gain factors to balance the color of images under various light conditions. The analog signals are converted into digital data of one line at a time and each line data is streamed out column by column. The Bayer RGB data passes through a sequence of image signal processing to produce various output datas. Image signal processing includes operations such as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. The PC7080D supports various interfaces such as composite, analog, and digital output. The control of internal functions and output signal timings can be enabled by modifying registers directly through a 2-wire serial interface called I2C or by programming the internal/external ROMs which contain device settings.

BT656 formatter supports 10-bit digital output and TV encoder supports CVBS analog output.

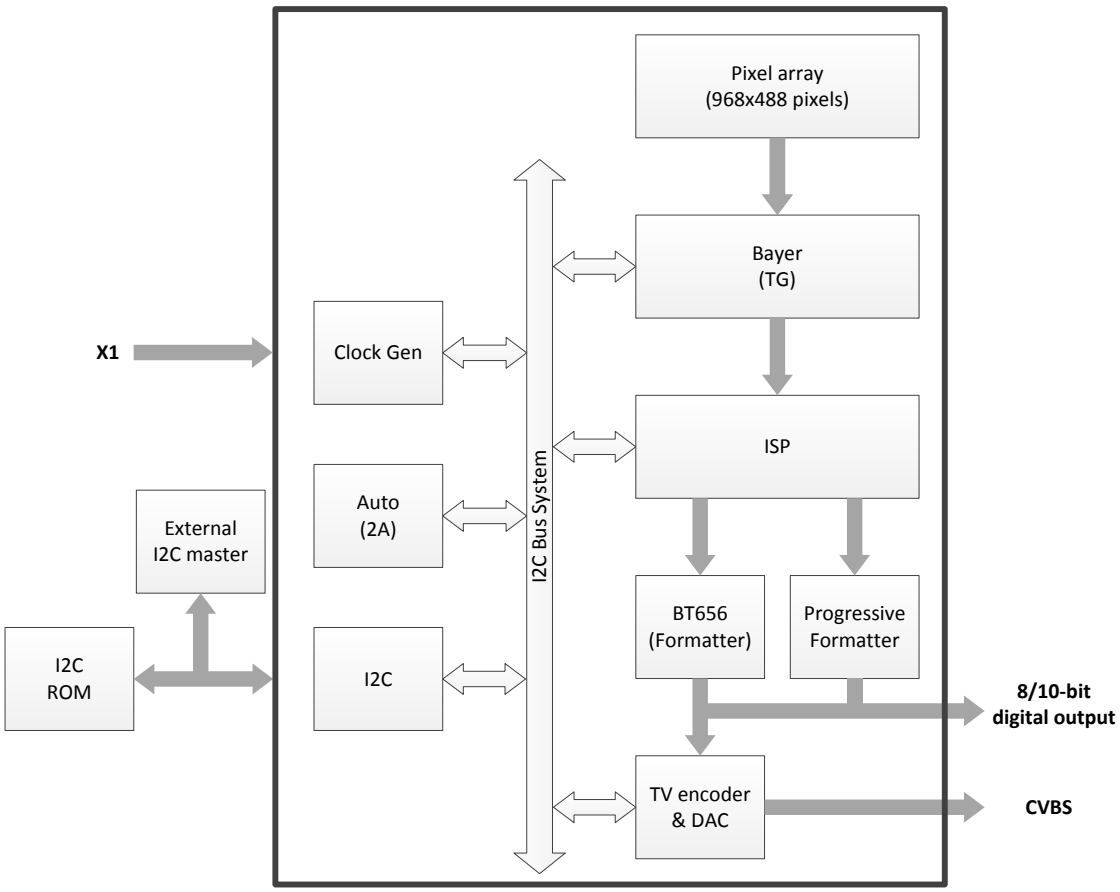


Figure 1 Chip architecture

Frame Structure

The size of a frame is determined by framewidth and frameheight registers. One frame consists of (framewidth + 1) columns and (frameheight + 1) rows, where the size of one frame is allowed to be larger than the total pixel array size. Window determines the output image size, and its default size is 640 x 480 pixels. It is possible to define a specific region of the frame by a determined window. Pixel scanning is performed row by row on entire frame. Frame row counter and frame column counter, which are limited by framewidth and frameheight values respectively, are used to indicate the current coordinate of pixel being scanning. The column counter value increase by every pixel clock (pclk). every time the column counter reaches maximum value, the row counter value increase. Figure 2 shows the default frame structure and the window position of the PC7080D with origin point (0,0) in the top right corner .

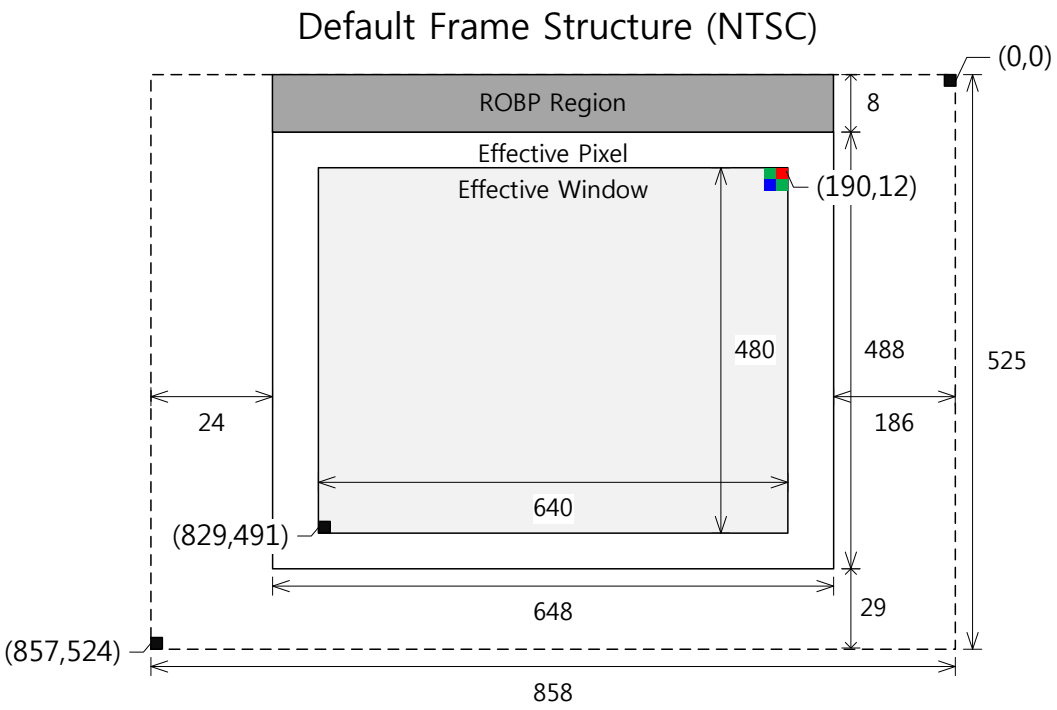


Figure 2 Default frame structure(top view)

Table 2 Register Table - Frame structure

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
framewidth_h	A	06	[3:0]	0xx	RW	aev	Framewidth
framewidth_l	A	07	[7:0]	0xx	RW	aev	
fd_fheight_a_h	A	08	[4:0]	0x02	RW	aev	Frameheight
fd_fheight_a_l	A	09	[7:0]	0xx	RW	aev	
fd_fheight_b_h	A	0A	[4:0]	0x02	RW	aev	
fd_fheight_b_l	A	0B	[7:0]	0xx	RW	aev	
m_tg_frameheight_H	B	E4	[7:0]		RO		Tg frameheight monitoring
m_tg_frameheight_L	B	E5	[7:0]		RO		
m_tg_framewidth_H	B	E6	[7:0]		RO		Tg framewdith monitoring
m_tg_framewidth_L	B	E7	[7:0]		RO		

Data Format

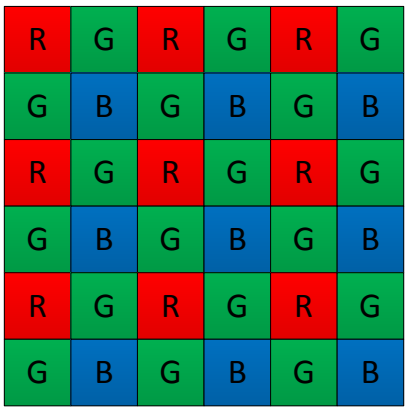


Figure 3 Bayer color filter pattern

Pixel array is covered with Bayer color filters as can be seen in the Figure 3. Since each pixel can have only one type of filter on it, only one color component can be produced by a pixel. PC7080D provides this Bayer pattern RGB data through an 10bit channel. It takes one pclk to pass one pixel RGB data to output bus. But since it is necessary to know all 3 color components R, G, B to produce a color for a pixel, the other two components must be inferred from other pixel data. For example, G component for a B pixel is calculated as an average of its four nearest G neighbors, and its R component as an average of its four nearest R neighbors. This operation of inferring missing data from existing ones is called the color interpolation. Color interpolation produces an undesirable artifact in image. Sampling nature of color filter can leave an interference pattern around an area with repetitive fine lines. PC7080D adopts a low pass filter to prevent the interference patterns (called Moire pattern) from degrading the image quality too much. After color interpolation, every pixel has all three color components.

It is possible to extract monochrome luminance data from RGB color components. And the color information is separated from luminance information. Since human eyes are less sensitive to color variation than to luminance, color components can be sub-sampled to reduce the amount of data to be transmitted, but preserving almost the same image quality. Figure 4 shows 4:2:2 YUV data sequence. PC7080D supports 4:2:2 YUV data format where U and V components are sampled once every two Y components (the format skips one set of U and V components). Therefore, each pixel utilizes one Y component and shares U and V component to represent color and brightness of a pixel.

Figure 4 YUV422 data sequence

Table 3 Register Table - Format control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
format	C	9E	[7:0]	0x00	RW	aev	Format control
o8bit	C	9C	[7]	1'b1	RW	aev	8bit output only mode @yuv format

Vsync and Hsync

By manipulating vsyncstartrow_f0, vsyncstoprow_f0, and vsynccolumn register value, start and stop positions of vsync are controlled. sync_drop register allows user to drop vsync or hsync. Figure 5 shows 4 different cases of sync_drop. In addition, sync_hsyncAllLines enables hsync during vsync blank region. Figure 6 shows operation of sync_hsyncAlllines.

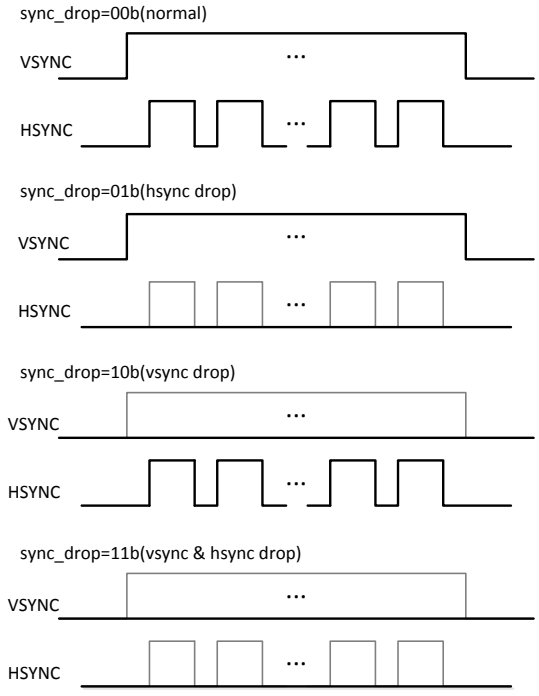


Figure 5 Sync drop

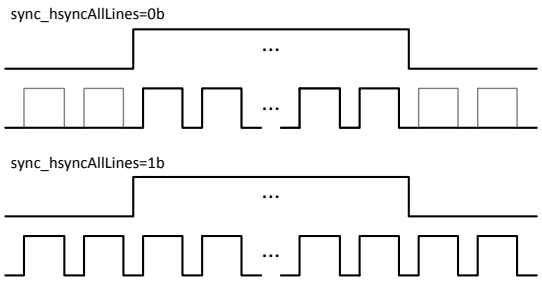
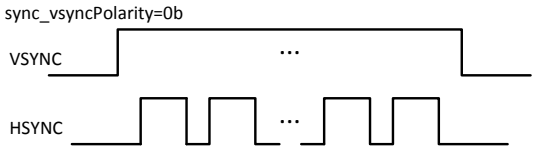


Figure 6 Hsync all lines

sync_vsyncPolarity, sync_hsyncPolarity, sync_pclkPolarity registers invert vsync, hsync, PCLK signal respectively. The inversion functions are shown in Figure 7, Figure 8, Figure 9.



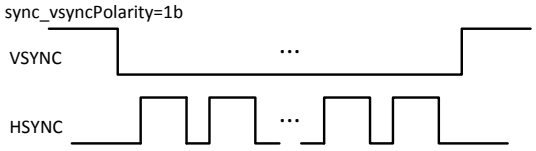
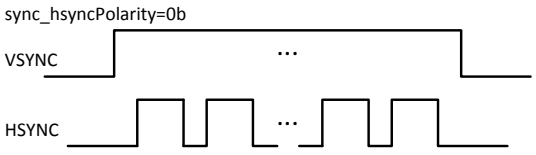


Figure 7 Vsync polarity



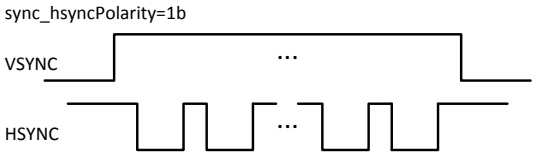


Figure 8 Hsync polarity

Table 4 Register Table - Sync control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
chip_mode	A	04	[1:0]	0xx	RW	aev	chip mode selection 2'b00 : CCIR656 else : N/A
vsyncstartrow_f0_h	A	14	[4:0]	0x00	RW	aev	Vsync generation
vsyncstartrow_f0_l	A	15	[7:0]	0x17	RW	aev	
vsyncstoprow_f0_h	A	16	[4:0]	0x01	RW	aev	
vsyncstoprow_f0_l	A	17	[7:0]	0xx	RW	aev	
vsyncstartrow_f1_h	A	18	[4:0]	0x01	RW	aev	
vsyncstartrow_f1_l	A	19	[7:0]	0xx	RW	aev	
vsyncstoprow_f1_h	A	1A	[4:0]	0x02	RW	aev	
vsyncstoprow_f1_l	A	1B	[7:0]	0xx	RW	aev	
vsynccolumn_h	A	1C	[3:0]	0x00	RW		
vsynccolumn_l	A	1D	[7:0]	0x02	RW		
sync_drop[1:0]	C	9A	[6:5]	2'b00	RW	aev	2'b00 : disable 2'b01 : hsync drop 2'b10 : vsync drop 2'b11 : hsync and vsync drop
sync_vsyncPolarity	C	9B	[6]	1'b0	RW	aev	vsync polarity change

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
sync_hsyncAllLines	C	9B	[5]	1'b0	RW	aev	hsync output all lines enable(blank and active)
sync_hsyncPolarity	C	9B	[4]	1'b0	RW	aev	hsync polarity change
vsync_pad_en	A	29	[7]	1'b0	RW		vsync pad enable
hsync_pad_en	A	29	[4]	1'b0	RW		hsync pad enable
hsync_drv[1:0]	A	29	[6:5]	2'b00	RW		hsync pad drivability
pad_drv	A	28	[7:6]	2'b00	RW		Fix to 2'b00 vsync, D9~D0 pad drivability

PCLK

PCLK rate is set by dividing pclk, and the division ratio is determined by sync_pclkrate. In addition, PCLK inversion can be enabled via sync_pclkPolarity register as shown in Figure 9.

Table 5 PCLK rate

pclk_rate	PCLK
0d	pclk
1d	pclk x 1/2

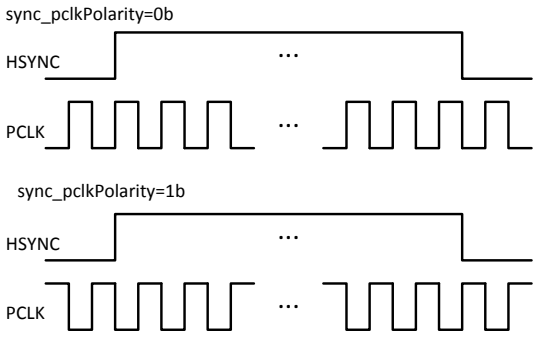


Figure 9 PCLK polarity

Table 6 Register Table - PCLK control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
sync_pclkrate	C	9A	[4:0]	5'b00000	RW	aev	PCLK rate
sync_pclkPolarity	C	9B	[2]	1'b0	RW	aev	PCLK polarity change
pclk_drv	A	28	[5:4]	2'b00	RW		PCLK drivability control
digi_pclk_delay	A	3F	[3:0]	4'b0000	RW		PCLK delay control
pclk_pad_en	A	28	[0]	1'b0	RW		PCLK pad enable

Windowing

Window sets pixel region displayed to users. The PC7080D outputs pixel datas within window when hsync and vsync are high. windowx1, windowx2, windowy1, and windowy2 registers determine the position and size of the window. upper right corner of window = (windowx1, windowy1)

lower left corner of window = (windowx2, windowy2)

Table 7 Register Table - Window

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
windowx1_h	A	0C	[1:0]	0x00	RW	aev	Window size control
windowx1_l	A	0D	[7:0]	0x01	RW	aev	
windowy1_h	A	0E	[1:0]	0x00	RW	aev	
windowy1_l	A	0F	[7:0]	0x01	RW	aev	
windowx2_h	A	10	[1:0]	0x02	RW	aev	
windowx2_l	A	11	[7:0]	0x80	RW	aev	
windowy2_h	A	12	[1:0]	0x01	RW	aev	
windowy2_l	A	13	[7:0]	0xE0	RW	aev	

Scale

Full scaled image pixel location
X point = 32*M
Y point = 32*N
Scaled image sampling point
X Sampling point = scale_x*P
Y Sampling point = scale_y*Q

When scale_x and scale_y are 32d. The scale ratio is 1:1 and the maximum horizontal and vertical scale ratio is 1/8.

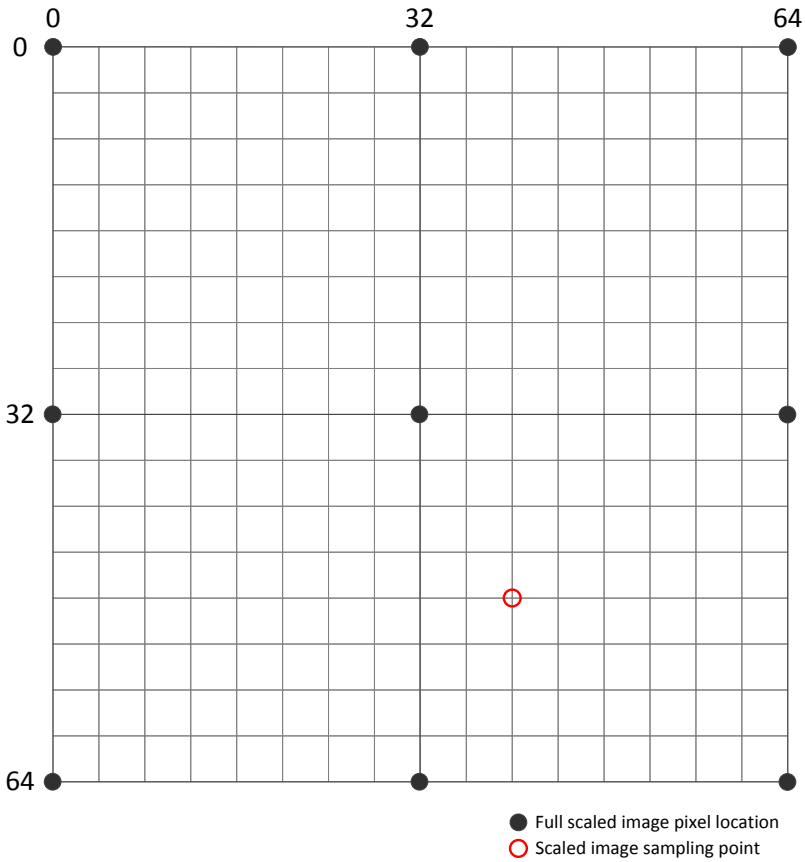


Figure 10 Example of scale down

Table 8 Register Table - Scale

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
scale_x	C	9F	[7:0]	0x20	RW	aev	Horizontal scale factor
scale_y	C	A0	[7:0]	0x20	RW	aev	Vertical scale factor
scale_th_h	C	A1	[2:0]	0x00	RW	aev	Scale buffer TH
scale_th_l	C	A2	[7:0]	0x0A	RW	aev	

ITU-R BT656

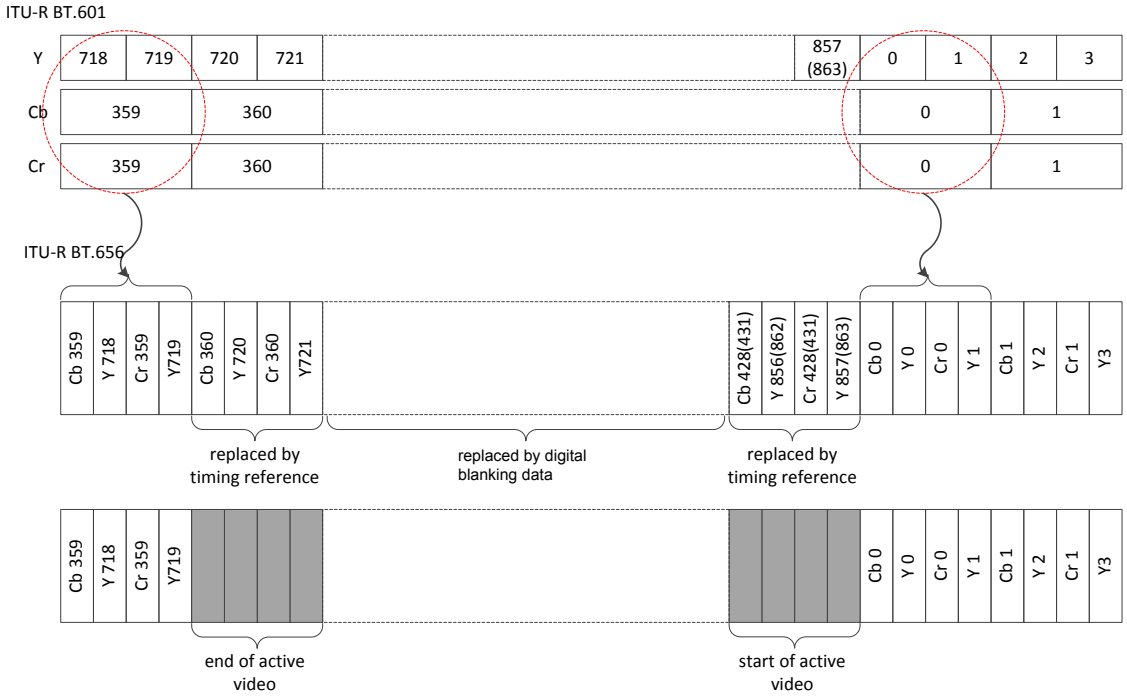


Figure 11 Timing diagram for ITU-R BT656

Figure 11 shows ITU-R BT601 and ITU-R BT656 timing diagram. Sampling clocks of ITU-R BT601 and ITU-R BT656 are 13.5MHz and 27MHz respectively. ITU-R BT656 format is generated from ITU-R BT601 format data by serialization and timing reference. Timing reference indicates Start or End of video. It includes field, vsync and hsync information. PC7080D provides two kinds of active video sizes with BT656 format such as 720x480i and 720x576i ('i' stands for interlaced scan). The horizontal size is stretched to 720 pixels. 720x480i size BT656 supports for 525-line video, and 720x576i size BT656 for 625-line video. Horizontal timing of 720x480i and 720x576i size BT656 is shown in Figure 11 and vertical Timing diagram is shown in Figure 12,Figure 13.

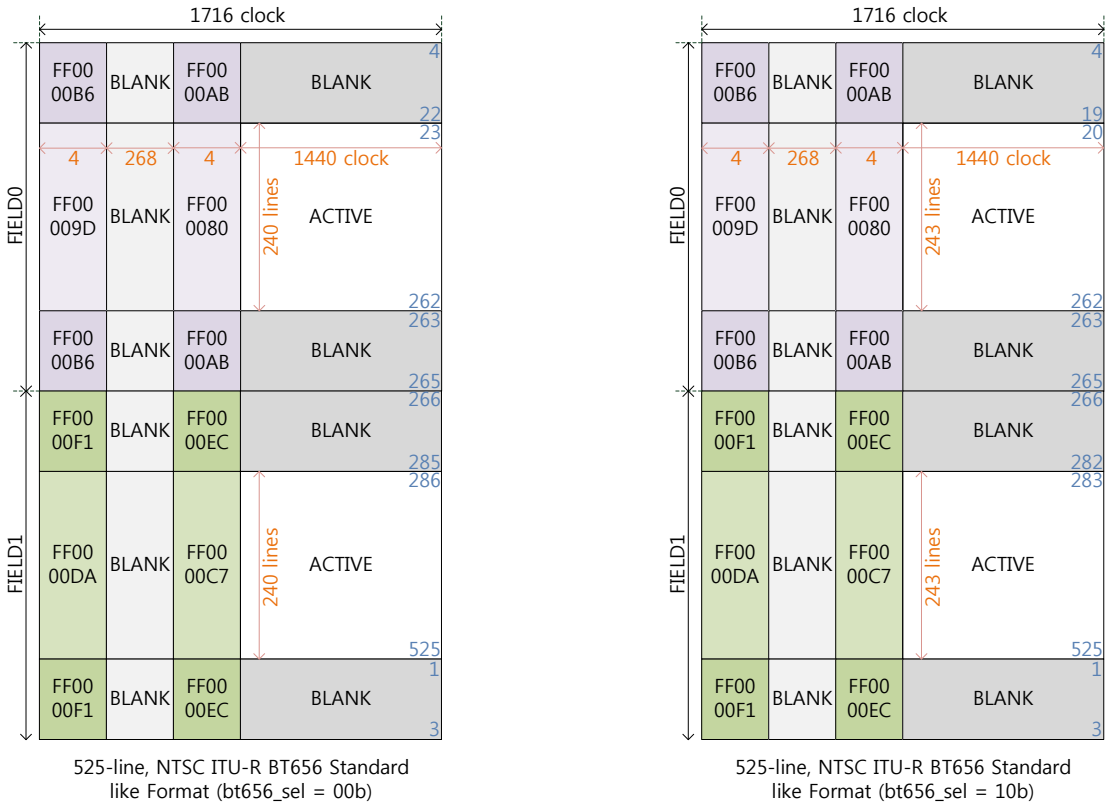


Figure 12 TRS and vertical timing

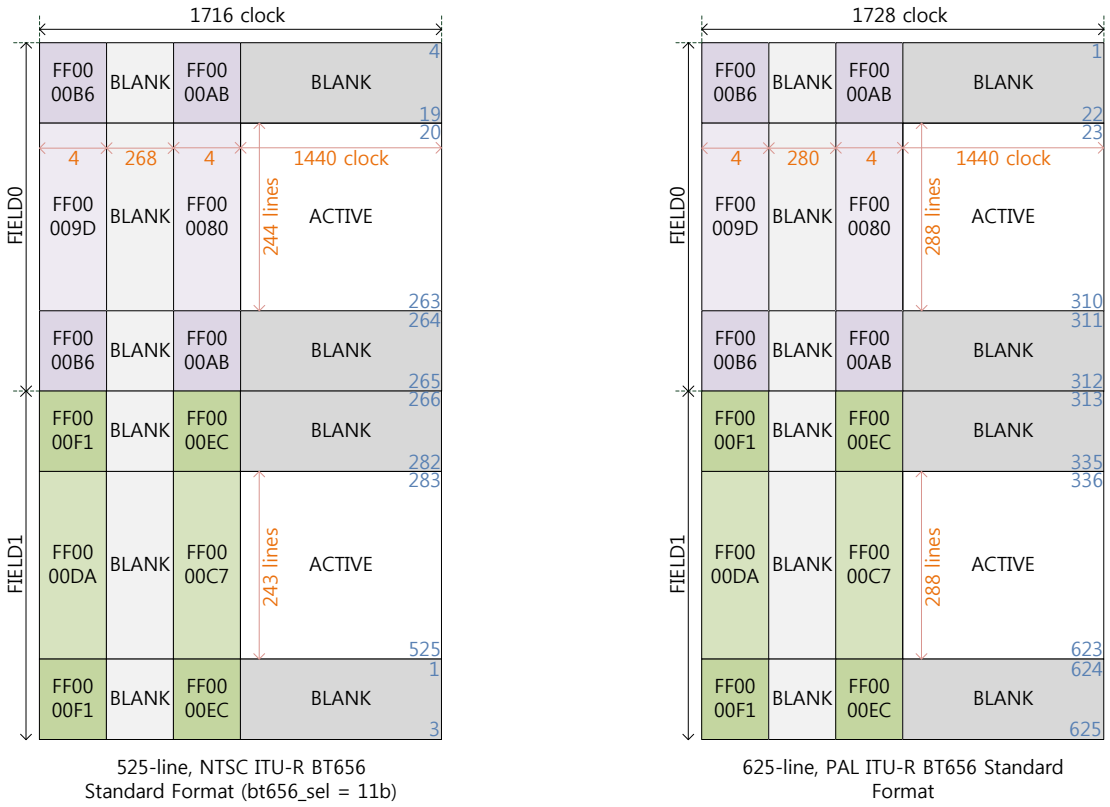


Figure 13 TRS and vertical timing

Table 9 Register Table - ITU-R BT656

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
bt656_sel	G	10	[7:6]	2'b10	RW		BT656 mode selection bits @ NTSC mode 2'b00 : even field output(720x240), odd filed output (720x240) 2'b10 : even field output(720x243), odd filed output (720x243) 2'b11 : even field output(720x244), odd filed output (720x243)
bt656_stdeff	G	10	[5]	1'b0	RW		Effective data slection @ BT656 standard mode 1'b0 : black 1'b1: effectieve data
reg_sel_Hscale	G	10	[4]	1'b1	RW		x scale factor selection 1'b0: old version 1'b1 : new version
x_delay_sel	G	13	[3:0]	0x02	RW		Zoom x delay selection
winy_sel	G	10	[3:2]	2'b00	RW		Digital output vertical size selection bits@ NTSC mode 2'b00 : even field digital output (720x240), odd field digital output (720x240) 2'b01 : even field digital output (720x243), odd field digital output (720x243)

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							2'b10 : even field digital output (720x244), odd field digital output (720x243) 2'b11 : even field digital output (720x244), odd field digital output (720x244)
even_drop	G	10	[1]	1'b0	RW		Digital CCIR656 output even field drop enable 1'b0 : disable 1'b1 : enable (even field drop)
odd_drop	G	10	[0]	1'b0	RW		Digital CCIR656 output odd field drop enable 1'b0 : disable 1'b1 : enable (odd field drop)
sync_blankEAV_f0	G	04	[7:0]	0xB6	RW		Blank EAV for field0 of CCIR656 data or blank EAV for frame data
sync_blankSAV_f0	G	05	[7:0]	0xAB	RW		Blank SAV for field0 of CCIR656 data or blank SAV for frame data
sync_activeEAV_f0	G	06	[7:0]	0x9D	RW		Active EAV for field0 of CCIR656 data or active EAV for frame data
sync_activeSAV_f0	G	07	[7:0]	0x80	RW		Active SAV for field0 of CCIR656 data or active SAV for frame data
sync_blankEAV_f1	G	08	[7:0]	0xF1	RW		Blank EAV for field1 of CCIR656 data or blank EAV for frame data
sync_blankSAV_f1	G	09	[7:0]	0xEC	RW		Blank SAV for field1 of CCIR656 data or blank SAV for frame data
sync_activeEAV_f1	G	0A	[7:0]	0xDA	RW		Active EAV for field1 of CCIR656 data or active EAV for frame data
sync_activeSAV_f1	G	0B	[7:0]	0xC7	RW		Active SAV for field1 of CCIR656 data or active SAV for frame data
sync_CCIR_FF	G	0C	[7:0]	0xFF	RW		CCIR656 blank data format
sync_CCIR_00	G	0D	[7:0]	0x00	RW		
sync_CCIR_80	G	0E	[7:0]	0x80	RW		
sync_CCIR_10	G	0F	[7:0]	0x10	RW		
d9_pad_en	A	2E	[7]	1'b0	RW		D9 data pad enable
d8_pad_en	A	2E	[6]	1'b0	RW		D8 data pad enable
d7_pad_en	A	2E	[5]	1'b0	RW		D7 data pad enable
d6_pad_en	A	2E	[4]	1'b0	RW		D6 data pad enable
d5_pad_en	A	2E	[3]	1'b0	RW		D5 data pad enable
d4_pad_en	A	2E	[2]	1'b0	RW		D4 data pad enable
d3_pad_en	A	2E	[1]	1'b0	RW		D3 data pad enable
d2_pad_en	A	2E	[0]	1'b0	RW		D2 data pad enable
d1_pad_en	A	29	[3]	1'b0	RW		D1 data pad enable
d0_pad_en	A	29	[2]	1'b0	RW		D0 data pad enable

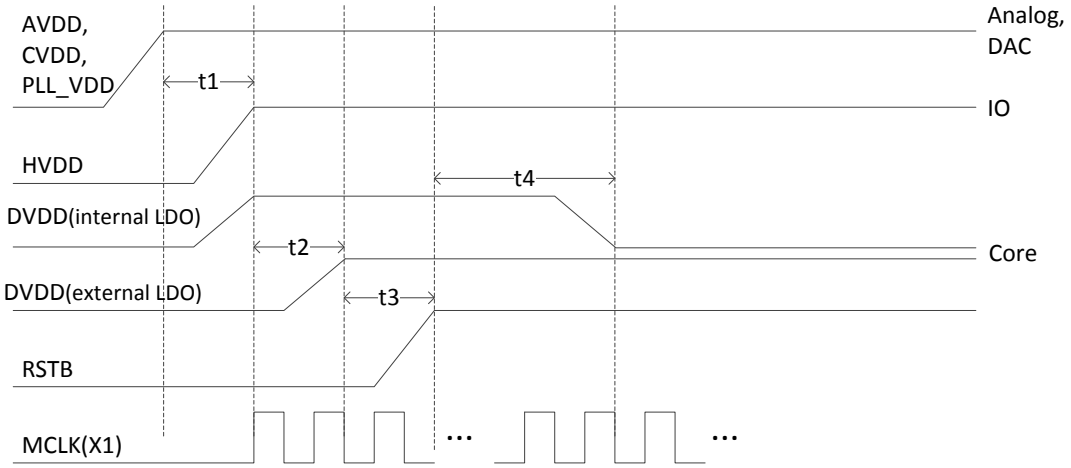
Recommended Power Sequence

Table 10 Recommended power on/down sequence

Symbol	Descriptions	Min	Typ	Max	Unit
t1	From AVDD,CVDD rising to HVDD rising	10	-	-	ms
t2 [a]	From HVDD rising to DVDD(external LDO) rising	10	-	-	ms
t3	Sensor reset time	8	-	-	MCLK
t4 [b]	From RSTB risng to internal LDO power down	10	-	-	ms
t5	From AVDD,CVDD falling to HVDD falling	10	-	-	ms
t6 [c]	From HVDD falling to DVDD(external LDO) falling	10	-	-	ms

[a]You should consider t2 when using external LDO.
[b]You should consider internal LDO power down when using external LDO. You can power down internal LDO though b_pd15, r_pd15 registers.
[c]You should consider t6 when using external LDO.

Power-on Sequence(using external LDO)



Power-on Sequence(using internal LDO)

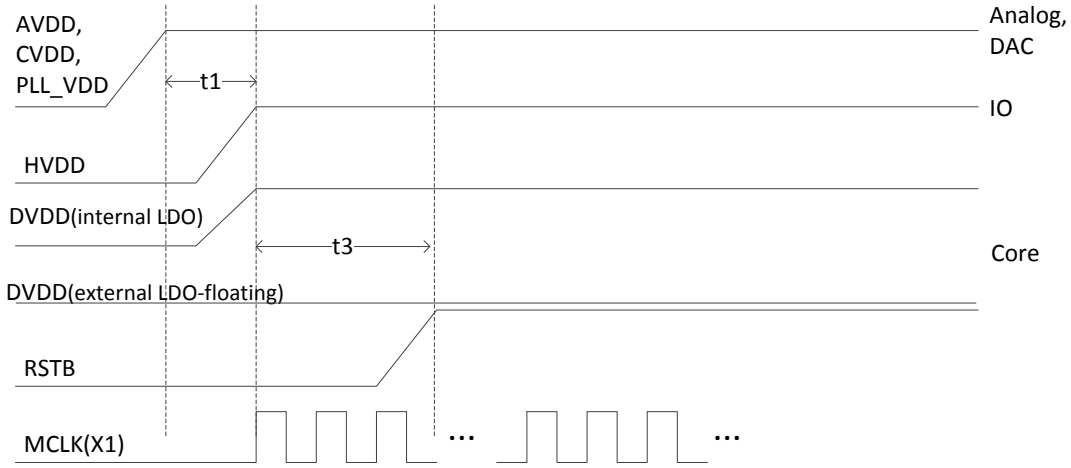


Figure 14 Recommended power on sequence

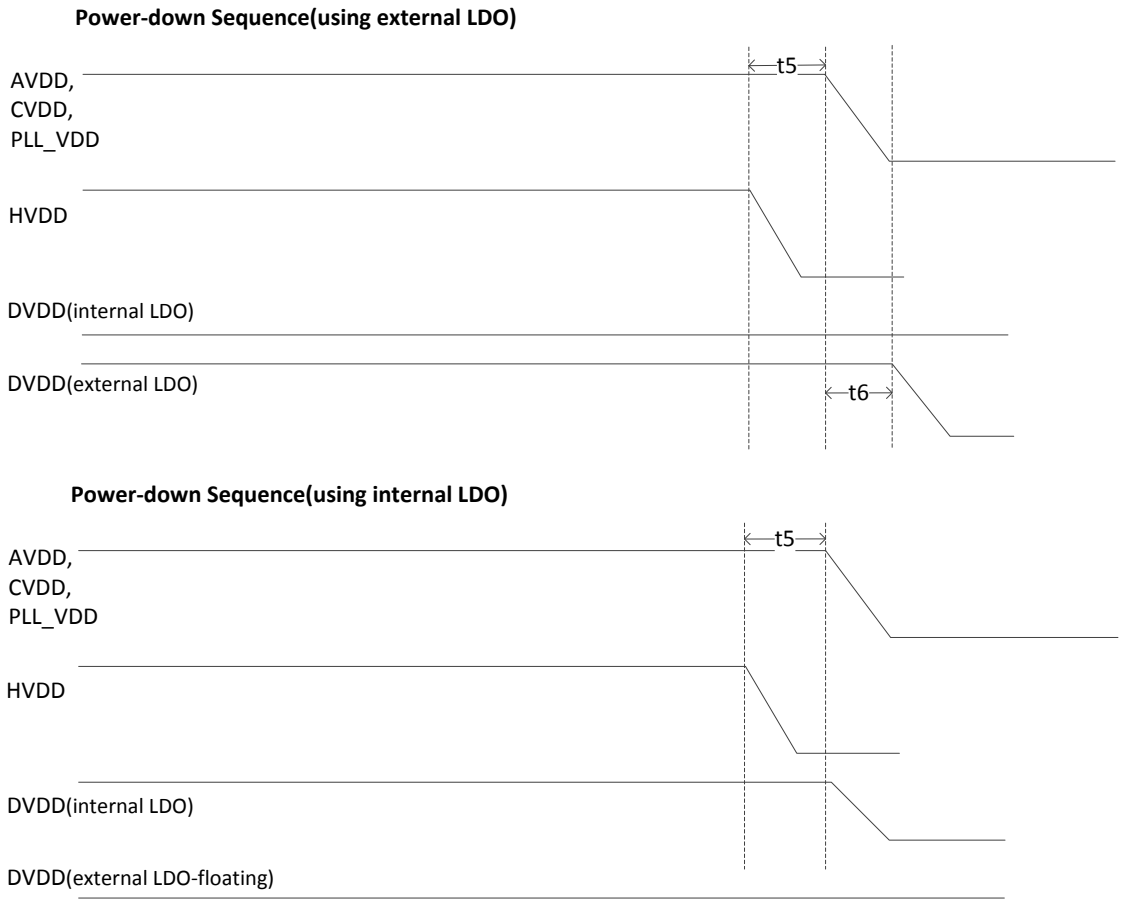


Figure 15 Recommended power down sequence

Clock

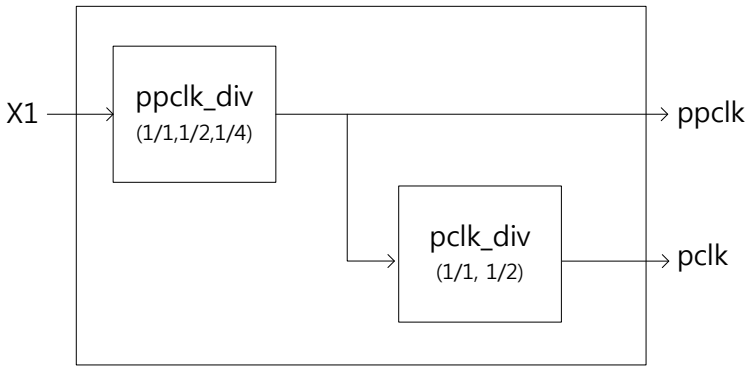


Figure 16 Clock divider

- X1 : PAD input clock
- pclk : internal pixel clock
- ppclk : internal double rate pixel clock for progressive parallel output

Clock Divider

Table 11 Clock Divider

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pclk_div	A	25	[5]	1'b1	RW	aev	pclk divider 1'b'0 : x1/2 1'b1 : x1
ppclk_div	A	25	[1:0]	2'b00	RW	aev	ppclk divider 2'b00 or 2'b11 : x1 2'b01 : x1/2 2'b10 : x1/4

System Reset

The PC7080D has two methods to reset: hard reset and soft reset. Hard reset signal from RSTB PAD must remain low (active low) for at least 8 master clocks to correctly reset the sensor. All registers are set to their default values after reset.

Figure 17 shows device soft reset by setting softreset register through I2C interface. When softreset register is set, async_rstb (asynchronous reset) and sync_rstb signal changes from 1 to 0 and holds for 1 clock of SCL. Afterward, async_rstb is set back to 1 while sync_rstb holds 0 for another 16 clocks of pclk for stable reset operation. Therefore, PC7080D requires at least 1 clock of SCL and 16 clocks of pclk to perform a soft reset operation.

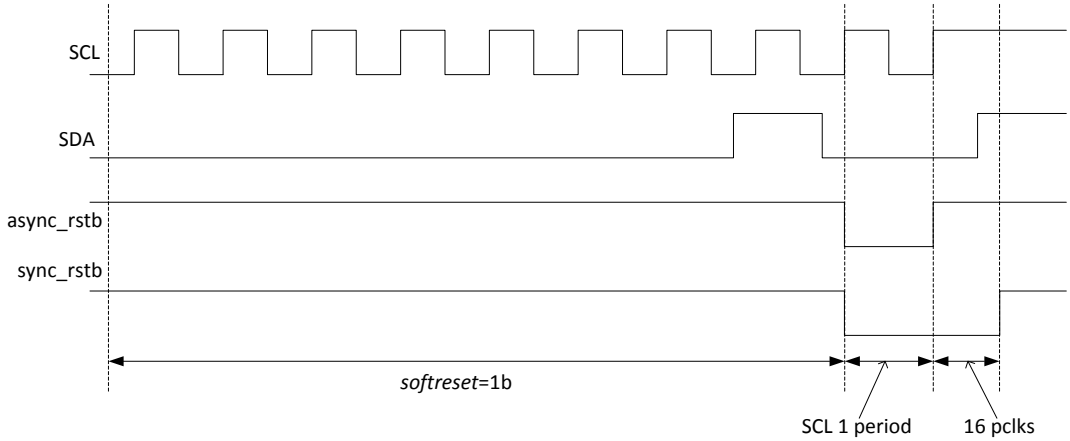


Figure 17 Soft reset

Table 12 Register Table - Soft reset

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
softreset	A	24	[0]	0x00	RW		soft reset

Initialization

Initialization Flow

When power is applied to the chip, an initialization operation is performed. The initialization operation performs different operations depending on the master mode. If master mode is off, initialization is not performed. If master mode is on, start from internal ROM setting. After completing the setting of the internal ROM, the I2C bus must be idle state before entering the next initialization phase.

After the internal ROM setting, EEPROM detection is performed. If the ROM does not exist, the process jumps to the next step. Initialization flow is shown in Figure 18.

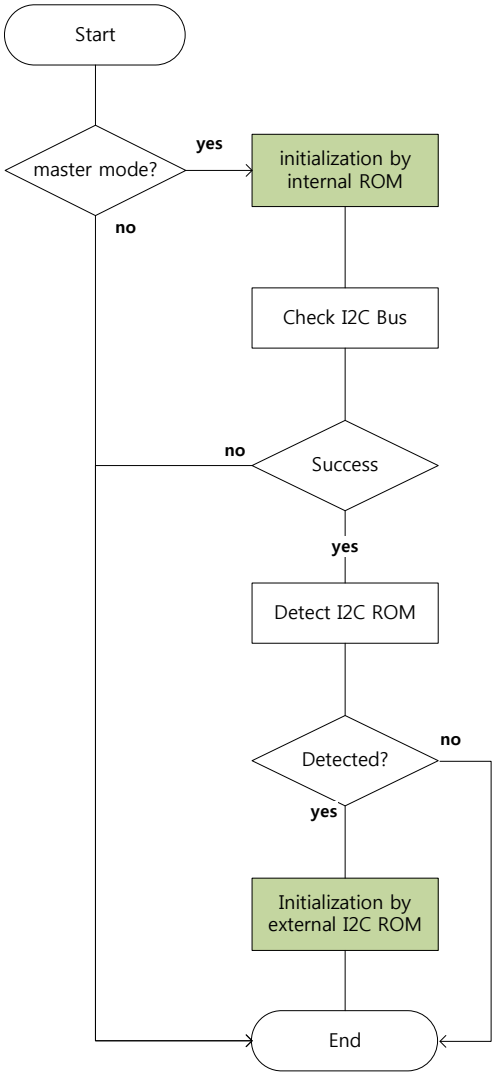


Figure 18 Initialization Flow

PC7080D has a single I2C master and shares the SCL / SDA line with the I2C slave. External I2C master can access PC7080D after Figure 18 process is completed. The initialization time depends on the conditions of master mode and external ROM.

Required Time of Initialization

- Master mode on
  a. In case that external ROM does not exist
     The time to end the internal ROM setting is 2.6 ms.
  b. In case that EEPROM does exist(SCL @ about 300 KHz)
     Cycle time for register write is 200 us
  c. In master mode, the initialization time is calculated as a + b.
- Master mode off
  a. Setting time is 0 s.
  b. The initialization time is not required when master mode is off.

sif_state indicates the status of SIF (serial interface control block), the initialization block of master mode (vsync = *1*). The user can make I2C communication from the outside after sif_state = 03h.

- sif_state register(when master mode is on)
  a. 00h, 01h, 02h -> PC7080D is being initialized.
  b. 03h -> initialization is done.

Table 13 Register Table - sif_state

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
sif_state	F	D3	[7:0]		RO		SIF state monitor

Wire-strapping

Wire-strapping is a function that can control the setting mode with PAD input. The setting mode is determined by VSYNC, HSYNC, D9 to D0 PAD. Check the PAD input voltage during chip initialization and perform setting according to setting mode. It is shown in setting mode Table 14 according to PAD input voltage.

Table 14 setting mode according to wire-strapping

		vsync	hsync	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TV Mode	(M)NTSC	-	-	-	-	-	-	-	L	L	L	-	-
	NTSC-J	-	-	-	-	-	-	-	L	L	H	-	-
	(M)PAL	-	-	-	-	-	-	-	L	H	L	-	-
	(Nc)PAL	-	-	-	-	-	-	-	L	H	H	-	-
	(B,D,G,H,I) PAL	-	-	-	-	-	-	-	H	L	L	-	-
	(N)PAL	-	-	-	-	-	-	-	H	L	H	-	-
	NTSC-4.43	-	-	-	-	-	-	-	H	H	L	-	-
Flicker	No Flicker cancel	-	-	-	-	-	L	L	-	-	-	-	-
	Manual-A	-	-	-	-	-	L	H	-	-	-	-	-
	Manual-B	-	-	-	-	-	H	L	-	-	-	-	-
	Auto Flicker cancel	-	-	-	-	-	H	H	-	-	-	-	-
Mirror	NO MIRROR	-	-	-	-	-	-	-	-	-	-	H	L
	MIRROR-V	-	-	-	-	-	-	-	-	-	-	L	L
	MIRROR-H	-	-	-	-	-	-	-	-	-	-	H	H
	MIRROR-VH	-	-	-	-	-	-	-	-	-	-	L	H

		vsync	hsync	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Max Gain selection	maxgain32	-	-	-	L	L	-	-	-	-	-	-	-
	maxgain48	-	-	-	L	H	-	-	-	-	-	-	-
	maxgain64	-	-	-	H	L	-	-	-	-	-	-	-
	maxgain80	-	-	-	H	H	-	-	-	-	-	-	-
OSD Enable	Enable	-	-	H	-	-	-	-	-	-	-	-	-
	Disable	-	-	L	-	-	-	-	-	-	-	-	-
Master Mode	ON	H	-	-	-	-	-	-	-	-	-	-	-
	OFF	L	-	-	-	-	-	-	-	-	-	-	-
General[2]	1'b1	-	H	-	-	-	-	-	-	-	-	-	-
	1'b0	-	L	-	-	-	-	-	-	-	-	-	-

When using general strap, max. gain strap can be used as general [1:0].

strap_smp is register to store strap inforation. when strap_smp =*0*, latch stores strap information.

Table 15 Register Table - strap_control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
strap_smp	A	2D	[0]	1'b0	RW		latch stores strap information when strap_smp=*0*

Real-time Strap

strap_control[7:0] matches Table 16. When the bit is set to *0*, the setting is applied in real time according to the setting mode.

Table 16 Register Table - strap_control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
strap_control	A	30	[7:0]	0xFF	RW		general mode real-time setting control [7] : master mode [6] : general mode [5] : OSD mode [4] : Max gain mode[1] [3] : Max gain mode[0] [2] : Flicker mode [1] : Mirror mode [0] : Video mode

Internal ROM

PC7080D reads the data according to the PAD input from the internal ROM and performs setting.

Register settings according to mirror mode are shown in Table 17.

Table 17 Mirror mode

[D1,D0]	2'b00	2'b01	2'b10	2'b11
Register name	**V mirror**	**HV mirror**	**NO mirror**	**H mirror**
mirror	02	03	00	01

Register settings according to chip mode selection are shown in Table 18.

Table 18 Chip Mode Selection

[D4,D3,D2]	3'b000	3'b001	3'b010	3'b011	3'b100	3'b101	3'b110
Register name	**(M)NTSC**	**NTSC-J**	**(M)PAL**	**(Nc)PAL**	**(OTHER)PALs**	**(N)PAL**	**NTSC-4.43**
pad_control7	01	01	01	01	01	01	01
chip_mode	00	00	00	01	01	01	00
framewidth_h	03	03	03	04	04	04	03
framewidth_l	59	59	59	0D	0D	0D	59
fd_a_step_h	03	03	03	04	04	04	03
fd_a_step_l	E8	E8	E8	BD	BD	BD	E8
fd_b_step_l	40	40	40	F0	F0	F0	40
fd_period_a_h	01	01	01	00	00	00	01
fd_period_a_m	03	03	03	D8	D8	D8	03
fd_period_a_l	80	80	80	F8	F8	F8	80
fd_period_b_m	3B	3B	3B	01	01	01	3B
fd_period_b_l	0D	0D	0D	00	00	00	0D
fd_period_c_h	06	06	06	05	05	05	06
fd_period_c_m	27	27	27	15	15	15	27
fd_fheight_a_l	0C	0C	0C	07	07	07	0C
fd_fheight_b_l	0C	0C	0C	07	07	07	0C
vsyncstoprow_f0_l	06	06	06	36	36	36	06
vsyncstartrow_f1_l	1E	1E	1E	50	50	50	1E
vsyncstoprow_f1_l	0D	0D	0D	6F	6F	6F	0D
osd_efld_s_h	00	00	00	00	00	00	00
osd_efld_s_l	01	01	01	01	01	01	01
osd_ofld_s_h	01	01	01	01	01	01	01
osd_ofld_s_l	0A	0A	0A	39	39	39	0A
expfrmh_h	02	02	02	02	02	02	02
expfrmh_l	07	07	07	02	02	02	07
midfrmheight_h	02	02	02	02	02	02	02
midfrmheight_l	07	07	07	02	02	02	07

[D4,D3,D2]	3'b000	3'b001	3'b010	3'b011	3'b100	3'b101	3'b110
Register name	**(M)NTSC**	**NTSC-J**	**(M)PAL**	**(Nc)PAL**	**(OTHER)PALs**	**(N)PAL**	**NTSC-4.43**
maxfrmheight_h	02	02	02	02	02	02	02
maxfrmheight_l	07	07	07	02	02	02	07
enc_mode	00	00	03	02	01	01	00
enc_blankL	F0	F0	F0	FC	FC	F0	F0
enc_pedestal	2A	00	2A	00	00	2A	2A
enc_burst	80	82	8C	8A	9C	9A	82
enc_Ygain	82	8D	82	89	89	82	82
enc_Ugain	6F	78	6F	75	75	6F	6F
enc_Vgain	9C	A9	9C	A6	A6	9C	9C
enc_Crange_L	48	62	48	5B	5B	48	48
enc_chroma_max_L	CD	DF	CD	D7	D7	CD	CD
enc_chroma_min_L	6D	35	6D	45	45	6D	6D
enc_scfreq	00	00	03	02	01	01	01
hsync_p_toffset	12	12	12	00	00	06	12
burst_duration	00	00	89	89	00	00	8D
l_blank_start	0C	0C	0D	12	15	10	0C
l_blank_stop	02	02	03	0B	0B	00	02
sync_rising	04	04	04	08	08	07	04
burst_toffset	88	88	08	8A	96	96	88
encdat_rising	04	04	04	07	08	07	04
setup_w	07	00	07	00	00	07	07

Register settings according to flicker mode are shown in Table 19.

Table 19 Flicker mode

[D6,D5]	2'b00	2'b01	2'b10	2'b11
Register name	**Normal(off)**	**manual A**	**manual B**	**auto fd**
flicker_control1	00	08	04	40

Register settings according to max gain selection mode are shown in Table 20.

Table 20 Max Gain Selection

{D8,D7}	2'b00	2'b01	2'b10	2'b11
Register name	**maxgain32**	**maxgain48**	**maxgain64**	**maxgain80**
minexp_h	00	00	00	00
minexp_m	01	01	01	01
minexp_l	00	00	00	00
midexp_t	00	01	01	02
midexp_h	E0	51	C1	32
midexp_m	E0	50	C0	30

{D8,D7}	2'b00	2'b01	2'b10	2'b11
Register name	**maxgain32**	**maxgain48**	**maxgain64**	**maxgain80**
maxexp_t	00	01	01	02
maxexp_h	E0	51	C1	32
maxexp_m	E0	50	C0	30

External ROM

External ROM Structure

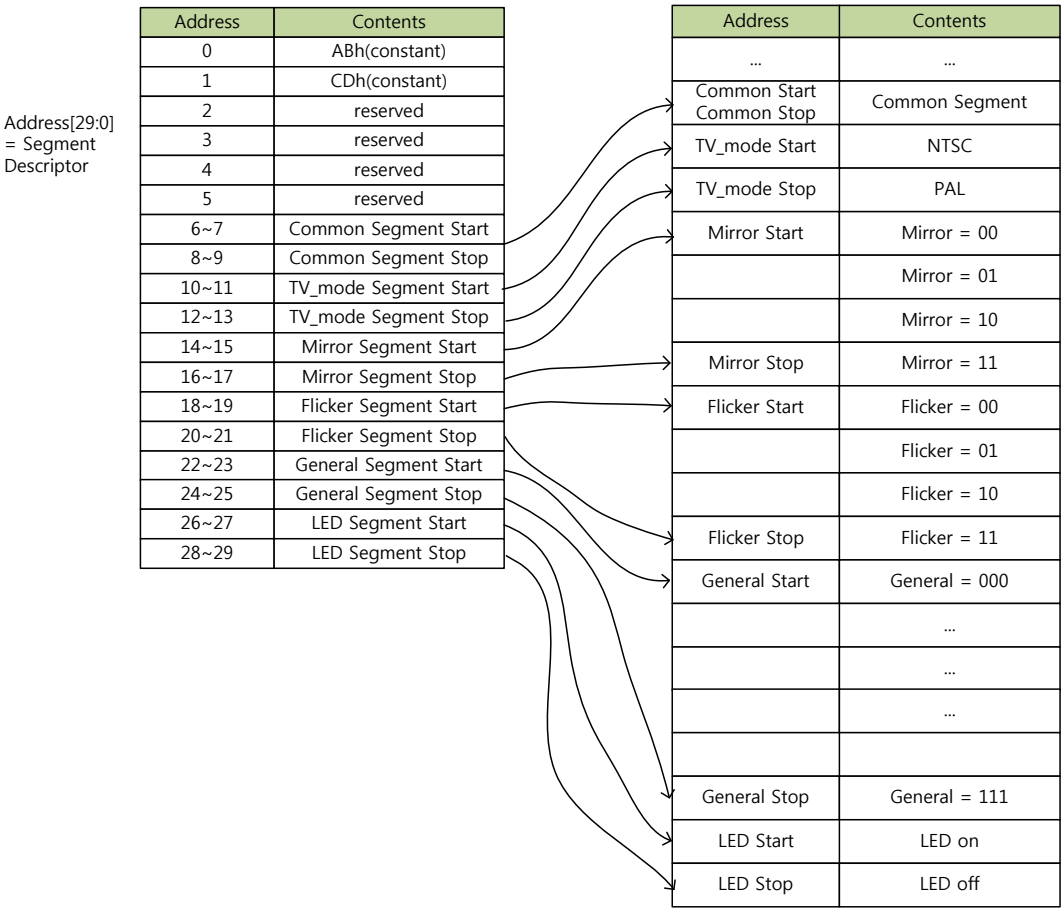


Figure 19 External ROM structure

Figure 19 shows external ROM structure. The user can use the external ROM to apply settings differently depending on the strap input or the external environment. The external ROM consists of the following segments.

Common segment : Regardless of the strap, it is set in the external ROM initialization process.
TV mode segment : Depending on the tv_mode strap, the settings are applied differently.
Mirror segment : Depending on the mirror strap, the settings are applied differently.
Flicker segment : Depending on the flicker strap, the settings are applied differently.
General segment : Depending on the general strap(General[2] strap, max. gain strap), the settings are applied differently
LED segment : Depending on the LED on/off, the settings are applied differently.

EEPROM

EEPROM can be used as External ROM. The SCL and SDA lines are pulled up to HVDD by a off-chip resistor of $2[k\Omega]$.

I2C Baud Rate

I2C baud rate is fixed to 300 Kbps

External Communication Specification

I2C Communication

I2C communication is a serial interface which utilizes SCL/SDA lines to transfer 8-bit data per transaction. The SCL and SDA lines are pulled up to HVDD by a off-chip resistor of $2[k\Omega]$. PC7080D includes only I2C slave function and requires external master to access the internal registers. Each transaction requires 8-bit data and 1-bit acknowledge bit. There are four types of operations supported in PC7080D's I2C operation: single write, multiple write, single read, multiple read.

In single write operation, after the start state, 7-bit slave address and write bit are transmitted from master device to PC7080D. If correct slave address is detected, PC7080D reply with acknowledge bit as confirmation of valid address. Then master device transmits register address and waits for acknowledge bit from PC7080D. Lastly, 8-bit data is sent to PC7080D and waits for acknowledge bit again. Once acknowledge bit is recieved, master device announces the stop state to terminate I2C communication.

Multiple write operation works exactly the same until stop state procedure. Instead of announcing the stop state, master device transmits more data. If PC7080D detects multiple write operation, any data stream following the first 8-bit is stored in subsequent register addresses of the first register address.

Read operation consists of two sub-procedure: address write and data read. The procedure is performed exactly same as register address write procedure from single write operation. Afterward, master device announces repeated start and transmit slave address with read bit. When PC7080D detects read operation, PC7080D sends acknowledge bit to master device, then reads register corresponding to register address. PC7080D transmits read data to master device and waits for master device to respond. If master device responds with no acknowledge bit followed by stop state, read operation is terminated. On the other hand, if master device responds with acknowledge, PC7080D reads the subsequent register and transmits again. As long as master device replies with acknowledge bit after each data transaction, PC7080D will continuously read the subsequent register and transmit until no acknolwedge bit followed by stop state is presented. If only one 8-bit data is read, the procedure is single read operation. whereas, reading more than 8-bit data is multiple read operation. Figure 20 shows read/ write operation of I2C communication.

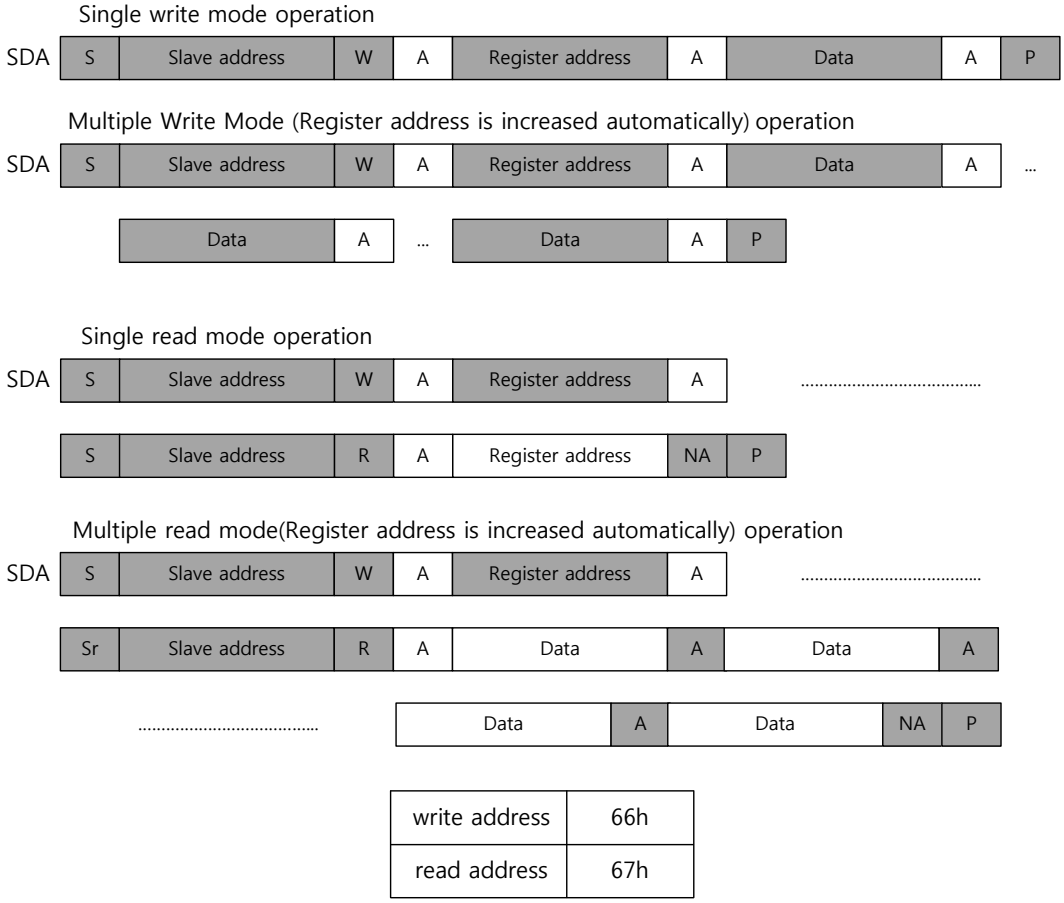


Figure 20 I2C functional description

Register Update Timing

The registers have three types of update timing: "aev" and "autov" update, regular update. The registers of "aev" and "autov" type update new values from I2C write operation at the last line of the frame. Whereas, registers with regular update type apply new values immediately after I2C write operation. However, By changing updatecontrol register value, register updates for "aev" and "autov" type can either be disabled or be updated immediately. Table 21 shows registers relevant to I2C update control.

Table 21 I2C update timing control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
updatecontrol[3:0]	A	23	[7:4]	4'b0101	RW		Control i2c register update update_autov <= updatecontrol[3] or (autov_update and updatecontrol[2]) update_aev <= updatecontrol[1] or (aev_update and updatecontrol[0])

Flicker Cancelation

PC7080D includes flicker cancelation feature. Generally, operating frequency of light source is either 60 Hz or 50 Hz. Therefore, PC7080D's flicker cancelation feature is pre-configured states with 60 Hz light source frequency as state A and 50 Hz light source frequency as state B.
Three different flicker cancelation mode is available in PC7080D: auto mode, manual A mode, and manual B mode.

- Auto mode(fd_en = 1'b1, manual_A = 1'b0, manual_B = 1'b0)
  When flicker in image is detected, current state is toggled. In other word, current state is switched to the other state.

- manual_A mode(fd_en = 1'b0, manual_A = 1'b1, manual_B = 1'b0)
  Manual A mode puts flicker cancelation state in state A regardless of flicker. Factory setting of PC7080D is configured for 60 Hz light source.

- manual_B mode(fd_en = 1'b0, manual_A = 1'b0, manual_B = 1'b1)
  Manual B mode puts flicker cancelation state in state B regardless of flicker. Factory setting of PC7080D is configured for 50 Hz light source.

Table 22 shows registers relevant to flicker cancelation.

Table 22 Register Table - Flicker cancelation

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
fd_en	A	4F	[6]	1'b0	RW		auto flicker detection enable
manual_A	A	4F	[3]	1'b0	RW		Manual flicker cancellation state control
manual_B	A	4F	[2]	1'b0	RW		

LED Control

LED control functions include IRLED control with Cds, LED blinking.

The IRLED control function uses infrared light by operating the external IRLED in low light conditions where there is not enough visible light. real_led_data means the amount of light absorbed by Cds. IRLED control function has auto mode and manual mode.

- ledctl en = 1'b1 (auto mode)
  When real_led_data is less than led_lvth1, 1'b1 (LED on) signal is output. When real_led_data is greater than led_lvth2, it outputs 1'b0 (LED off) signal. The led_frame is a value that delays the IRLED on / off transition. The unit of led_frame is frame. (refet to Figure 21)

- ledctl en = 1'b0 (manual mode)
  The ledctl manual controls the IRLED control output. When ledctl manual is set to 1'b1, it outputs LED on signal, If ledctl manual is set to 1'b0, it outputs LED off signal.

Bwled en is a function that changes the screen to black and white in LED on operation.

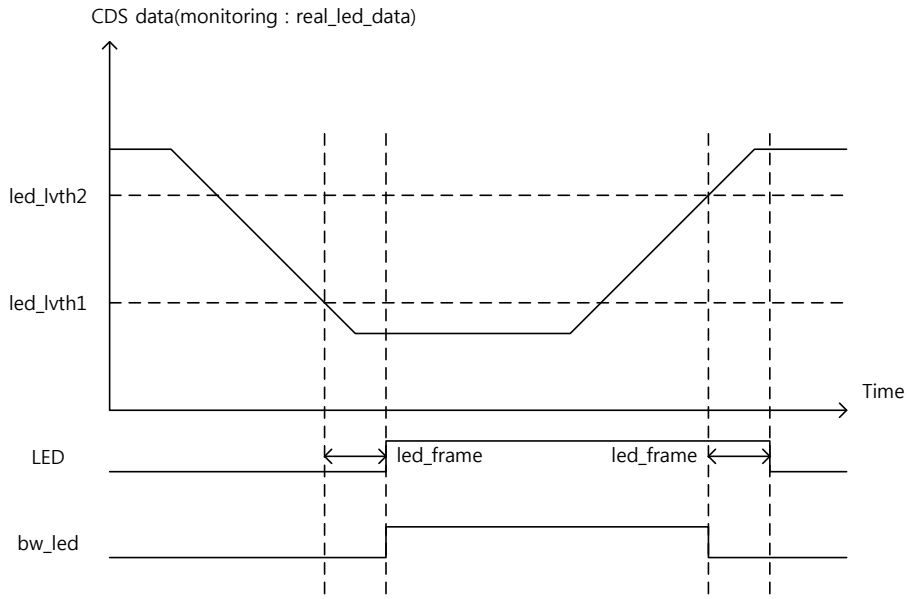


Figure 21 LED control with CdS

The LED blink function is a function that periodically repeats the LED on/off status by setting the LED on time and the LED off time. LED blinking features LED blinking, fixed LED on / off.

- ledblnk en = 1'b1 (LED blinking)
  Led_blink_frame [7: 4] controls the LED on time, Led_blink_frame [3: 0] indicates the LED off time. (refet to Figure 22)

- ledblnk en = 1'b0 (fixed LED on/off)
  The output is controlled by ledblnk manual. If ledblnk manual is 1'b1, LED on signal is output. If ledblnk manual is 1'b0, LED is off signal.

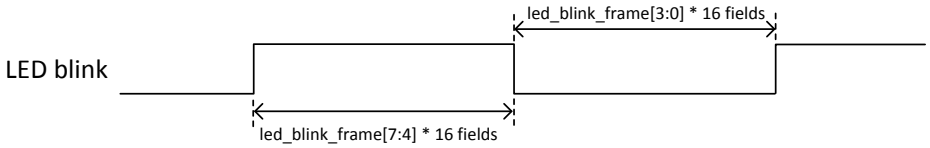


Figure 22 LED blink signal waveform

The blinking interval differs depending on the TV mode. The blinking interval for each TV mode is as follows:

- NTSC mode
  The range for setting the blinking interval is 0.27 to 4.00 [sec]. increments unit of blinking interval is 0.27 [sec].

- PAL mode
  The range for setting the blinking interval is 0.32 to 4.80 [sec]. increments unit of blinking interval is 0.32 [sec].

PC7080D can output IRLED control signal and LED blink signal at the same time.

HSYNC, IRLED_CTRL pad output depends on hsync_pad_selection, ledblnk selection, and ledctl selection settings. (refet to Figure 23)

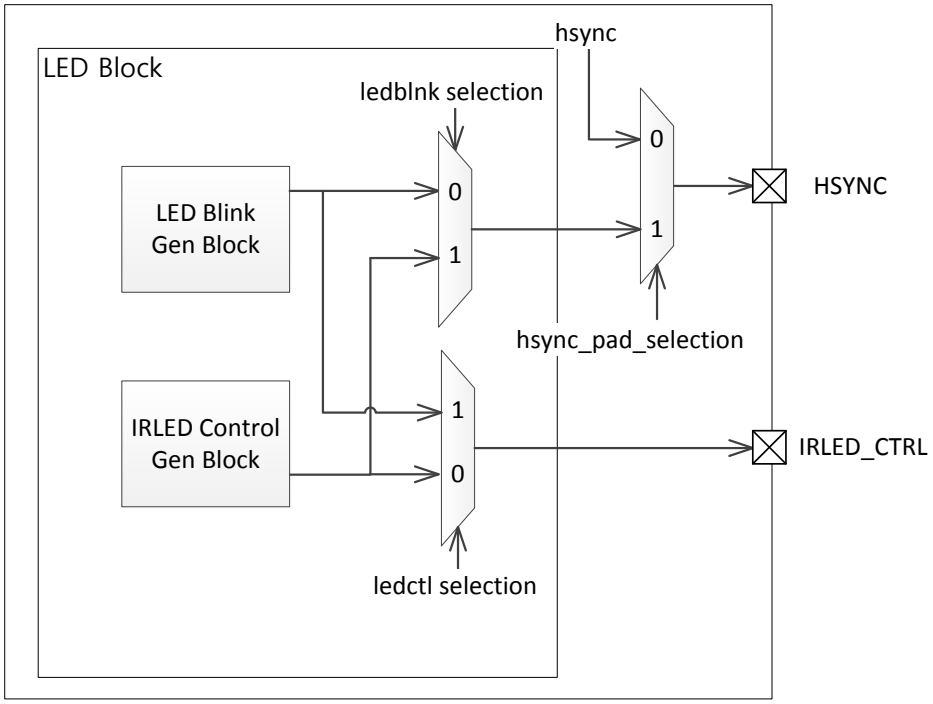


Figure 23 LED blink signal output path

Table 23 Register Table - LED control with CdS

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
led_lvth1	A	7C	[7:0]	0x00	RW		LED control level threshold 1
led_lvth2	A	7D	[7:0]	0x00	RW		LED control level threshold 2
led_frame	A	7E	[7:0]	0x80	RW		LED control wait period in frame unit
ledctrl_en	A	2A	[7]	1'b0	RW		LED pad control 1'b0: disable 1'b1: enable
ledctrl_pad_drv[1:0]	A	2A	[6:5]	2'b00	RW		LED pad drivability
ledctrl_pull_en	A	3F	[5]	1'b1	RW		LED PAD pull-up/pull-down enable 0b : LED PAD is "HIZ" @ ledctrl_en = 0 1b: LED PAD is *L* or *H* (refer to ledctrl_pull_sel)
ledctrl_pull_sel	A	3F	[4]	1'b0	RW		LED PAD pull-up/pull-down selsection 0b: LED PAD is "L" @ ledctrl_en = 1 1b: LED PAD is "H" @ ledctrl_en = 1
ledctl en	A	7B	[7]	1'b0	RW		LED control enable 1'b0: disable 1'b1: enable
ledctl manual	A	7B	[6]	1'b0	RW		LED manual control 1'b0: disable 1'b1: enable @ ledctl en = 1'b0
ledctl polarity	A	7B	[5]	1'b0	RW		LED output polarity inversion 1'b0: disable 1'b1: enable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ledctl selection	A	7B	[3]	1'b0	RW		Output signal selection to LED_CTRL PAD 1'b0: LED control signal 1'b1: LED blink signal
bwled en	A	7B	[4]	1'b0	RW		LED black and white enable
exrom_set_en	A	7B	[0]	1'b0	RW		enable setting from external rom @ led on/off 0b: disable 1b: enable
ledblnk en	A	7A	[7]	1'b0	RW		LED blink enable 1'b0: disable 1'b1: enable
ledblnk manual	A	7A	[6]	1'b0	RW		LED blink manual control 1'b0: disable 1'b1: enable @ ledblnk_en = 1'b0
ledblnk polarity	A	7A	[5]	1'b0	RW		LED blink polarity inversion 1'b0: disable 1'b1: enable
ledblnk selection	A	7A	[4]	1'b0	RW		Output signal selection to HSYNC PAD 1'b0: LED blink signal 1'b1: LED control signal
led_blink_frame	A	7F	[7:0]	0x33	RW		LED blink frame
hsync_pad_selection	A	29	[1]	1'b0	RW		HSYNC PAD selection 1'b0: hsync 1'b1: LED signal
led_dsel[1:0]	B	15	[1:0]	2'b01	RW		CdS data selection
inv_led	B	16	[2]	1'b0	RW		CdS data inverting enable
led_delay[3:0]	B	1D	[3:0]	4'b0011	RW		CdS data timing selection
real_led_data	B	D7	[7:0]		RO		Current CdS data

Exposure Control

Integration Time

PC7080D employs rolling shutter [1] for capturing image. Reset operation initializes ROBP and active pixel region in sequence row by row. Readout process reads pixel data stored in photodetector at the identical order and speed as reset operation. The difference in time between reset and readout operation is known as integration time (refer to Figure 24). Integration time controls photodetector's level of exposure to light. Integration time can be adjusted in line unit level (line inttime) and column unit level (column inttime). Upper 16 bits of inttime register represent number of lines for line inttime and lower 8 bits of inttime register represent number of column inttime, where number of column changes in framewidth/256 increment. Trade-off relationship can be set between integration time and frame rate by enabling frame variable mode. If frmvar_en=1'b1 and integration time is larger than the frame height, the system accommodates the integration time by changing the maximum frame height internally. Due to this process, overall frame structure increases which results in decrease in frame rate.

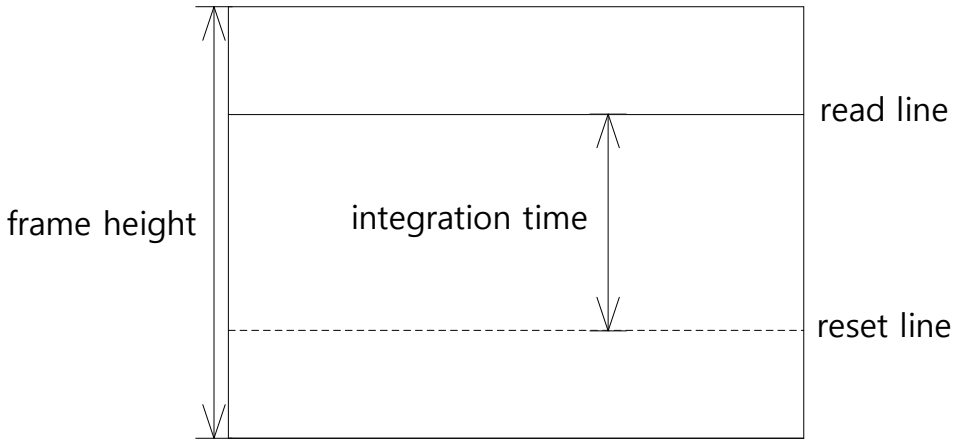


Figure 24 Fundamental concept of integration time

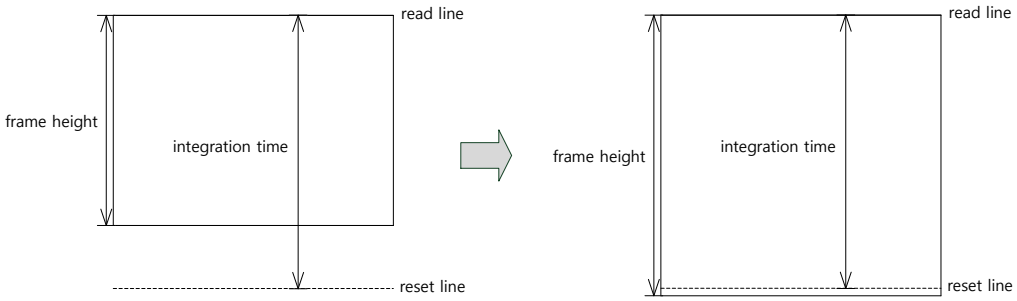


Figure 25 Integration time with frame variable mode enabled

Table 24 shows registers relevant to integration time.

[1] Image capture method in which each frame is scanned row by row instead of capturing entire frame at once

Table 24 Register Table - Integration time

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
auto_off	C	8B	[7:0]	0x00	RW		All automatic operation on / off 1'b0 : auto on 1'b1 : auto off
inttime_h	B	BC	[7:0]	0x01	RW	aev	Integration time (line)
inttime_m	B	BD	[7:0]	0x40	RW	aev	
inttime_l	B	BE	[7:0]	0x00	RW	aev	Integration time (column)
frmvar_en	B	15	[6]	1'b0	RW		Frame rate variable mode 1'b0: disable 1'b1: enable
m_inttime_tgout_H	B	E9	[7:0]		RO		Tg intergration time monitoring
m_inttime_tgout_M	B	EA	[7:0]		RO		
m_inttime_tgout_L	B	EB	[7:0]		RO		

Global Gain

Global gain affects analog gain level of comparators, which determines Bayer data values.

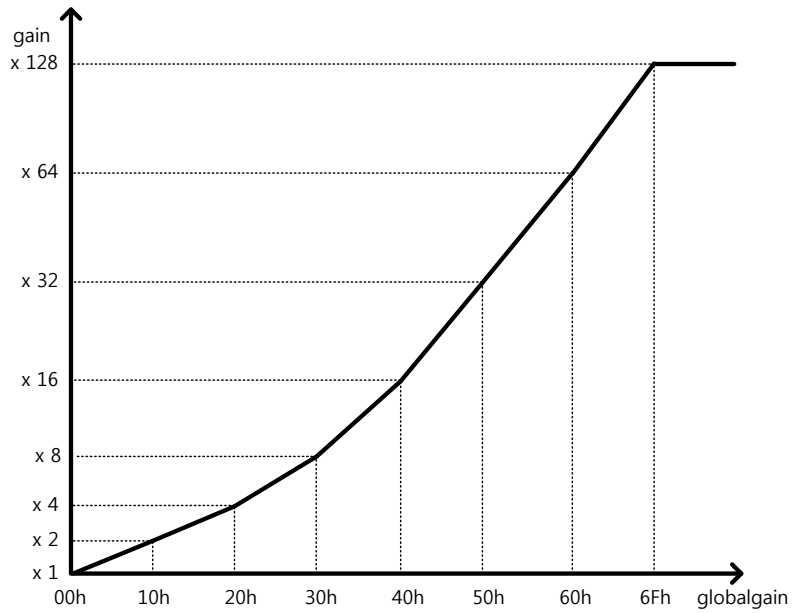


Figure 26 Globalgain's gain

Table 25 shows registers relevant to global gain.

Table 25 Register Table - Global Gain

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
globalgain	B	BF	[7:0]	0x00	RW	aev	Analog gain

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
globalgain_max	B	F4	[7:0]	0x6F	RW		Max. analog gain

Digital Gain

Analog signal is converted to digital value through ADC operation, and the digital value can be amplified by digital gain. digitalgain register's upper 2 bits are positive integer and lower 6 bits are fraction.

Table 26 shows registers relevant to digital gain

Table 26 Register Table - Digital gain

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
digitalgain	B	C0	[7:0]	0x40	RW	aev	Digital gain

Recommended Exposure Setting Procedure

Due to exposure controls being split across several registers, all exposure related registers, such as inttime, global gain, and digital gain, needs to be updated simultaneously to ensure reliable exposure update. It is recommended to disable "aev" type registers updates before updating exposure registers. Disabling "aev" type updates can be achieved by setting i2c_control = 0. Once exposure register updates are disabled, user can set the exposure value safely. New exposure value is applied to next frame after reverting i2c_control register to default value. Figure 27 shows sequence of recommended exposure setting

Note If recommended exposure setting procedure is not followed for setting exposure registers, then it may not update all the new exposure values in one frame.

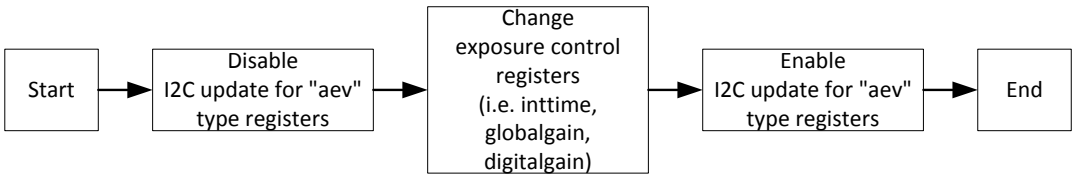


Figure 27 Recommended exposure setting sequence

Black Level Compensation (BLC) Control

Digital black level compensation (BLC) evaluates reference black level based on row optical black pixel (ROBP) and subtracts black level from active pixel value.

Front Black Fitting and Evaluation

Front black is used as an offset value to black level in BLC calculation.

- if dblc_mode = 1'b0, 8-bit 1's complement number representation, which ranges from -127 to 127, is used.
- if dblc_mode = 1'b1, 8-bit positive real number is used, front black value can range from 0 to 255.
- if "front_black fitting" = 1'b0, front_black_ref0 becomes front black value.
- if "front_black fitting" = 1'b1, front_black_ref0~7 are used as reference points for linear fitting respect to global gain.

Figure 28 shows an example of front black fitting.

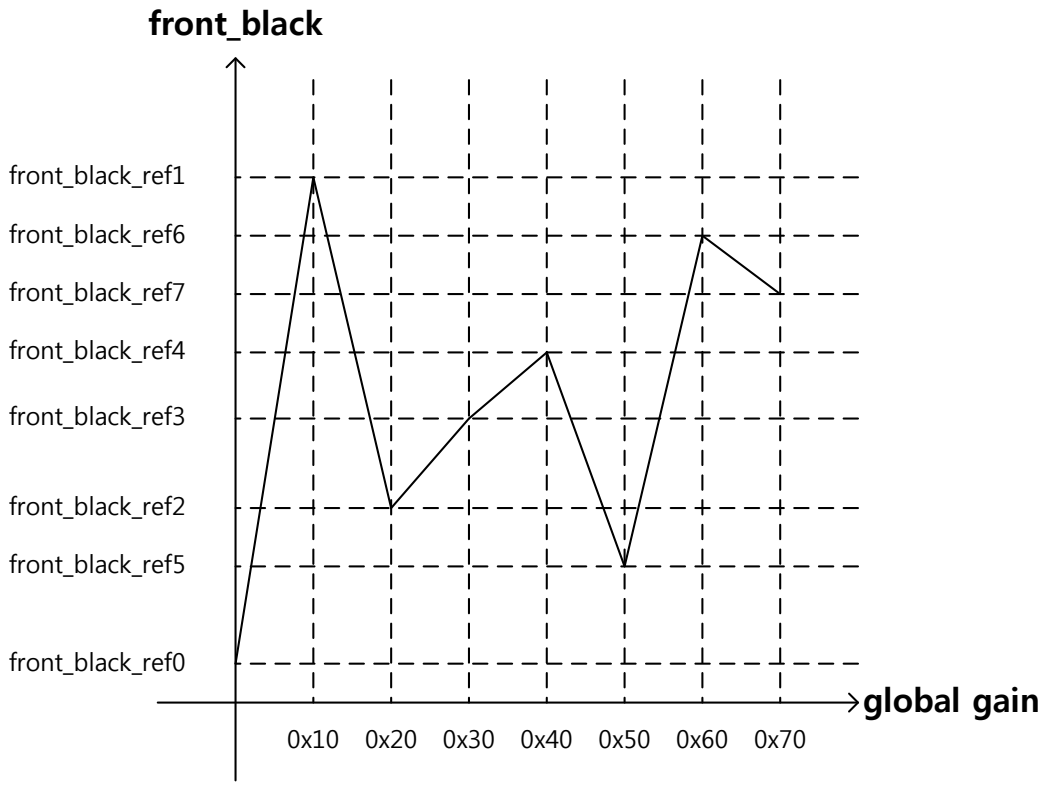


Figure 28 Example of front black fitting

Table 27 shows registers relevant to front black fitting and evaluation.

Table 27 Register Table - Front black

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
fb gg	E	05	[3]	1'b0	RW	autov	Global gain selection in front black fitting 1'b0 : high sensitivity conversion gain 1'b1 : normal gain
front_black fitting	E	06	[4]	1'b0	RW	autov	Front black fitting control 1'b0: disable 1'b1: enable
front_black	B	A8	[7:0]	0x00	RW	aev	Front black value
front_black_ref0	B	A0	[7:0]	0x82	RW		Front black fitting points @ front_black_fit_en=1'b1
front_black_ref1	B	A1	[7:0]	0x82	RW		
front_black_ref2	B	A2	[7:0]	0x82	RW		
front_black_ref3	B	A3	[7:0]	0x00	RW		
front_black_ref4	B	A4	[7:0]	0x02	RW		
front_black_ref5	B	A5	[7:0]	0x02	RW		
front_black_ref6	B	A6	[7:0]	0x02	RW		
front_black_ref7	B	A7	[7:0]	0x02	RW		
blackdly	B	16	[4]	1'b1	RW		Front black delay
dblc_mode	B	1E	[3]	1'b0	RW	aev	Number representation control 1'b0: 1's compliment number 1'b1: natural number

ISP(Image Signal Processing)

Test Pattern (TP) Control

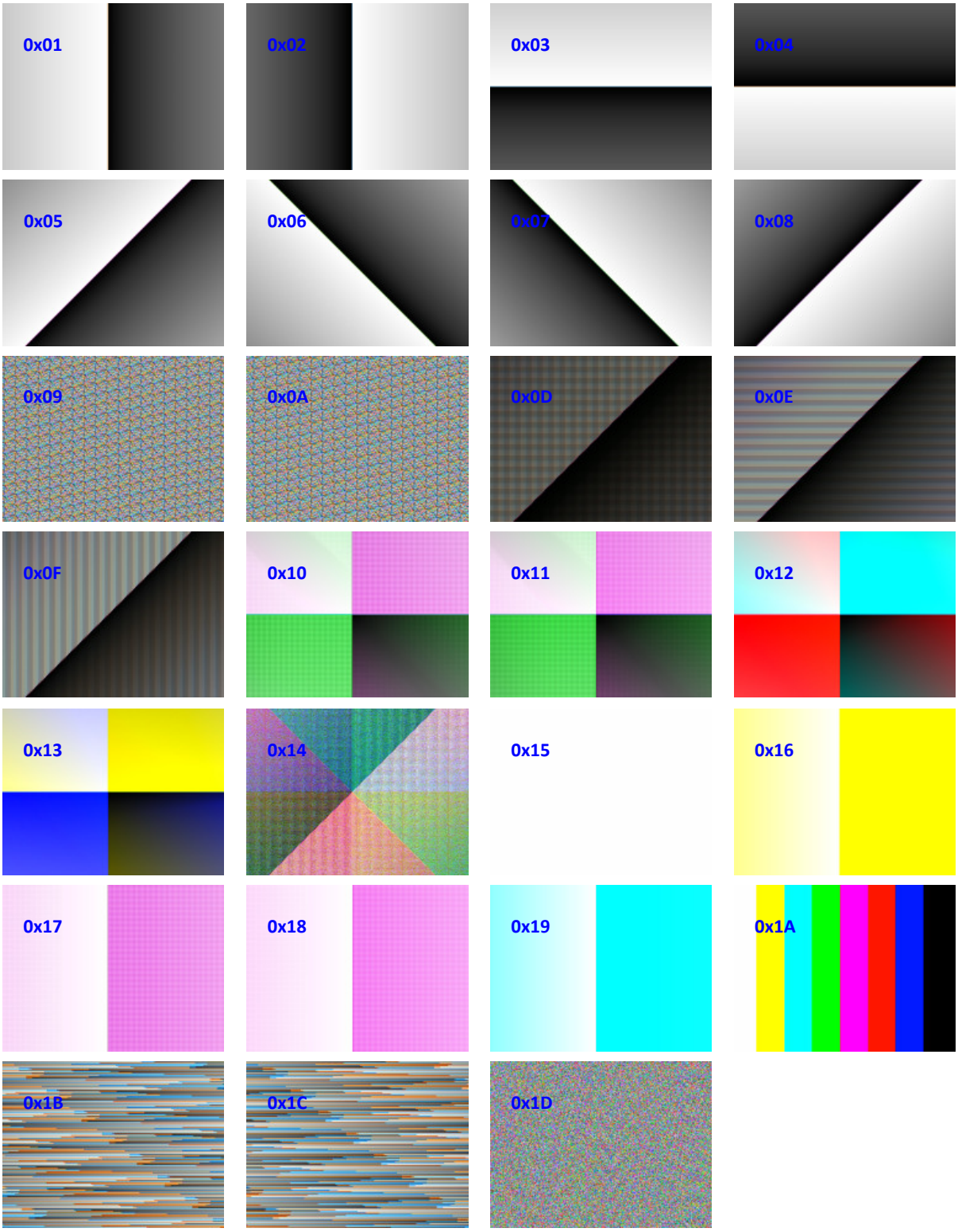
TP control generates test images from ISP block. Test images type can be selected by setting tp_control_0 registers. In case of test image types from 0x15 to 0x1A values for tp_control_0, front_black_ref1/2/3/4/5 registers are used as color values and the following rule shows how the color value is determined:

- R : {front_black_ref1, front_black_ref5[7:6]}
- G1 : {front_black_ref2, front_black_ref5[5:4]}
- G2 : {front_black_ref3, front_black_ref5[3:2]}
- B : {front_black_ref4, front_black_ref5[1:0]}

Table 28 shows registers relevant to Test Pattern Control

Table 28 Register Table - ISP test pattern

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
tp_control_0	C	0C	[7:0]	0x00	RW		Test image selection
front_black_ref1	B	A1	[7:0]	0x00	RW		R[9:2] value for test image
front_black_ref2	B	A2	[7:0]	0x00	RW		Gr[9:2] value for test image
front_black_ref3	B	A3	[7:0]	0x00	RW		Gb[9:2] value for test image
front_black_ref4	B	A4	[7:0]	0x00	RW		B[9:2] value for test image
front_black_ref5	B	A5	[7:0]	0x00	RW		{R[1:0], G1[1:0], G2[1:0], B[1:0]} value for test image



[front_black_ref1, front_black_ref2, front_black_ref3, front_black_ref4, front_black_ref5 = 0xFF]

Figure 29 ISP test pattern

Lens Shading Compensation (LSC)

Pixel sensor residing in edge of the lens receives less light, whereas ample light exposure is obtained in center pixels. LSC feature compensates this uneven distribution of light exposure. By setting lens_en = 1'b1, LSC feature is enabled. LSC function control components are LSC center, LSC scale, and LSC gain.

- LSC center
  By setting lens_x and lens_y, LSC center is adjusted as shown in Figure 30. This parameter is adjusted if the center of the image is not lined up with the center of the lens.

- LSC scale
  By setting lens_scale, scale rate of lens gain from the LSC center is adjusted. lens_scale value is directly proportional to lens gain value.

- LSC gain
  Lens gain of R, G1, G2, B channel can be separately adjusted through lens_gainr, lens_gaing1, lens_gaing2, and lens_gainb registers respectively. Setting high value to the registers result in high lens gain.

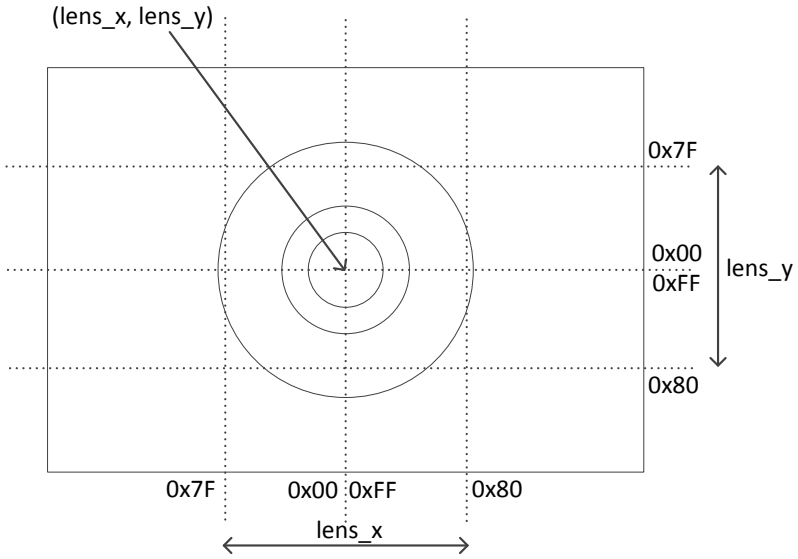


Figure 30 LSC center control

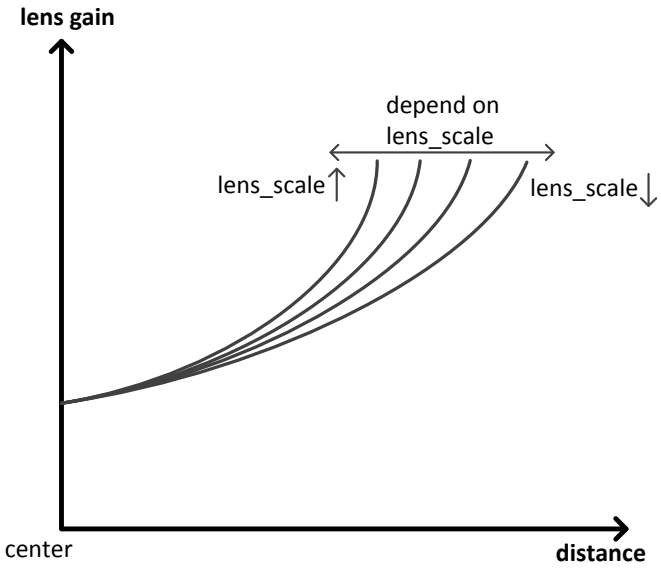


Figure 31 LSC gain fitting with LSC center and LSC scale

Table 29 shows registers relevant to LSC functions.

Table 29 Register Table - LSC

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
lens_en	C	04	[7]	1'b1	RW	aev	Lens shading compensation enable 1'b0 : disable 1'b1 : enable
lens_scale	C	0E	[7:0]	0x51	RW		Lens shading scale control
lens_x	C	13	[7:0]	0x00	RW		Lens shading center control
lens_y	C	14	[7:0]	0x00	RW		
lens_gainr	C	0F	[7:0]	0x00	RW	aev	R gain for lens shading
lens_gaing1	C	10	[7:0]	0x02	RW	aev	G1 gain for lens shading
lens_gaing2	C	11	[7:0]	0x02	RW	aev	G2 gain for lens shading
lens_gainb	C	12	[7:0]	0x00	RW	aev	B gain for lens shading

White Balance Gain

WB gain is applied to images to remove the unrealistic color coming from different color temperature. Proper application of WB results in objects which appear white in person are displayed white in the output image.

Table 30 shows registers relevant to WB gain

Table 30 Register Table - White balance gain

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
awb_en	C	04	[6]	1'b1	RW	aev	AWB gain multification enable 1'b0 : disable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							1'b1 : enable
wb_rgain_h	D	1B	[0]	0x00	RW	aev	White balance gain
wb_rgain_l	D	1C	[7:0]	0x5D	RW	aev	
wb_ggain_h	D	1D	[0]	0x00	RW	aev	
wb_ggain_l	D	1E	[7:0]	0x40	RW	aev	
wb_bgain_h	D	1F	[0]	0x00	RW	aev	
wb_bgain_l	D	20	[7:0]	0x5E	RW	aev	

Edge Enhancement

Edge enhancement function controls the sharpness of input image. The function is enabled by setting edge_en = 1’b1. Control factors for edge enhancement are edge gain, edge threshold, and edge maximum value.

- Edge gain
  Edge is intensified directly by setting high edge gain values. edge_gain, ec_pgain and ec_mgain affects positive edge gain and negative edge gain respectively.

- Edge threshold
  Threshold can be set to exclude edge with certain level to be excluded from edge enhancement process. Edge value smaller than dark_ec_pth are excluded from the process for positive edge. In similar fashion, edge value smaller than dark_ec_mth are excluded from the process for negative edge.

- Edge Max. value
  After edge threshold evaluation, maximum value clamping is proceeded. Maximum edge value for positive edge is dark_ec_pmax and for negative edge is dark_ec_mmax.

Table 31 shows registers relevant to edge enhancement functions.

Table 31 Register Table - Edge enhancement

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
edge_en	C	05	[3]	1'b1	RW	aev	Edge enhancement enable 1'b0 : disable 1'b1 : enable
edge_gain	C	27	[7:0]	0x20	RW	aev	Edge gain
ec_pgain	C	28	[7:0]	0x40	RW		Positive edge clamp gain
ec_mgain	C	29	[7:0]	0x80	RW		Negative edge clamp gain
dark_ec_pth	D	68	[7:0]	0x04	RW	aev	Positive edge clamp threshold
dark_ec_mth	D	6C	[7:0]	0x04	RW	aev	Negative edge clamp threshold
dark_ec_pmax	D	70	[7:0]	0x7F	RW	aev	Max. positive edge clamp
dark_ec_mmax	D	74	[7:0]	0x7F	RW	aev	Max. negative edge clamp

Color Correction (CCR)

CCR function utilizes 3 by 3 matrix multiplication to correct RGB color. dark_ccr register reduces the effectiveness of CCR. As dark_ccr value increases, degree of CCR decreases.

$$\begin{bmatrix} R` \\ G` \\ B` \end{bmatrix} = \begin{bmatrix} ccr\_m11 & ccr\_m12 & ccr\_m13 \\ ccr\_m21 & ccr\_m22 & ccr\_m23 \\ ccr\_m31 & ccr\_m32 & ccr\_m33 \end{bmatrix} X \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Figure 32 CCR matrix

Table 32 shows registers relevant to CCR functions.

Table 32 Register Table - CCR

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ccr_en	C	04	[1]	1'b1	RW	aev	Color correction enable 1'b0 : disable 1'b1 : enable
ccr_m11	C	33	[7:0]	0x30	RW		Color correction matrix value
ccr_m12	C	34	[7:0]	0x8C	RW		
ccr_m13	C	35	[7:0]	0x84	RW		
ccr_m21	C	36	[7:0]	0x86	RW		
ccr_m22	C	37	[7:0]	0x34	RW		
ccr_m23	C	38	[7:0]	0x8C	RW		
ccr_m31	C	39	[7:0]	0x81	RW		
ccr_m32	C	3A	[7:0]	0x99	RW		
ccr_m33	C	3B	[7:0]	0x3A	RW		
dark_ccr	D	4B	[7:0]	0x00	RW	aev	Darkness value for color correction

RGB Gamma

RGB gamma function performs non-linear operation on RGB color after CCR. RGB gamma function can configure two different gamma reference curves: gamma curve1 and gamma curve2. Depending on the dark_rgb_gm setting level, the system determines which curve to apply for RGB (refer to Figure 33). RGB gamma is enabled by setting rgbgm_en = 1’b1.

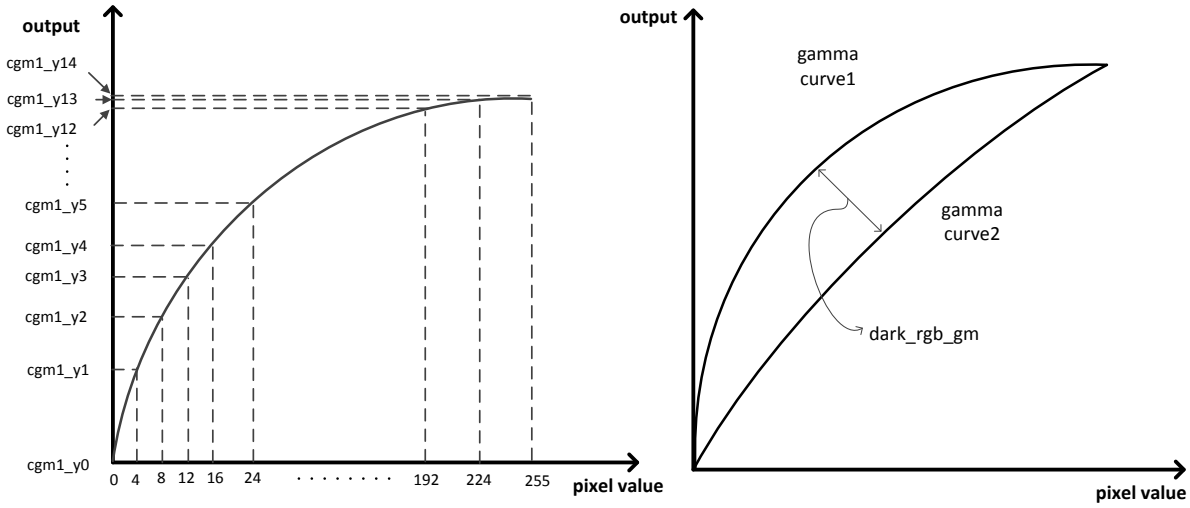


Figure 33 Gamma curve fitting of RGB gamma

Table 33 shows registers relevant to RGB gamma functions.

Table 33 Register Table - RGB gamma

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
rgbgm_en	C	05	[7]	1'b1	RW	aev	RGB gamma enable 1'b0 : disable 1'b1 : enable
cgm1_y0	C	5B	[7:0]	0x00	RW		Gamma curve reference1 for RGB gamma
cgm1_y1	C	5C	[7:0]	0x0B	RW		
cgm1_y2	C	5D	[7:0]	0x17	RW		
cgm1_y3	C	5E	[7:0]	0x22	RW		
cgm1_y4	C	5F	[7:0]	0x2E	RW		
cgm1_y5	C	60	[7:0]	0x40	RW		
cgm1_y6	C	61	[7:0]	0x50	RW		
cgm1_y7	C	62	[7:0]	0x6E	RW		
cgm1_y8	C	63	[7:0]	0x88	RW		
cgm1_y9	C	64	[7:0]	0xAE	RW		
cgm1_y10	C	65	[7:0]	0xCA	RW		
cgm1_y11	C	66	[7:0]	0xDC	RW		
cgm1_y12	C	67	[7:0]	0xEC	RW		
cgm1_y13	C	68	[7:0]	0xF6	RW		
cgm1_y14	C	69	[7:0]	0xFF	RW		
cgm2_y0	C	6A	[7:0]	0x00	RW		Gamma curve reference2 for RGB gamma
cgm2_y1	C	6B	[7:0]	0x04	RW		
cgm2_y2	C	6C	[7:0]	0x08	RW		

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
cgm2_y3	C	6D	[7:0]	0x0C	RW		
cgm2_y4	C	6E	[7:0]	0x10	RW		
cgm2_y5	C	6F	[7:0]	0x18	RW		
cgm2_y6	C	70	[7:0]	0x20	RW		
cgm2_y7	C	71	[7:0]	0x30	RW		
cgm2_y8	C	72	[7:0]	0x40	RW		
cgm2_y9	C	73	[7:0]	0x60	RW		
cgm2_y10	C	74	[7:0]	0x80	RW		
cgm2_y11	C	75	[7:0]	0xA0	RW		
cgm2_y12	C	76	[7:0]	0xC0	RW		
cgm2_y13	C	77	[7:0]	0xE0	RW		
cgm2_y14	C	78	[7:0]	0xFF	RW		
dark_rgb_gm	D	55	[7:0]	0x00	RW	aev	Darkness value for RGB gamma

De-color

De-color function reduces chroma level and is enabled by setting dc_en = 1’b1. High dark_dc level results in achromatic color. The maximum value of dark_dc is 0x3F.

Table 34 shows registers relevant to decolor functions.

Table 34 Register Table - De-color

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
dc_en	C	0A	[2]	1'b1	RW	aev	De-color enable 1'b0 : disable 1'b1 : enable
dark_dc	D	7A	[7:0]	0x00	RW	aev	De-color component

Y Gamma

Y gamma function performs non-linear operation on Y component. Y gamma function can configure two different gamma reference curves: gamma curve1 and gamma curve2. Depending on the dark_y_gm setting level, the system determines which curve to apply for Y (refer to Figure 34). Y gamma is enabled by setting ygm_en = 1’b1.

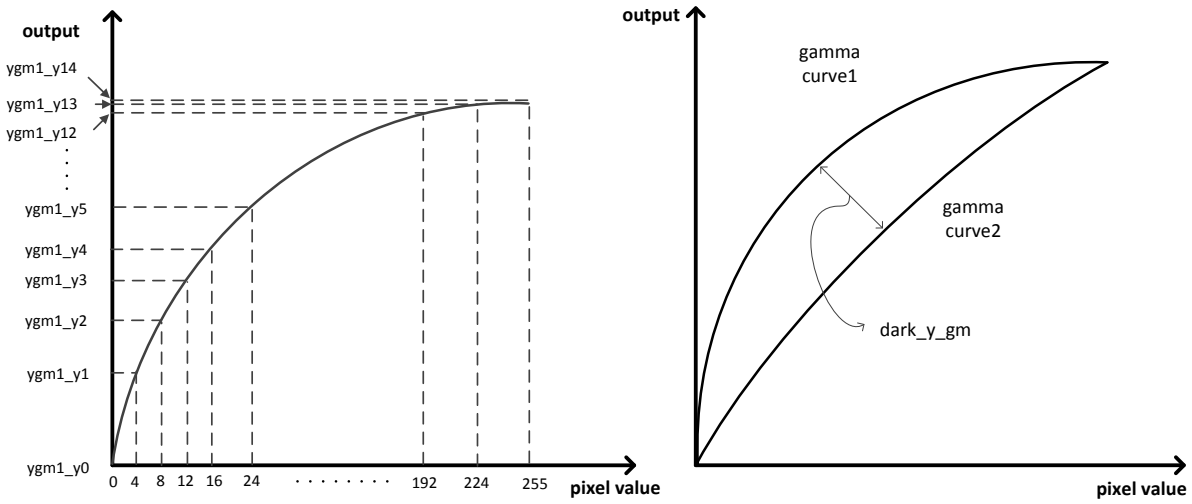


Figure 34 Gamma curve fitting of Y gamma

Table 35 shows registers relevant to Y gamma functions.

Table 35 Register Table - Y Gamma

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ygm_en	C	05	[6]	1'b1	RW	aev	Y gamma enable 1'b0 : disable 1'b1 : enable
ygm1_y0	C	3D	[7:0]	0x00	RW		Y gamma1 curve reference
ygm1_y1	C	3E	[7:0]	0x05	RW		
ygm1_y2	C	3F	[7:0]	0x14	RW		
ygm1_y3	C	40	[7:0]	0x25	RW		
ygm1_y4	C	41	[7:0]	0x34	RW		
ygm1_y5	C	42	[7:0]	0x4B	RW		
ygm1_y6	C	43	[7:0]	0x5B	RW		
ygm1_y7	C	44	[7:0]	0x73	RW		
ygm1_y8	C	45	[7:0]	0x86	RW		
ygm1_y9	C	46	[7:0]	0xA3	RW		
ygm1_y10	C	47	[7:0]	0xBA	RW		
ygm1_y11	C	48	[7:0]	0xCE	RW		
ygm1_y12	C	49	[7:0]	0xE0	RW		
ygm1_y13	C	4A	[7:0]	0xF0	RW		
ygm1_y14	C	4B	[7:0]	0xFF	RW		
ygm2_y0	C	4C	[7:0]	0x00	RW		Y gamma2 curve reference
ygm2_y1	C	4D	[7:0]	0x06	RW		
ygm2_y2	C	4E	[7:0]	0x0B	RW		

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ygm2_y3	C	4F	[7:0]	0x10	RW		
ygm2_y4	C	50	[7:0]	0x15	RW		
ygm2_y5	C	51	[7:0]	0x1E	RW		
ygm2_y6	C	52	[7:0]	0x27	RW		
ygm2_y7	C	53	[7:0]	0x39	RW		
ygm2_y8	C	54	[7:0]	0x49	RW		
ygm2_y9	C	55	[7:0]	0x6A	RW		
ygm2_y10	C	56	[7:0]	0x89	RW		
ygm2_y11	C	57	[7:0]	0xA8	RW		
ygm2_y12	C	58	[7:0]	0xC6	RW		
ygm2_y13	C	59	[7:0]	0xE3	RW		
ygm2_y14	C	5A	[7:0]	0xFF	RW		
dark_y_gm	D	51	[7:0]	0x00	RW	aev	Darkness value for Y gamma

Contrast

Contrast function performs linear operation on Y component. y_cont_th2 acts as the reference point of linear function, and y_cont_slope2 determines the linear function's slope.

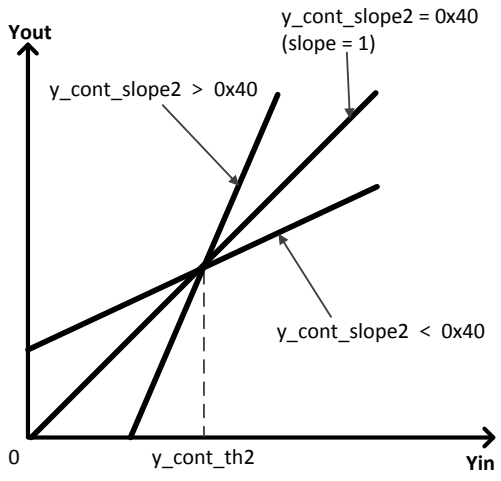


Figure 35 ISP Contrast control

Table 36 shows registers relevant to contrast functions.

Table 36 Register Table - Contrast

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
y_cont_th2	D	9A	[7:0]	0x80	RW	aev	X-axis standard for contrast line
y_cont_slope2	D	9E	[7:0]	0x40	RW	aev	Slope for contrast line

Color Saturation

Color saturation functions performs 2 by 2 matrix operation on chroma domain (Cb/Cr) to adjust hue and saturation. user_cs register is additional multiplication coefficient parameter for cs11 and cs22 components

$$\begin{bmatrix} Cb` \\ Cr` \end{bmatrix} = user\_cs \begin{bmatrix} cs11 & cs12 \\ cs21 & cs22 \end{bmatrix} X \begin{bmatrix} Cb \\ Cr \end{bmatrix}$$

Figure 36 Color saturation matrix

Table 37 shows registers relevant to color saturation functions.

Table 37 Register Table - Color saturation

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
cs11	C	80	[7:0]	0x25	RW	aev	Color saturation matrix value
cs12	C	81	[7:0]	0x00	RW	aev	
cs21	C	82	[7:0]	0x00	RW	aev	
cs22	C	83	[7:0]	0x25	RW	aev	
user_cs	D	13	[7:0]	0x2C	RW		User color saturation gain

Auto Exposure Control

AE Auto/Manual Mode Control

There are auto mode and manual mode in AE operation mode. Normally, it operates in auto mode. Auto/manual mode operates as follows according to exposure_mode [1:0] setting.

- exposure_mode[1:0] = 2'b00(auto mode)
  The exposure value changes according to the image characteristic. Inttime, globalgain, and digitalgain are calculated by the exposure value.
- exposure_mode[1:0] = 2'b01(manual1 : exposure control)
  The user can set the exposure directly. Inttime, globalgain, and digitalgain are calculated by the exposure value.
- exposure_mode[1:0] = 2'b10(manual2 : external gain control)
  The applied inttime corresponds to ext_inttime, and the applied globalgain corresponds to ext_glbg. User can set ext_inttime, ext_glbg directly.
- exposure_mode[1:0] = 2'b11(manual3 : inttime, gain control)
  User directly controls inttime, globalgain, and digitalgain.

Table 38 Register Table - AE manual

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
auto_off	C	8B	[7:0]	0x00	RW		Auto off (MCU off)
exposure mode	E	04	[1:0]	2'b00	RW	autov	Exposure mode selection 2'b00 : auto mode 2'b01 : manual1 (exposure write) 2'b10 : manual2 (ext_inttime, ext_glbgain write) 2'b11 : manual3 (inttime, globalgain write)
exposure_t	E	27	[7:0]	0x00	RW	autov	Exposure value
exposure_h	E	28	[7:0]	0x01	RW	autov	
exposure_m	E	29	[7:0]	0x40	RW	autov	
exposure_l	E	2A	[7:0]	0x00	RW	autov	
ext_inttime_h	E	22	[7:0]	0x00	RW	autov	Manual integration time @ external AE mode
ext_inttime_m	E	23	[7:0]	0x80	RW	autov	Manual integration time @ external AE mode
ext_inttime_l	E	24	[7:0]	0x00	RW	autov	Manual integration time @ external AE mode
ext_glbg_h	E	25	[7:0]	0x01	RW	autov	Manual analog gain @ external AE mode
ext_glbg_l	E	26	[7:0]	0x00	RW	autov	Manual analog gain @ external AE mode
inttime_h	B	BC	[7:0]	0x01	RW	aev	Integration time (line)
inttime_m	B	BD	[7:0]	0x40	RW	aev	Integration time (line)
inttime_l	B	BE	[7:0]	0x00	RW	aev	Integration time (column)
globalgain	B	BF	[7:0]	0x00	RW	aev	Analog gain
digitalgain	B	C0	[7:0]	0x40	RW	aev	Digital gain

AE Window Setting

The AE window is divided into AE_window1, AE_windiw2, AE_windiw3, AE_window4, and AE_windowC areas(refer to Figure 37). The user can view the AE window as an output image by setting win_show[1] to 1'b1.

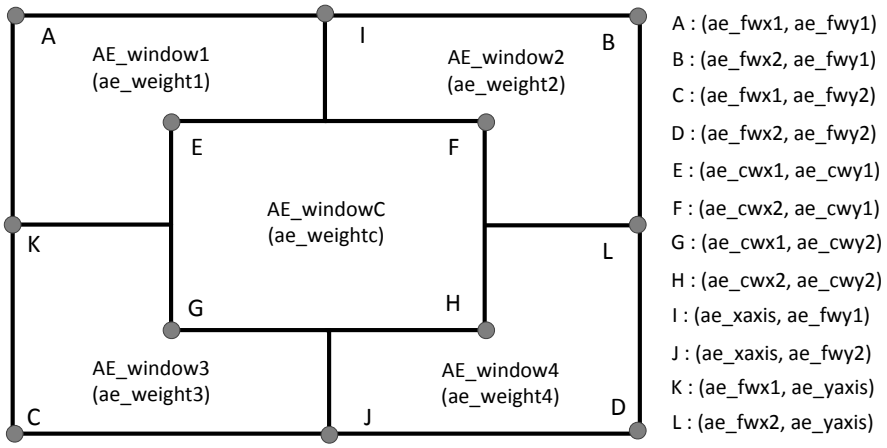


Figure 37 AE window setting

Table 39 Register Table - AE window setting

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
win_show[1:0]	C	08	[7:6]	2'b00	RW	aev	win_show[1] : ae window show enable 1'b0 : disable 1'b1 : enable win_show[0] : awb window show enable 1'b0 : disable 1'b1 : enable
ae_fwx1_h	C	B3	[1:0]	0x00	RW		AE window control
ae_fwx1_l	C	B4	[7:0]	0x01	RW		
ae_fwx2_h	C	B5	[1:0]	0x02	RW		
ae_fwx2_l	C	B6	[7:0]	0x80	RW		
ae_fwy1_h	C	B7	[1:0]	0x00	RW		
ae_fwy1_l	C	B8	[7:0]	0x01	RW		
ae_fwy2_h	C	B9	[1:0]	0x01	RW		
ae_fwy2_l	C	BA	[7:0]	0xE0	RW		
ae_cwx1_h	C	BB	[1:0]	0x00	RW		
ae_cwx1_l	C	BC	[7:0]	0xD6	RW		
ae_cwx2_h	C	BD	[1:0]	0x01	RW		
ae_cwx2_l	C	BE	[7:0]	0xAB	RW		
ae_cwy1_h	C	BF	[1:0]	0x00	RW		
ae_cwy1_l	C	C0	[7:0]	0xA1	RW		
ae_cwy2_h	C	C1	[1:0]	0x01	RW		
ae_cwy2_l	C	C2	[7:0]	0x40	RW		

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ae_xaxis_h	C	C3	[1:0]	0x01	RW		
ae_xaxis_l	C	C4	[7:0]	0x41	RW		
ae_yaxis_h	C	C5	[1:0]	0x00	RW		
ae_yaxis_l	C	C6	[7:0]	0xF1	RW		

Auto White Balance Control

AWB Auto/Manual Mode Control

There are auto mode and manual mode in AWB operation mode. Normally, it operates in auto mode. Auto/manual mode operates as follows according to wb_mode setting.

- wb_mode = 1'b0(auto mode)
  The AWB block calculates the WB gain to match the white balance. WB gain is stored in wb_rgain_h to wb_bgain_l.

- wb_mode = 1'b1(manual mode)
  The user can adjust the WB gain by directly writing wb_rgain_h to wb_bgain_l.

Wb_gratio adjusts the G gain value among the WB gains. The default value is 0x80. As the data is written more than 0x80, the image has a greenish characteristic.

Table 40 Register Table - AWB Manual

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
wb mode	E	04	[2]	1'b0	RW	autov	White blance mode selection 1'b0 : auto mode 1'b1 : manual mode using wb_rgain_h ~ wb_bgain_l
wb_rgain_h	D	1B	[0]	0x00	RW	aev	White balance gain @ wb_manual = 00h
wb_rgain_l	D	1C	[7:0]	0x5D	RW	aev	
wb_ggain_h	D	1D	[0]	0x00	RW	aev	
wb_ggain_l	D	1E	[7:0]	0x40	RW	aev	
wb_bgain_h	D	1F	[0]	0x00	RW	aev	
wb_bgain_l	D	20	[7:0]	0x5E	RW	aev	
wb_gratio	D	5B	[7:0]	0x80	RW		wb_ggain ratio

AWB Window Setting

The AWB window setting controls the area to be applied to the AWB calculation(refer to Figure 38). The user can view the AWB window as an output image by setting win_show[0] to 1'b1.

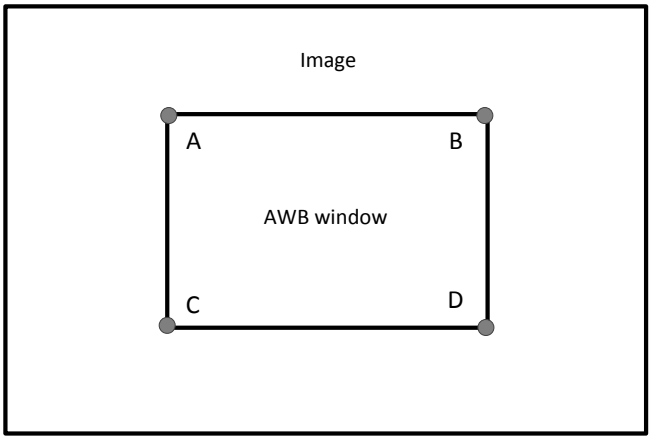


Figure 38 AWB window setting

Table 41 Register Table - AWB window

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
win_show[1:0]	C	08	[7:6]	2'b00	RW	aev	win_show[1] : ae window show enable 1'b0 : disable 1'b1 : enable win_show[0] : awb window show enable 1'b0 : disable 1'b1 : enable
awb_wx1_h	C	C7	[1:0]	0x00	RW		AWB window control
awb_wx1_l	C	C8	[7:0]	0x01	RW		
awb_wx2_h	C	C9	[1:0]	0x02	RW		
awb_wx2_l	C	CA	[7:0]	0x80	RW		
awb_wy1_h	C	CB	[1:0]	0x00	RW		
awb_wy1_l	C	CC	[7:0]	0x01	RW		
awb_wy2_h	C	CD	[1:0]	0x01	RW		
awb_wy2_l	C	CE	[7:0]	0xE0	RW		

Embedded Parking Guide Line

Parking Guide Line Palette

The Parking guide line image is composed of various straight lines and various colors. A palette is used to represent the color of the straight lines. The color of the palette can be controlled by register setting. The YCbCr domain represents palette colors and consists of a total of 4 palettes.

Table 42 Register Table - Parking guide line palette

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
palette_1_y	G	1A	[7:0]	0x90	RW		Palette 1
palette_1_cb	G	1B	[7:0]	0x35	RW		
palette_1_cr	G	1C	[7:0]	0x22	RW		
palette_2_y	G	1D	[7:0]	0xD2	RW		Palette 2
palette_2_cb	G	1E	[7:0]	0x10	RW		
palette_2_cr	G	1F	[7:0]	0x92	RW		
palette_3_y	G	20	[7:0]	0x51	RW		Palette 3
palette_3_cb	G	21	[7:0]	0x5A	RW		
palette_3_cr	G	22	[7:0]	0xF0	RW		
palette_4_y	G	23	[7:0]	0x10	RW		Palette 4
palette_4_cb	G	24	[7:0]	0x80	RW		
palette_4_cr	G	25	[7:0]	0x80	RW		
osd3_enable	A	81	[3]	1'b0	RW		OSD layer3 display 0b: disable 1b: enable
osd_opac3	G	18	[4:0]	0x10	RW		OSD transparency

Parking Guide Line Control

Since the image data related to the parking guide is stored in PC7080D, the data of the external ROM is not necessary.

Figure 39 represents the parking guide line. If pg_enable is 1'b1, the parking guide line is enabled.

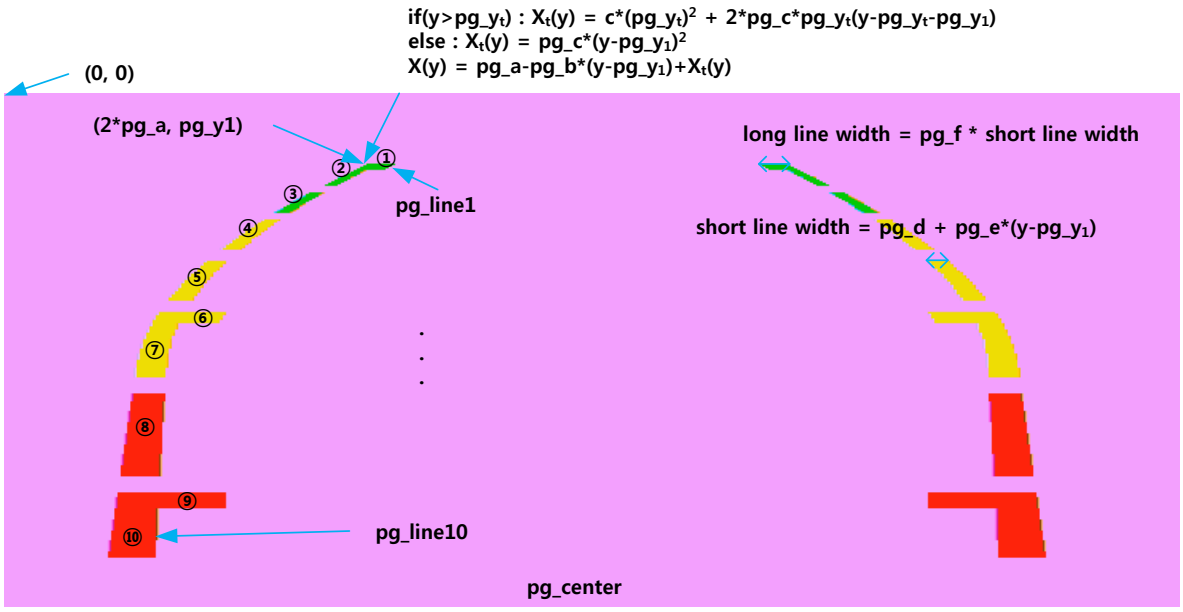


Figure 39 Parking guide line

- pg_yt
  It shows the boundary between the straight line and the curve of the embedded parking guide line.
- pg_y1~10
  Embedded parking guide lines can be represented by up to 10 dashed lines. pg_y1 ~ 10 represent y start coordinates of 10 dashed lines. pg_y2 / 10 is the relative coordinate with pg_y1.
- pg_a
  pg_a is the starting x-coordinate of the embedded parking guide line. The x-coordinate is 2*pg_a and must be at least 1.
- pg_b
  pg_b determines the overall linear slope of the embedded parking guide line.
- pg_c
  Pg_c indicates the degree of bending of the curve of the embedded parking guide line
- pg_d
  pg_d is the initial line width of the embedded parking guide line. The line width should be at least 4.
- pg_e
  The line width of the embedded parking guide line increases as it goes downward. pg_e adjusts the increment of the line width.
- pg_f

pg_f determines the size of the long line width. The "long line width" is pg_f*"short line width".

- pg_line1~10
  Pg_line1~10 determine the height of each dotted line.
- pg_line_info1~10
  - pg_line_info1~10[3:1] : line palette
  - pg_line_info1~10[0] : line type
- pg_center
  Embedded parking guide line is symmetrical about pg_center.
- pg_hl_en
  Each line's highlight zone enable(pg_control0[4] takes precedence over pg_hl_en.)

Table 43 Register Table - Parking guide line

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pg_yt	F	08	[7:0]	0x7F	RW	aev	Embedded parking guide line height control
pg_y1	F	09	[7:0]	0x73	RW	aev	
pg_y2	F	0A	[7:0]	0x02	RW	aev	
pg_y3	F	0B	[7:0]	0x08	RW	aev	
pg_y4	F	0C	[7:0]	0x0F	RW	aev	
pg_y5	F	0D	[7:0]	0x19	RW	aev	
pg_y6	F	0E	[7:0]	0x25	RW	aev	
pg_y7	F	0F	[7:0]	0x28	RW	aev	
pg_y8	F	10	[7:0]	0x38	RW	aev	
pg_y9	F	11	[7:0]	0x4E	RW	aev	
pg_y10	F	12	[7:0]	0x52	RW	aev	
pg_a	F	13	[7:0]	0x8F	RW	aev	
pg_b	F	14	[7:0]	0x64	RW	aev	
pg_c	F	15	[7:0]	0xBF	RW	aev	
pg_d	F	16	[7:0]	0x07	RW	aev	
pg_e	F	17	[7:0]	0x0C	RW	aev	
pg_f	F	18	[7:0]	0x15	RW	aev	
pg_line1	F	19	[7:0]	0x21	RW	aev	
pg_line2	F	1A	[7:0]	0x23	RW	aev	
pg_line3	F	1B	[7:0]	0x24	RW	aev	
pg_line4	F	1C	[7:0]	0x46	RW	aev	
pg_line5	F	1D	[7:0]	0x48	RW	aev	
pg_line6	F	1E	[7:0]	0x42	RW	aev	
pg_line7	F	1F	[7:0]	0x4B	RW	aev	
pg_line8	F	20	[7:0]	0x71	RW	aev	

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pg_line9	F	21	[7:0]	0x63	RW	aev	
pg_line10	F	22	[7:0]	0x74	RW	aev	
pg_center_h	F	23	[1:0]	0x01	RW	aev	
pg_center_l	F	24	[7:0]	0x68	RW	aev	
pg_hl_en_h	F	27	[1:0]	0x00	RW	aev	
pg_hl_en_l	F	28	[7:0]	0x00	RW	aev	
pg_hlight	F	04	[4]	1'b0	RW	aev	All pg highlight enable
pg_rm_ych	F	04	[3]	1'b1	RW	aev	Remove yochul line of PG
pg_rm	F	04	[2:1]	2'b00	RW	aev	pg_rm[1] : remove left side of PG pg_rm[0] : remove right side of PG
pg_enable	F	04	[0]	1'b1	RW	aev	pg enable
pg_f_div	F	04	[5]	1'b0	RW	aev	Dividing pg field(even,odd) 1'b0: not dividing 1'b1: dividing field(even,odd)
osd_efld_s_h	G	32	[1:0]	0x00	RW	aev	OSD even field start
osd_efld_s_l	G	33	[7:0]	0x01	RW	aev	
osd_ofld_s_h	G	34	[1:0]	0x01	RW	aev	OSD odd field start
osd_ofld_s_l	G	35	[7:0]	0x0A	RW	aev	

TV Encoder

Encoder Mode

PC7080D supports NTSC, PAL mode (TV mode). In detail, there are NTSC-M, NTSC-J, PAL-M, PAL-NC, PAL-D (B, G, H, I and N), PAL-N and NTSC-4.43.

Table 44 Register Table - Encoder mode

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
enc_mode	G	B7	[1:0]	0xx	RW		Encoder mode

Horizontal Timing Control

User can control setup time, sync rising / falling timing and active data rising / falling timing according to the situation.

- Setup time
  The setup time representing the black level can be set between 0x00 and 0x1F in pclk units by setting setup_w. Figure 40 shows the horizontal time, including the setup time.

- Hsync rising(falling) and data rising(falling)
  By setting sync_rising, sync rising/falling time can be controlled. Sync_rising has a range of 0x00 to 0x0F. The unit of sync_rising is pclk.

The rising/falling time of horizontal active data start/stop is controlled by setting encdat_rising. Encdat_rising has a range of 0x00 to 0x0F. The unit of encdat_rising is pclk.

Figure 40 shows horizontal timeing including sync rising/falling and data rising/falling.

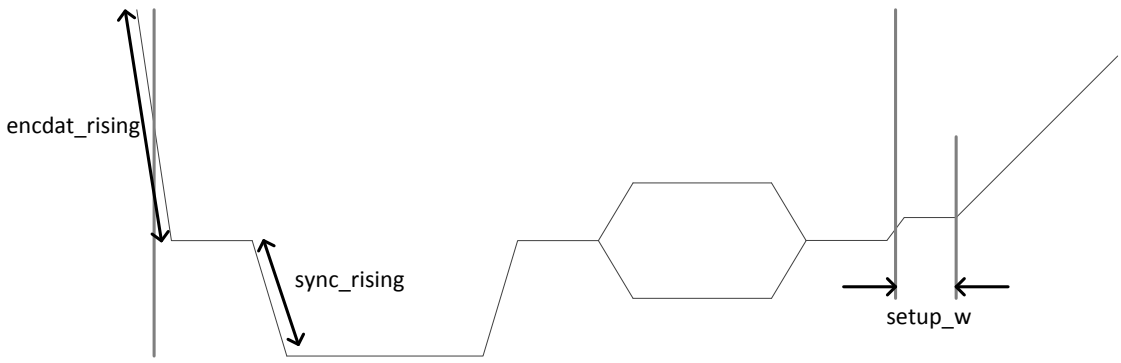


Figure 40 Horizontal timing

Table 45 Register Table - Horizontal timing

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
setup_w	G	A9	[4:0]	0x07	RW		Setup time width

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
sync_rising	G	AF	[3:0]	0x01	RW		Horizontal sync rising(falling) time control
encdat_rising	G	EB	[3:0]	0x01	RW		Edge of the line blanking pulse rising(falling) time control

Composite Level and Data Range

Each TV standard offers different levels of sync level, blank level, pedestal level, burst amplitude, and composite signal maximum level. So PC7080D is designed to be register controlled to meet each TV standard. The TV encoder uses an 11-bit data width to internally generate a composite signal and clamps it to send 10-bit data to the DAC. The user must control the min / max and Y / C range of the composite signal for clamping. Figure 41 and Figure 42 show composite signal level and data (Y / C) ranges, respectively.

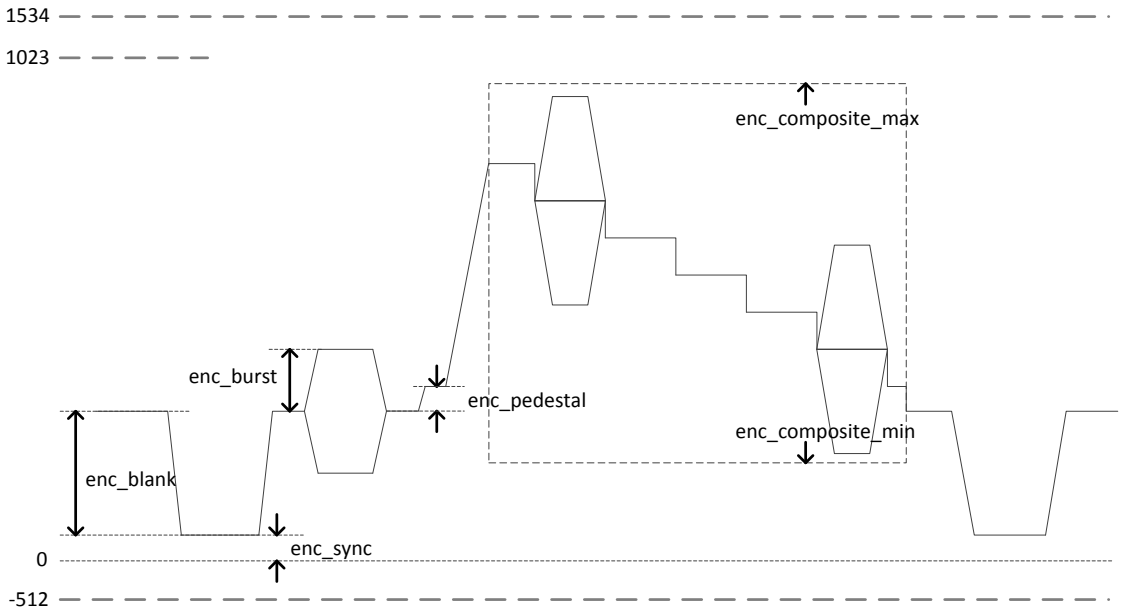


Figure 41 Composite level

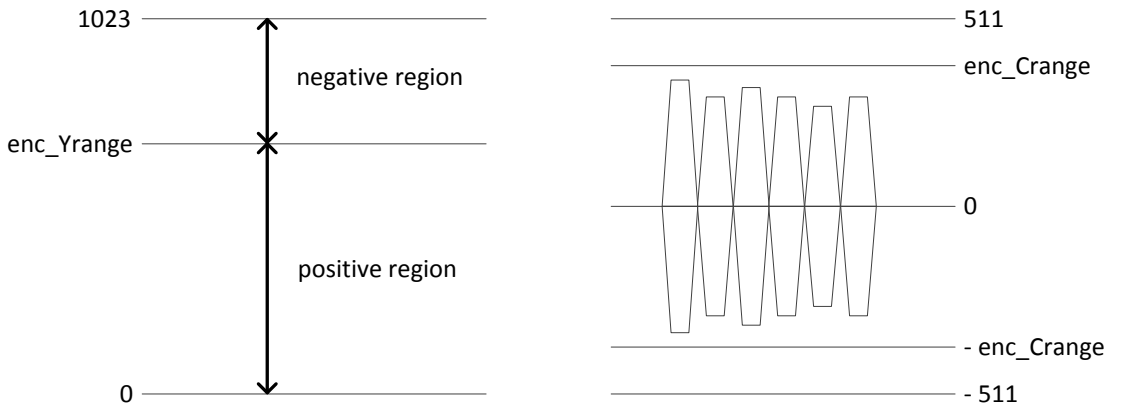


Figure 42 Data range

Table 46 Register Table - Composite level and data range

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
enc_sync	G	B8	[7:0]	0x10	RW		composite sync level
enc_blankH	G	B9	[7:0]	0x00	RW		Composite blank level
enc_blankL	G	BA	[7:0]	0xx	RW		
enc_pedestal	G	BB	[7:0]	0xx	RW		Composite pedestal level
enc_burst	G	BC	[7:0]	0xx	RW		Burst amplitude
enc_Ygain	G	BD	[7:0]	0xx	RW		Y convergence gain from YCbCr to YUV
enc_Ugain	G	BE	[7:0]	0xx	RW		U convergence gain from YCbCr to YUV
enc_Vgain	G	BF	[7:0]	0xx	RW		V convergence gain from YCbCr to YUV
enc_Yrange_H	G	C0	[7:0]	0x03	RW		Max. luminance
enc_Yrange_L	G	C1	[7:0]	0x20	RW		
enc_Crange_H	G	C2	[7:0]	0x01	RW		Max. amplitudes of chrominance
enc_Crange_L	G	C3	[7:0]	0xx	RW		
enc_chroma_max_H	G	C4	[7:0]	0x03	RW		Maximum chrominance of composite output
enc_chroma_max_L	G	C5	[7:0]	0xx	RW		
enc_chroma_min_H	G	C6	[7:0]	0x00	RW		Minimum chrominance of composite output
enc_chroma_min_L	G	C7	[7:0]	0xx	RW		

Color Kill

In low-light conditions where the IR LED is lit, the TV encoder input may be a black and white image with no color components. In this case, the TV encoder can make the chrominance range of the color burst and the active line zero in black and white mode. It can also be controlled manually.

Table 47 Register Table - Color kill

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
enc_chroma_kill	G	9D	[3]	1'b0	RW		Composite chroma signal kill enable@led on(bw mode) 1'b0 : disable 1'b1 : enable
burst kill	G	9D	[2]	1'b0	RW		Composite color burst signal kill enable@led on(bw mode) 1'b0 : disable 1b : enable
manual_chroma_kill	G	9D	[1]	1'b0	RW		Composite chroma signal manual kill enable 1'b0 : disable 1'b1 : enable
manual_burst_kill	G	9D	[0]	1'b0	RW		Composite color burst manual kill enable 1'b0 : disable 1'b1 : enable

GPO

When GPO (General Purpose Output) is used, user can output desired value to data pad.

GPO Using I2C

PC7080D can use D9 ~ D2 pad as GPO pad. To use the GPO function, the D9 to D2 pad must be enabled. If d_pad_selection is 1'b1, user can control output of D9~D2 pad by setting d9~d2_pad_manual.

Table 48 Register Table - I2C GPO control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
d9_pad_en	A	2E	[7]	1'b0	RW		D9 pad enable
d8_pad_en	A	2E	[6]	1'b0	RW		D8 pad enable
d7_pad_en	A	2E	[5]	1'b0	RW		D7 pad enable
d6_pad_en	A	2E	[4]	1'b0	RW		D6 pad enable
d5_pad_en	A	2E	[3]	1'b0	RW		D5 pad enable
d4_pad_en	A	2E	[2]	1'b0	RW		D4 pad enable
d3_pad_en	A	2E	[1]	1'b0	RW		D3 pad enable
d2_pad_en	A	2E	[0]	1'b0	RW		D2 pad enable
d9_pad_manual	A	2F	[7]	1'b0	RW		D9 pad output set 1'b1 : High 1'b0 : Low
d8_pad_manual	A	2F	[6]	1'b0	RW		D8 pad output set 1'b1 : High 1'b0 : Low
d7_pad_manual	A	2F	[5]	1'b0	RW		D7 pad output set 1'b1 : High 1'b0 : Low
d6_pad_manual	A	2F	[4]	1'b0	RW		D6 pad output set 1'b1 : High 1'b0 : Low
d5_pad_manual	A	2F	[3]	1'b0	RW		D5 pad output set 1'b1 : High 1'b0 : Low
d4_pad_manual	A	2F	[2]	1'b0	RW		D4 pad output set 1'b1 : High 1'b0 : Low
d3_pad_manual	A	2F	[1]	1'b0	RW		D3 pad output set 1'b1 : High 1'b0 : Low
d2_pad_manual	A	2F	[0]	1'b0	RW		D2 pad output set 1'b1 : High 1'b0 : Low
d_pad_selection	A	29	[0]	1'b0	RW		GPO enable 1'b0 : GPO disable 1'b1 : D9~D2 pad are correspond to d9~d2_pad_manual

Electrical Characteristics

PC7080D does not have tolerant input pads. The input signal must have HVDD power level for stable operation. If the power of input signal is higher than the recommended level, leakage current may flow via short circuit path in the input pads.

DC Characteristics

Absolute maximum ratings [1]
AVDD supply voltage : -0.3 [V] to 4.5 [V]
HVDD supply voltage : -0.3 [V] to 4.5 [V]
CVDD supply voltage : -0.3 [V] to 4.5 [V]
DVDD supply voltage(using external LDO) : -0.3 [V] to 2.5 [V]
DC voltage at any input pin : -0.3 [V] to HVDD+0.3 [V]
DC voltage at any output pin : -0.3 [V] to HVDD+0.3 [V]
Storage temperature : -40 [^{o}C] to + 125 [^{o}C]

Table 49 DC characteristics

Symbol	Descriptions	Min	Typ	Max	Unit
AVDD	Analog voltage relative to GND(AGND) level	2.97	3.3	3.63	[V]
HVDD	High VDD(HVDD) voltage relative to GND(DGND) level	2.97	3.3	3.63	[V]
CVDD	DAC VDD(CVDD) voltage relative to GND(CGND) level	2.97	3.3	3.63	[V]
DVDD	Digital VDD(DVDD) voltage relative to GND(DGND) level	1.35	1.5	1.65	[V]
I_{DDD}	HVDD=3.3 [V] @ CVBS	-	34.3	35.7	[mA]
	AVDD=3.3 [V] @ CVBS	-	9.0	9.3	
	CVDD=3.3 [V] @ CVBS	-	33.7	34.0	
	HVDD=3.3 [V] @ DVP	-	30.0	33.0	
	AVDD=3.3 [V] @ DVP	-	9.0	9.3	
	CVDD=3.3 [V] @ DVP	-	0.1	0.1	
I_{DDS}	Standby supply current	-	157.1	183.2	[uA]
V_{IL1}	Input voltage low level	-0.3	-	HVDD*0.3	[V]
V_{IH1}	Input voltage high level	HVDD*0.7	-	4	[V]
V_{IL2}	Input voltage low level for rClk, rData.	-0.3	-	HVDD*0.3	[V]
V_{IH2}	Input voltage high level for rClk, rData	HVDD*0.7	-	4	[V]
C_{IN}	Input pin capacitance	-	-	10	[pF]
V_{OL1}	Output voltage low	-	-	0.2	[V]
V_{OH1}	Output voltage high	HVDD-0.2	-	-	[V]
V_{OL2}	Output voltage low level for rClk, rData.	-	-	0.2	[V]
V_{OH2}	Output voltage high level for rData.	HVDD-0.2	-	-	[V]
I_{IN}	Input leakage current	-	0.005	1	[uA]

[1]Excessive stresses may cause permanent damage to the device.

Symbol	Descriptions	Min	Typ	Max	Unit
I_{OT}	Output leakage current	-	0.005	1	[uA]

AC Characteristics

Table 50 Digital Video Parallel output interface characteristics

Symbol	Descriptions	Min	Typ	Max	Unit
t_1	PCLK rising & falling time (load : 10pF)	0.31	0.55	0.78	ns
t_2	PCLK rising edge to VSYNC	7.88	8.35	8.81	ns
t_3	PCLK rising edge to HSYNC	8.03	8.59	9.16	ns
t_4	PCLK rising edge to DATA	8.87	9.70	10.54	ns

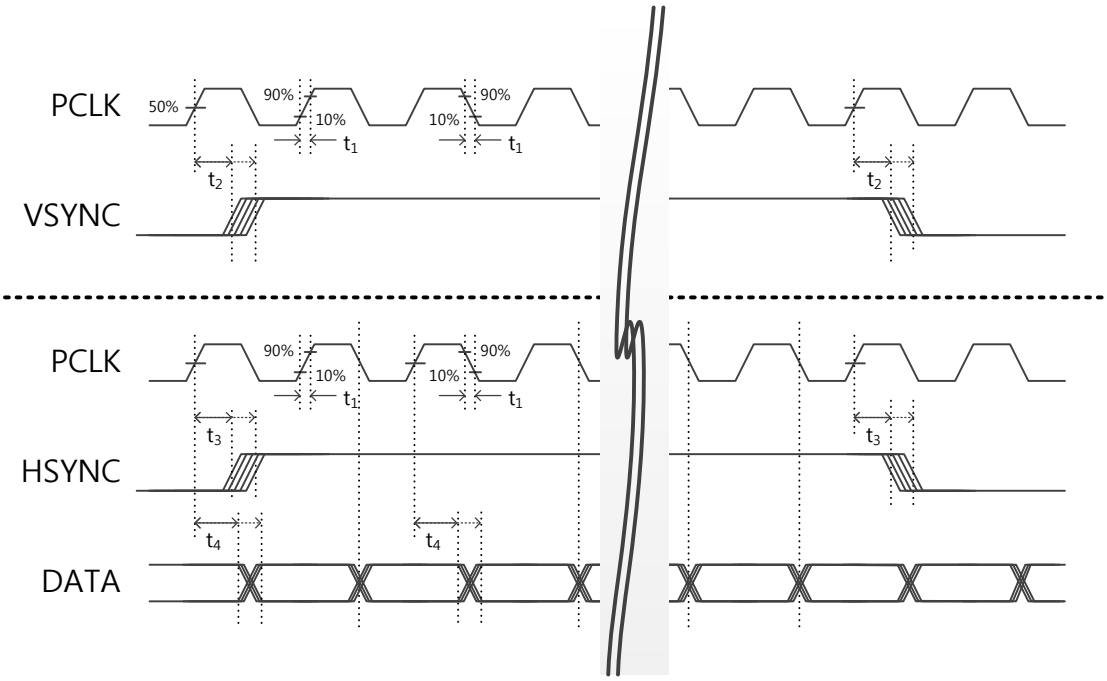


Figure 43 Timing diagram of PCLK, VSYNC, HSYNC, and DATA

test conditon : input clock = 27Mhz, AVDD/HVDD/CVDD=3.3V, using internal LDO, 25 ^{o}C

Table 51 2-wire serial interface characteristics

Symbol	Descriptions	Min	Typ	Max	Unit
f_{SCL}	2-wire serial interface Clock frequency	-	-	400	kHz
T_{ic}	2-wire serial interface Clock period	2.5	-	-	us
T_{icl}	2-wire serial interface Clock low level width	1.3	-	-	us
T_{ich}	2-wire serial interface Clock high level width	0.6	-	-	us
T_{iss}	Setup time for start condition	0.6	-	-	us
T_{ihs}	Hold time for start condition	0.6	-	-	us
T_{isd}	Setup time for input data	0.1	-	-	us
T_{ihd}	Hold time for input data	0	-	0.9	us
T_{isp}	Setup time for stop condition	0.6	-	-	us
T_{buf}	Bus free time between a stop and a new start condition	1.3	-	-	us
T_r	10% to 90% rising time for SCL/SDA (load : 10pF)	-	-	0.3	us
T_f	90% to 10% falling time for SCL/SDA (load : 10pF)	-	-	0.3	us
R_p	SCL, SDA pull-up resistor	-	2	-	kΩ

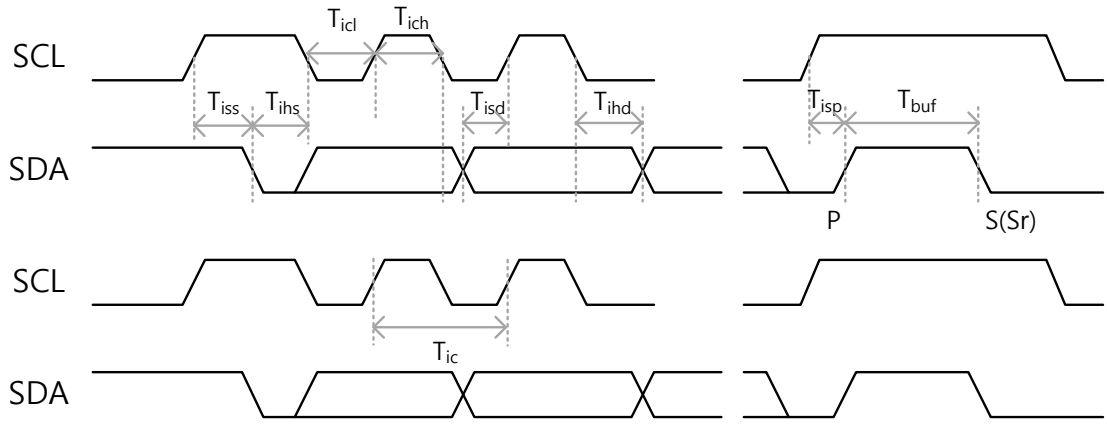


Figure 44 Timing diagram of SCL and SDA

Register Map

Table 52 Register Table - Group A

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
bank	A	03	[7:0]	0x00	RW		Register group selector
chip_mode	A	04	[1:0]	0xx	RW	aev	chip mode selection
mirror	A	05	[1:0]	0xx	RW	aev	Mirror
framewidth_h	A	06	[3:0]	0xx	RW	aev	Framewidth
framewidth_l	A	07	[7:0]	0xx	RW	aev	Framewidth
fd_fheight_a_h	A	08	[4:0]	0x02	RW	aev	Frameheight
fd_fheight_a_l	A	09	[7:0]	0xx	RW	aev	Frameheight
fd_fheight_b_h	A	0A	[4:0]	0x02	RW	aev	Frameheight
fd_fheight_b_l	A	0B	[7:0]	0xx	RW	aev	Frameheight
windowx1_h	A	0C	[1:0]	0x00	RW	aev	Window
windowx1_l	A	0D	[7:0]	0x01	RW	aev	Window
windowy1_h	A	0E	[1:0]	0x00	RW	aev	Window
windowy1_l	A	0F	[7:0]	0x01	RW	aev	Window
windowx2_h	A	10	[1:0]	0x02	RW	aev	Window
windowx2_l	A	11	[7:0]	0x80	RW	aev	Window
windowy2_h	A	12	[1:0]	0x01	RW	aev	Window
windowy2_l	A	13	[7:0]	0xE0	RW	aev	Window
vsyncstartrow_f0_h	A	14	[4:0]	0x00	RW	aev	Vsync generation
vsyncstartrow_f0_l	A	15	[7:0]	0x17	RW	aev	Vsync generation
vsyncstoprow_f0_h	A	16	[4:0]	0x01	RW	aev	Vsync generation
vsyncstoprow_f0_l	A	17	[7:0]	0xx	RW	aev	Vsync generation
vsyncstartrow_f1_h	A	18	[4:0]	0x01	RW	aev	Vsync generation
vsyncstartrow_f1_l	A	19	[7:0]	0xx	RW	aev	Vsync generation
vsyncstoprow_f1_h	A	1A	[4:0]	0x02	RW	aev	Vsync generation
vsyncstoprow_f1_l	A	1B	[7:0]	0xx	RW	aev	Vsync generation
vsynccolumn_h	A	1C	[3:0]	0x00	RW		Vsync generation
vsynccolumn_l	A	1D	[7:0]	0x02	RW		Vsync generation
clkdiv	A	25	[5:0]	0x20	RW	aev	Clock divider
strap_control	A	30	[7:0]	0xFF	RW		Strap control
flicker_control1	A	4F	[7:0]	0xx	RW		Flicker control
led_control2	A	7A	[7:0]	0x00	RW		LED control
led_control1	A	7B	[7:0]	0x00	RW		LED control
led_lvth1	A	7C	[7:0]	0x00	RW		CdS level threshold for LED control via CdS
led_lvth2	A	7D	[7:0]	0x00	RW		CdS level threshold for LED control via CdS
led_frame	A	7E	[7:0]	0x80	RW		LED control wait period in frame unit

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
led_blink_frame	A	7F	[7:0]	0x33	RW		LED blink pulse width control

Table 53 Register Table - Group B

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
bayer_control_01	B	15	[7:0]	0x11	RW		Bayer control
bayer_control_02	B	16	[7:0]	0xFA	RW		Bayer control
front_black_ref0	B	A0	[7:0]	0x82	RW		Front black fitting reference point
front_black_ref1	B	A1	[7:0]	0x82	RW		Front black fitting reference point
front_black_ref2	B	A2	[7:0]	0x82	RW		Front black fitting reference point
front_black_ref3	B	A3	[7:0]	0x00	RW		Front black fitting reference point
front_black_ref4	B	A4	[7:0]	0x02	RW		Front black fitting reference point
front_black_ref5	B	A5	[7:0]	0x02	RW		Front black fitting reference point
front_black_ref6	B	A6	[7:0]	0x02	RW		Front black fitting reference point
front_black_ref7	B	A7	[7:0]	0x02	RW		Front black fitting reference point
front_black	B	A8	[7:0]	0x00	RW	aev	Front black value
inttime_h	B	BC	[7:0]	0x01	RW	aev	Integration time (line)
inttime_m	B	BD	[7:0]	0x40	RW	aev	Integration time (line)
inttime_l	B	BE	[7:0]	0x00	RW	aev	Integration time (column)
globalgain	B	BF	[7:0]	0x00	RW	aev	Analog gain
digitalgain	B	C0	[7:0]	0x40	RW	aev	Digital gain
real_led_data	B	D7	[7:0]		RO		Current CdS data

Table 54 Register Table - Group C

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
isp_func_0	C	04	[7:0]	0xF7	RW	aev	ISP function control
isp_func_1	C	05	[7:0]	0xFF	RW	aev	ISP function control
isp_func_4	C	08	[7:0]	0x20	RW	aev	ISP function control
isp_func_6	C	0A	[7:0]	0x35	RW	aev	ISP function control
tp_control_0	C	0C	[7:0]	0x00	RW		Test pattern control
lens_scale	C	0E	[7:0]	0x51	RW		Lens shading scale control
lens_gainr	C	0F	[7:0]	0x00	RW	aev	R gain for lens shading
lens_gaing1	C	10	[7:0]	0x02	RW	aev	G1 gain for lens shading
lens_gaing2	C	11	[7:0]	0x02	RW	aev	G2 gain for lens shading
lens_gainb	C	12	[7:0]	0x00	RW	aev	B gain for lens shading
lens_x	C	13	[7:0]	0x00	RW		Lens shading center control
lens_y	C	14	[7:0]	0x00	RW		Lens shading center control
edge_gain	C	27	[7:0]	0x20	RW	aev	Edge gain value
ec_pgain	C	28	[7:0]	0x40	RW		Positive edge clamp gain
ec_mgain	C	29	[7:0]	0x80	RW		Negative edge clamp gain
ccr_m11	C	33	[7:0]	0x30	RW		Color correction matrix value
ccr_m12	C	34	[7:0]	0x8C	RW		Color correction matrix value
ccr_m13	C	35	[7:0]	0x84	RW		Color correction matrix value
ccr_m21	C	36	[7:0]	0x88	RW		Color correction matrix value
ccr_m22	C	37	[7:0]	0x34	RW		Color correction matrix value
ccr_m23	C	38	[7:0]	0x8C	RW		Color correction matrix value
ccr_m31	C	39	[7:0]	0x81	RW		Color correction matrix value
ccr_m32	C	3A	[7:0]	0x99	RW		Color correction matrix value
ccr_m33	C	3B	[7:0]	0x3A	RW		Color correction matrix value
ygm1_y0	C	3D	[7:0]	0x00	RW		Y gamma1 curve reference
ygm1_y1	C	3E	[7:0]	0x0A	RW		Y gamma1 curve reference
ygm1_y2	C	3F	[7:0]	0x18	RW		Y gamma1 curve reference
ygm1_y3	C	40	[7:0]	0x24	RW		Y gamma1 curve reference
ygm1_y4	C	41	[7:0]	0x32	RW		Y gamma1 curve reference
ygm1_y5	C	42	[7:0]	0x43	RW		Y gamma1 curve reference
ygm1_y6	C	43	[7:0]	0x4F	RW		Y gamma1 curve reference
ygm1_y7	C	44	[7:0]	0x65	RW		Y gamma1 curve reference
ygm1_y8	C	45	[7:0]	0x77	RW		Y gamma1 curve reference
ygm1_y9	C	46	[7:0]	0x95	RW		Y gamma1 curve reference
ygm1_y10	C	47	[7:0]	0xAE	RW		Y gamma1 curve reference
ygm1_y11	C	48	[7:0]	0xC5	RW		Y gamma1 curve reference
ygm1_y12	C	49	[7:0]	0xDA	RW		Y gamma1 curve reference

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ygm1_y13	C	4A	[7:0]	0xED	RW		Y gamma1 curve reference
ygm1_y14	C	4B	[7:0]	0xFF	RW		Y gamma1 curve reference
ygm2_y0	C	4C	[7:0]	0x00	RW		Y gamma2 curve reference
ygm2_y1	C	4D	[7:0]	0x1A	RW		Y gamma2 curve reference
ygm2_y2	C	4E	[7:0]	0x28	RW		Y gamma2 curve reference
ygm2_y3	C	4F	[7:0]	0x34	RW		Y gamma2 curve reference
ygm2_y4	C	50	[7:0]	0x40	RW		Y gamma2 curve reference
ygm2_y5	C	51	[7:0]	0x51	RW		Y gamma2 curve reference
ygm2_y6	C	52	[7:0]	0x60	RW		Y gamma2 curve reference
ygm2_y7	C	53	[7:0]	0x7A	RW		Y gamma2 curve reference
ygm2_y8	C	54	[7:0]	0x8E	RW		Y gamma2 curve reference
ygm2_y9	C	55	[7:0]	0xAC	RW		Y gamma2 curve reference
ygm2_y10	C	56	[7:0]	0xC3	RW		Y gamma2 curve reference
ygm2_y11	C	57	[7:0]	0xD7	RW		Y gamma2 curve reference
ygm2_y12	C	58	[7:0]	0xE6	RW		Y gamma2 curve reference
ygm2_y13	C	59	[7:0]	0xF6	RW		Y gamma2 curve reference
ygm2_y14	C	5A	[7:0]	0xFF	RW		Y gamma2 curve reference
cgm1_y0	C	5B	[7:0]	0x00	RW		RGB gamma1 curve reference
cgm1_y1	C	5C	[7:0]	0x0B	RW		RGB gamma1 curve reference
cgm1_y2	C	5D	[7:0]	0x15	RW		RGB gamma1 curve reference
cgm1_y3	C	5E	[7:0]	0x21	RW		RGB gamma1 curve reference
cgm1_y4	C	5F	[7:0]	0x2F	RW		RGB gamma1 curve reference
cgm1_y5	C	60	[7:0]	0x44	RW		RGB gamma1 curve reference
cgm1_y6	C	61	[7:0]	0x55	RW		RGB gamma1 curve reference
cgm1_y7	C	62	[7:0]	0x71	RW		RGB gamma1 curve reference
cgm1_y8	C	63	[7:0]	0x8C	RW		RGB gamma1 curve reference
cgm1_y9	C	64	[7:0]	0xB3	RW		RGB gamma1 curve reference
cgm1_y10	C	65	[7:0]	0xD0	RW		RGB gamma1 curve reference
cgm1_y11	C	66	[7:0]	0xE3	RW		RGB gamma1 curve reference
cgm1_y12	C	67	[7:0]	0xEF	RW		RGB gamma1 curve reference
cgm1_y13	C	68	[7:0]	0xFA	RW		RGB gamma1 curve reference
cgm1_y14	C	69	[7:0]	0xFF	RW		RGB gamma1 curve reference
cgm2_y0	C	6A	[7:0]	0x00	RW		RGB gamma2 curve reference
cgm2_y1	C	6B	[7:0]	0x04	RW		RGB gamma2 curve reference
cgm2_y2	C	6C	[7:0]	0x08	RW		RGB gamma2 curve reference
cgm2_y3	C	6D	[7:0]	0x0C	RW		RGB gamma2 curve reference
cgm2_y4	C	6E	[7:0]	0x10	RW		RGB gamma2 curve reference
cgm2_y5	C	6F	[7:0]	0x18	RW		RGB gamma2 curve reference

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
cgm2_y6	C	70	[7:0]	0x20	RW		RGB gamma2 curve reference
cgm2_y7	C	71	[7:0]	0x30	RW		RGB gamma2 curve reference
cgm2_y8	C	72	[7:0]	0x40	RW		RGB gamma2 curve reference
cgm2_y9	C	73	[7:0]	0x60	RW		RGB gamma2 curve reference
cgm2_y10	C	74	[7:0]	0x80	RW		RGB gamma2 curve reference
cgm2_y11	C	75	[7:0]	0xA0	RW		RGB gamma2 curve reference
cgm2_y12	C	76	[7:0]	0xC0	RW		RGB gamma2 curve reference
cgm2_y13	C	77	[7:0]	0xE0	RW		RGB gamma2 curve reference
cgm2_y14	C	78	[7:0]	0xFF	RW		RGB gamma2 curve reference
cs11	C	80	[7:0]	0x25	RW	aev	Color saturation matrix
cs12	C	81	[7:0]	0x00	RW	aev	Color saturation matrix
cs21	C	82	[7:0]	0x00	RW	aev	Color saturation matrix
cs22	C	83	[7:0]	0x25	RW	aev	Color saturation matrix
auto_off	C	8B	[7:0]	0x00	RW		Auto feature disable
y_weight	C	8D	[7:0]	0x40	RW	aev	Weight between Y gamma and RGB gamma
sync_control_0	C	9A	[7:0]	0x80	RW	aev	Sync. control
sync_control_1	C	9B	[7:0]	0x00	RW	aev	Sync. control
format	C	9E	[7:0]	0x00	RW	aev	
scale_x	C	9F	[7:0]	0x20	RW	aev	
scale_y	C	A0	[7:0]	0x20	RW	aev	
scale_th_h	C	A1	[2:0]	0x00	RW	aev	
scale_th_l	C	A2	[7:0]	0x0A	RW	aev	
ae_fwx1_h	C	B3	[1:0]	0x00	RW		AE full window X start position
ae_fwx1_l	C	B4	[7:0]	0x01	RW		AE full window X start position
ae_fwx2_h	C	B5	[1:0]	0x02	RW		AE full window X stop position
ae_fwx2_l	C	B6	[7:0]	0x80	RW		AE full window X stop position
ae_fwy1_h	C	B7	[1:0]	0x00	RW		AE full window Y start position
ae_fwy1_l	C	B8	[7:0]	0x01	RW		AE full window Y start position
ae_fwy2_h	C	B9	[1:0]	0x01	RW		AE full window Y stop position
ae_fwy2_l	C	BA	[7:0]	0xE0	RW		AE full window Y stop position
ae_cwx1_h	C	BB	[1:0]	0x00	RW		AE center window X start position
ae_cwx1_l	C	BC	[7:0]	0xD6	RW		AE center window X start position
ae_cwx2_h	C	BD	[1:0]	0x01	RW		AE center window X stop position
ae_cwx2_l	C	BE	[7:0]	0xAB	RW		AE center window X stop position
ae_cwy1_h	C	BF	[1:0]	0x00	RW		AE center window Y start position
ae_cwy1_l	C	C0	[7:0]	0xA1	RW		AE center window Y start position
ae_cwy2_h	C	C1	[1:0]	0x01	RW		AE center window Y stop position
ae_cwy2_l	C	C2	[7:0]	0x40	RW		AE center window Y stop position

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ae_xaxis_h	C	C3	[1:0]	0x01	RW		AE window X axis
ae_xaxis_l	C	C4	[7:0]	0x41	RW		AE window X axis
ae_yaxis_h	C	C5	[1:0]	0x00	RW		AE window Y axis
ae_yaxis_l	C	C6	[7:0]	0xF1	RW		AE window Y axis
awb_wx1_h	C	C7	[1:0]	0x00	RW		AWB window X start position
awb_wx1_l	C	C8	[7:0]	0x01	RW		AWB window X start position
awb_wx2_h	C	C9	[1:0]	0x02	RW		AWB window X stop position
awb_wx2_l	C	CA	[7:0]	0x80	RW		AWB window X stop position
awb_wy1_h	C	CB	[1:0]	0x00	RW		AWB window Y start position
awb_wy1_l	C	CC	[7:0]	0x01	RW		AWB window Y start position
awb_wy2_h	C	CD	[1:0]	0x01	RW		AWB window Y stop position
awb_wy2_l	C	CE	[7:0]	0xE0	RW		AWB window Y stop position

Table 55 Register Table - Group D

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
user_cs	D	13	[7:0]	0x2C	RW		User color saturation gain
wb_rgain_h	D	1B	[0]	0x00	RW	aev	White balance gain
wb_rgain_l	D	1C	[7:0]	0x5D	RW	aev	White balance gain
wb_ggain_h	D	1D	[0]	0x00	RW	aev	White balance gain
wb_ggain_l	D	1E	[7:0]	0x40	RW	aev	White balance gain
wb_bgain_h	D	1F	[0]	0x00	RW	aev	White balance gain
wb_bgain_l	D	20	[7:0]	0x5E	RW	aev	White balance gain
dark_ccr	D	4B	[7:0]	0x00	RW	aev	CCR offset
dark_y_gm	D	51	[7:0]	0x00	RW	aev	Y gamma level
dark_rgb_gm	D	55	[7:0]	0x00	RW	aev	RGB gamma level
wb_gratio	D	5B	[7:0]	0x80	RW		wb_ggain ratio
dark_ec_pth	D	68	[7:0]	0x04	RW	aev	Positive edge clamp threshold level
dark_ec_mth	D	6C	[7:0]	0x04	RW	aev	Negative edge clamp threshold level
dark_ec_pmax	D	70	[7:0]	0x7F	RW	aev	Max. positive edge clamp level
dark_ec_mmax	D	74	[7:0]	0x7F	RW	aev	Max. negative edge clamp level
dark_dc	D	7A	[7:0]	0x00	RW	aev	De-color component
y_cont_th2	D	9A	[7:0]	0x80	RW	aev	Pivot point for contrast line
y_cont_slope2	D	9E	[7:0]	0x40	RW	aev	Slope level control for contrast line

Table 56 Register Table - Group E

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
auto_control_1	E	04	[7:0]	0x98	RW	autov	Auto control
auto_control_2	E	05	[7:0]	0x65	RW	autov	Auto control
ext_inttime_h	E	22	[7:0]	0x00	RW	autov	Manual integration time @ external AE mode
ext_inttime_m	E	23	[7:0]	0x80	RW	autov	Manual integration time @ external AE mode
ext_inttime_l	E	24	[7:0]	0x00	RW	autov	Manual integration time @ external AE mode
ext_glbg_h	E	25	[7:0]	0x01	RW	autov	Manual analog gain @ external AE mode
ext_glbg_l	E	26	[7:0]	0x00	RW	autov	Manual analog gain @ external AE mode
exposure_t	E	27	[7:0]	0x00	RW	autov	Exposure value
exposure_h	E	28	[7:0]	0x01	RW	autov	Exposure value
exposure_m	E	29	[7:0]	0x40	RW	autov	Exposure value
exposure_l	E	2A	[7:0]	0x00	RW	autov	Exposure value

Table 57 Register Table - Group F

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pg_control0	F	04	[7:0]	0x09	RW	aev	Embedded parking guide line control
pg_yt	F	08	[7:0]	0x7F	RW	aev	Embedded parking guide line control
pg_y1	F	09	[7:0]	0x73	RW	aev	Embedded parking guide line control
pg_y2	F	0A	[7:0]	0x02	RW	aev	Embedded parking guide line control
pg_y3	F	0B	[7:0]	0x08	RW	aev	Embedded parking guide line control
pg_y4	F	0C	[7:0]	0x0F	RW	aev	Embedded parking guide line control
pg_y5	F	0D	[7:0]	0x19	RW	aev	Embedded parking guide line control
pg_y6	F	0E	[7:0]	0x25	RW	aev	Embedded parking guide line control
pg_y7	F	0F	[7:0]	0x28	RW	aev	Embedded parking guide line control
pg_y8	F	10	[7:0]	0x38	RW	aev	Embedded parking guide line control
pg_y9	F	11	[7:0]	0x4E	RW	aev	Embedded parking guide line control
pg_y10	F	12	[7:0]	0x52	RW	aev	Embedded parking guide line control
pg_a	F	13	[7:0]	0x8F	RW	aev	Embedded parking guide line control
pg_b	F	14	[7:0]	0x64	RW	aev	Embedded parking guide line control
pg_c	F	15	[7:0]	0xBF	RW	aev	Embedded parking guide line control
pg_d	F	16	[7:0]	0x07	RW	aev	Embedded parking guide line control
pg_e	F	17	[7:0]	0x0C	RW	aev	Embedded parking guide line control
pg_f	F	18	[7:0]	0x15	RW	aev	Embedded parking guide line control
pg_line1	F	19	[7:0]	0x21	RW	aev	Embedded parking guide line control
pg_line2	F	1A	[7:0]	0x23	RW	aev	Embedded parking guide line control
pg_line3	F	1B	[7:0]	0x24	RW	aev	Embedded parking guide line control
pg_line4	F	1C	[7:0]	0x46	RW	aev	Embedded parking guide line control
pg_line5	F	1D	[7:0]	0x48	RW	aev	Embedded parking guide line control
pg_line6	F	1E	[7:0]	0x42	RW	aev	Embedded parking guide line control
pg_line7	F	1F	[7:0]	0x4B	RW	aev	Embedded parking guide line control
pg_line8	F	20	[7:0]	0x71	RW	aev	Embedded parking guide line control
pg_line9	F	21	[7:0]	0x63	RW	aev	Embedded parking guide line control
pg_line10	F	22	[7:0]	0x74	RW	aev	Embedded parking guide line control
pg_center_h	F	23	[1:0]	0x01	RW	aev	Embedded parking guide line control
pg_center_l	F	24	[7:0]	0x68	RW	aev	Embedded parking guide line control
pg_hl_en_h	F	27	[1:0]	0x00	RW	aev	Embedded parking guide line control
pg_hl_en_l	F	28	[7:0]	0x00	RW	aev	Embedded parking guide line control
sif_state	F	D3	[7:0]		RO		SIF state monitor

Table 58 Register Table - Group G

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
sync_blankEAV_f0	G	04	[7:0]	0xB6	RW		Blank EAV for field 0 data
sync_blankSAV_f0	G	05	[7:0]	0xAB	RW		Blank SAV for field 0 data
sync_activeEAV_f0	G	06	[7:0]	0x9D	RW		Active EAV for field 0 data
sync_activeSAV_f0	G	07	[7:0]	0x80	RW		Active SAV for field 0 data
sync_blankEAV_f1	G	08	[7:0]	0xF1	RW		Blank EAV for field 01 data
sync_blankSAV_f1	G	09	[7:0]	0xEC	RW		Blank SAV for field 01 data
sync_activeEAV_f1	G	0A	[7:0]	0xDA	RW		Active EAV for field 01 data
sync_activeSAV_f1	G	0B	[7:0]	0xC7	RW		Active SAV for field 01 data
sync_CCIR_FF	G	0C	[7:0]	0xFF	RW		CCIR656 blank data format
sync_CCIR_00	G	0D	[7:0]	0x00	RW		CCIR656 blank data format
sync_CCIR_80	G	0E	[7:0]	0x80	RW		CCIR656 blank data format
sync_CCIR_10	G	0F	[7:0]	0x10	RW		CCIR656 blank data format
osd_opac3	G	18	[4:0]	0x10	RW		OSD layer3 transparency
palette_1_y	G	1A	[7:0]	0x90	RW		Palette set0 palette 1
palette_1_cb	G	1B	[7:0]	0x35	RW		Palette set0 palette 1
palette_1_cr	G	1C	[7:0]	0x22	RW		Palette set0 palette 1
palette_2_y	G	1D	[7:0]	0xD2	RW		Palette set0 palette 2
palette_2_cb	G	1E	[7:0]	0x10	RW		Palette set0 palette 2
palette_2_cr	G	1F	[7:0]	0x92	RW		Palette set0 palette 2
palette_3_y	G	20	[7:0]	0x51	RW		Palette set0 palette 3
palette_3_cb	G	21	[7:0]	0x5A	RW		Palette set0 palette 3
palette_3_cr	G	22	[7:0]	0xF0	RW		Palette set0 palette 3
palette_4_y	G	23	[7:0]	0x10	RW		Palette set0 palette 4
palette_4_cb	G	24	[7:0]	0x80	RW		Palette set0 palette 4
palette_4_cr	G	25	[7:0]	0x80	RW		Palette set0 palette 4
osd_efld_s_h	G	32	[1:0]	0x00	RW	aev	OSD even field start
osd_efld_s_l	G	33	[7:0]	0x01	RW	aev	OSD even field start
osd_ofld_s_h	G	34	[1:0]	0x01	RW	aev	OSD odd field start
osd_ofld_s_l	G	35	[7:0]	0x0A	RW	aev	OSD odd field start
enc_control1	G	9D	[7:0]	0x00	RW		Encoder control
setup_w	G	A9	[4:0]	0x07	RW		Setup time width
sync_rising	G	AF	[3:0]	0x01	RW		Horizontal sync rising(falling) time control
enc_mode	G	B7	[1:0]	0xx	RW		Encoder mode
enc_sync	G	B8	[7:0]	0x10	RW		Composite sync level
enc_blankH	G	B9	[7:0]	0x00	RW		Composite blank level
enc_blankL	G	BA	[7:0]	0xx	RW		Composite blank level
enc_pedestal	G	BB	[7:0]	0xx	RW		Composite pedestal level

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
enc_burst	G	BC	[7:0]	0xx	RW		Burst amplitude
enc_Ygain	G	BD	[7:0]	0xx	RW		Y convergence gain from YCbCr to YUV
enc_Ugain	G	BE	[7:0]	0xx	RW		U convergence gain from YCbCr to YUV
enc_Vgain	G	BF	[7:0]	0xx	RW		V convergence gain from YCbCr to YUV
enc_Yrange_H	G	C0	[7:0]	0x03	RW		Max. luminance
enc_Yrange_L	G	C1	[7:0]	0x20	RW		Max. luminance
enc_Crange_H	G	C2	[7:0]	0x01	RW		Max. amplitudes of chrominance
enc_Crange_L	G	C3	[7:0]	0xx	RW		Max. amplitudes of chrominance
enc_chroma_max_H	G	C4	[7:0]	0x03	RW		Max. chrominance of composite output
enc_chroma_max_L	G	C5	[7:0]	0xx	RW		Max. chrominance of composite output
enc_chroma_min_H	G	C6	[7:0]	0x00	RW		Min. chrominance of composite output
enc_chroma_min_L	G	C7	[7:0]	0xx	RW		Min. chrominance of composite output
DAC_tp_period	G	E5	[7:0]	0x00	RW		DAC test pattern period
encdat_rising	G	EB	[3:0]	0x01	RW		Rising time control of the line blank pulse

Table 59 Register Table - Control Register

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
i2c_control_1	A	23	[7:4]	4'b0101	RW		updatecontrol[3:0] control i2c register update by auto_vsync update_autov <= reg_updatecontrol(3) or (autov_update and reg_updatecontrol(2)) control i2c register update by ae_vsync update_aev <= reg_updatecontrol(1) or (aev_update and reg_updatecontrol(0))
clkdiv	A	25	[5]	1'b1	RW	aev	pclk_div pclk divider 1'b0 : x1/2 1'b1 : x1
	A	25	[1:0]	2'b00	RW	aev	ppclk_div ppclk divider 2'b00 or 2'b11 : x1 2'b01 : x1/2 2'b10 : x1/4
pad_control3	A	29	[7]	1'b0	RW		vsync_pad_en VSYNC pad enable
	A	29	[4]	1'b0	RW		hsync_pad_en HSYNC pad enable
	A	29	[3]	1'b0	RW		d1_pad_en D1 pad enable
	A	29	[2]	1'b0	RW		d0_pad_en D0 pad enable
	A	29	[1]	1'b0	RW		hsync_pad_selection HSYNC pad selection 1'b0: hsync 1'b1: LED signal
	A	29	[0]	1'b0	RW		d_pad_selection D9~D2 pad manual mode enable 1'b0 : GPO disable 1'b1 : D9~D2 pad are correspond to d9~d2_pad_manual
pad_control4	A	2A	[7]	1'b0	RW		ledctrl_en IRLED pad enable 1'b0: disable 1'b1: enable
pad_control7	A	2D	[0]	1'b0	RW		strap_smp latch stores strap information when strap_smp=*0*
pad_control8	A	2E	[7]	1'b0	RW		strap_smp latch stores strap information when strap_smp=*1*
	A	2E	[6]	1'b0	RW		d8_pad_en D8 pad enable
	A	2E	[5]	1'b0	RW		d7_pad_en D7 pad enable
	A	2E	[4]	1'b0	RW		d6_pad_en D6 pad enable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
	A	2E	[3]	1'b0	RW		d5_pad_en D5 pad enable
	A	2E	[2]	1'b0	RW		d4_pad_en D4 pad enable
	A	2E	[1]	1'b0	RW		d3_pad_en D3 pad enable
	A	2E	[0]	1'b0	RW		d2_pad_en D2 pad enable
pad_control9	A	2F	[7]	1'b0	RW		d9_pad_manual D9 pad level control @ d_pad_selection = 1b
	A	2F	[6]	1'b0	RW		d8_pad_manual D8 pad level control @ d_pad_selection = 1b
	A	2F	[5]	1'b0	RW		d7_pad_manual D7 pad level control @ d_pad_selection = 1b
	A	2F	[4]	1'b0	RW		d6_pad_manual D6 pad level control @ d_pad_selection = 1b
	A	2F	[3]	1'b0	RW		d5_pad_manual D5 pad level control @ d_pad_selection = 1b
	A	2F	[2]	1'b0	RW		d4_pad_manual D4 pad level control @ d_pad_selection = 1b
	A	2F	[1]	1'b0	RW		d3_pad_manual D3 pad level control @ d_pad_selection = 1b
	A	2F	[0]	1'b0	RW		d2_pad_manual D2 pad level control @ d_pad_selection = 1b
flicker_control1	A	4F	[6]	1'b0	RW		fd_en flicker enable
	A	4F	[3]	1'b0	RW		manual_A manual_A
	A	4F	[2]	1'b0	RW		manual_B manual_B
led_control2	A	7A	[7]	1'b0	RW		ledblnk en led blink enable 0b : disable 1b : enable
	A	7A	[6]	1'b0	RW		ledblnk manual led blink output value @ led blink disable
	A	7A	[5]	1'b0	RW		ledblnk polarity led blink output polarity change enable 0b : disable 1b : enable
	A	7A	[4]	1'b0	RW		ledblnk selection led blink output selection 0b : led blink output 1b : led output
led_control1	A	7B	[7]	1'b0	RW		ledctl en led control enable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							0b : disable 1b : enable
	A	7B	[6]	1'b0	RW		ledctl manual led output value @ led control disable
	A	7B	[5]	1'b0	RW		ledctl polarity led output polarity change enable 0b : disable 1b : enable
	A	7B	[4]	1'b0	RW		bwled en black & white mode @ led on enable 0b : disable 1b : enable
	A	7B	[3]	1'b0	RW		ledctl selection led output selection 0b : led output 1b : led blink output
	A	7B	[0]	1'b0	RW		exrom_set_en enable setting from external rom @ led on/off 0b: disable 1b: enable
bayer_control_01	B	15	[6]	1'b0	RW		frmvar_en frame rate varying enable
	B	15	[1:0]	2'b01	RW		led_dsel[1:0] led data selection
bayer_control_02	B	16	[2]	1'b0	RW		inv_led led data inverting enable
isp_func_0	C	04	[7]	1'b1	RW	aev	lens_en lens shading compensation enable 0b : disable 1b : enable
	C	04	[6]	1'b1	RW	aev	awb_en awb gain multification enable 0b : disable 1b : enable
	C	04	[1]	1'b1	RW	aev	ccr_en color correction enable 0b : disable 1b : enable
	C	04	[0]	1'b1	RW	aev	ccr_lpf color correction input selection 0b : normal 1b : low pass filtering
isp_func_1	C	05	[7]	1'b1	RW	aev	rgbgm_en rgb gamma enable 0b : disable 1b : enable
	C	05	[6]	1'b1	RW	aev	ygm_en y gamma enable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							0b : disable 1b : enable
	C	05	[3]	1'b1	RW	aev	edge_en edge enhancement enable 0b : disable 1b : enable
isp_func_4	C	08	[7:6]	2'b00	RW	aev	win_show[1:0] win_show[1] : ae window show enable 0b : disable 1b : enable win_show[0] : awb window show enable 0b : disable 1b : enable
isp_func_6	C	0A	[2]	1'b1	RW	aev	dc_en de-color enable 0b : disable 1b : enable
sync_control_0	C	9A	[6:5]	2'b00	RW	aev	sync_drop[1:0] 0 : disable 1 : hsync drop 2 : vsync drop 3 : hsync and vsync drop
sync_control_1	C	9B	[6]	1'b0	RW	aev	sync_vsyncPolarity vsync polarity change
	C	9B	[5]	1'b0	RW	aev	sync_hsyncAllLines hsync output all lines enable(black and active)
	C	9B	[4]	1'b0	RW	aev	sync_hsyncPolarity hsync polarity change
	C	9B	[2]	1'b0	RW	aev	sync_pclkPolarity pclk polarity change
auto_control_1	E	04	[2]	1'b0	RW	au-tov	wb mode white blance mode selection 0b : auto mode 1b : manual mode
	E	04	[1:0]	2'b00	RW	au-tov	exposure mode exposue mode selection 00b : auto mode 01b : manual mode (expsoure write) 10b : manual mode (ext_inttime, ext_glbgain write) 11b : manual mode (inttime, globalgain write)
auto_control_2	E	05	[3]	1'b0	RW	au-tov	fb gg globalgian selection @ front_black fitting 0b : high sensitivity conversion gain 1b : normal gain
pg_control0	F	04	[5]	1'b0	RW	aev	pg_f_div dividing pg field(even,odd) 0b: not dividing 1b: dividing field(even,odd)
	F	04	[4]	1'b0	RW	aev	pg_hlight

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							all pg hlight enable
	F	04	[3]	1'b1	RW	aev	pg_rm_ych remove yochul line of PG
	F	04	[2:1]	2'b00	RW	aev	pg_rm remove left side of PG
	F	04	[0]	1'b1	RW	aev	pg_enable pg enable
enc_control1	G	9D	[3]	1'b0	RW		enc_chroma_kill TV encoder chroma signal kill enable@led ON(BW_mode) 0b : disable 1b : enable
	G	9D	[2]	1'b0	RW		burst kill TV encoder color burst kill enable@led ON(BW_mode) 0b : disable 1b : enable
	G	9D	[1]	1'b0	RW		manual_chroma_kill TV encoder chroma signal manual kill enable 0b : disable 1b : enable
	G	9D	[0]	1'b0	RW		manual_burst_kill TV encoder color burst manual kill enable 0b : disable 1b : enable

Revision History

Version	Date [D/M/Y]	Notes	Writer
0.0	21/06/2018	(Preliminary)	Yeari Seo
0.1	06/09/2018	Fill in the electrical sepc and typical parameter	SangHyun Han
0.2	26/02/2019	Update to Key Performance Parameter	ByungGwan Park
0.3	20/05/2019	Update to Key Performance Parameter Digital parallel data pad, i2c usage related comment	Kibbeum Kim
0.4	23/05/2019	Delete i2c usage related comment pad_drv register description	Kibbeum Kim
0.5	22/06/2020	• Update Key Performance Parameter - P.8 – Operating Temp. • Update Frame Structure - P.10 – Default frame structure	Jaedong Park
0.6	10/07/2020	• Update DC characteristics. - P.68 – Table format • Update AC characteristics. - P.69 – Table format • Update Register Map. – modified pad_drv register description	Jaedong Park
0.7	17/12/2020	• Update General Description. - P.8 – 40PLCC	Jaedong Park
0.8	23/04/2021	• Update LED Control. - P.38 • Update Register Map. - P.85 – Register • Update AC characteristics. - P.69	Jaedong Park
0.9	14/05/2021	• Update AC characteristics. - P.69	Jaedong Park
1.0	08/07/2021	• Update General Description. - P.7~8 – Power consumption • Update DC Characteristics. - P.68~69 – IDDD	Jaedong Park
1.1	11/11/2021	• Update Initialization. - P.27 • Update AC Characteristics. - P.71 – I2C timing	Jaedong Park