Himax Imaging, Inc.

DATA SHEET

(DOC No. HM2140-DS)

HM2140

1/4″ FHD 1080p 30FPS CMOS Image Sensor

Version 05 November, 2018

Himax Imaging, Inc.

HM2140 UltraSense™ BSI

1/4″ FHD 1080p 30FPS CMOS Image Sensor

Himax Imaging, Inc.
http://www.himax.com.tw

November, 2018

Features

- Back Side Illuminated **(BSI)** pixel delivers outstanding sensitivity, response uniformity and noise performance.
- Design for low power consumption at 30 frames per second **(FPS)**
- Operates up to 30FPS at full resolution and up to 60FPS in sub-sample over MIPI interface and Parallel interface.
- Global analog gain up to 15.5x
- Single lane MIPI CSI-2 supports RAW10 format
- Precision black level calibration independent of operation temperature, gain and voltage
- On-chip temperature sensor
- Support SSCG on MIPI DPHY
- Available in CSP package
- Support 3D SYNC for image synchronization
- Integrated LDO, POR and PLL

Key Parameters

Sensor parameters	Value
Pixel array **(Full / Active)**	1928 x 1088 / 1920 x 1080
Pixel size	2µm x 2µm
Full image area	3856µm x 2176µm
Diagonal **(Optical Format)**	4.42mm **(1/4")**
Color filter array	Bayer
Scan mode	Progressive
Shutter type	Electronic rolling shutter
Frame rate	30FPS @1080P MIPI RAW10
	30FPS @1080P Parallel RAW10
Analog gain **(Max.)**	15.5x
S/N ratio **(Max.)**	36.7 dB
Dynamic range **(8 x gain**)	63dB
Sensitivity @ 530nm	1650 mV/lux.sec
CRA **(Max.)**	18°

General parameters		Value
Supply voltage	Analog	3.0-3.6 V **(3.3V Typ.)**
	Digital	Bypass LDO: 1.08-1.32 V **(1.2V Typ.)**
		Internal LDO: 1.7-3.6 V **(1.8V Typ.)**
	I/O	1.7-3.6 V **(1.8 Typ.)**
Input reference clock		6 - 27 MHz
Serial interface **(I2C)**		2-Wire, 400kHz **(Max.)**
Video data interface		1-lane MIPI CSI-2 10-bit Parallel
Output format		10-bit Raw for MIPI 10-bit Raw for Parallel
Power consumption		30FPS @1080P MIPI **(Typ.)** 89.5 mW 30FPS @1080P Parallel **(Typ.)** 94.7 mW
		SHUTDOWN **(Typ.)** 0.24µW

Order Information

Part no.	CFA	Package type
HM2140-AWA	Bayer **(Color)**	CSP

Revision History

November, 2018

Version	Date	Description of changes
01	2017/02/06	New setup.
02	2017/07/03	Page 2 1. Modify 'Features'. Page 25 2. Remove CH '5.5 Total gain control'. 3. Remove CH '5.6 Streaming control'.
	2017/11/06	All pages 1. Modify CIS technology from Back Side Illuminated **(BSI)** to Through Silicon Illumination **(TSI)**. Page 2 2. Modify 'Features'. 3. Modify 'Key Parameters'. Page 11. 4. Modify 'Table 2.1: CSP pin description'. Page 24 5. Modify CH '5.3 Analog gain control'. Page 25 6. Add CH '5.5 Total gain control'. 7. Add CH '5.6 Streaming control'. Page 45 8. Modify CH '11.3 DC characteristics'
03	2017/12/28	Page 2 1. Modify 'Key Parameters'. Page 16 2. Modify 'Table 3.1: Window horizontal (x) and vertical (y) address programming constraints'. 3. Modify 'Table 3.2: Sub-sampling registers' Page 19 4. Modify CH '4.3 Black level (data pedestal) control'. Page 23 5. Modify CH '5.1 Clock generation'. Page 26 6. Modify 'Table 6.1: MIPI control registers'. Page 35 7. Modify 'Table 9.3: Power-up sequence timing (XSHUTDOWN)'. Page 37~43 8. Modify CH '10. Register Table'.
04	2018/07/30	All pages 1. Remove 'preliminary' wording. 2. Modify CIS technology from Through Silicon Illumination **(TSI)** to Back Side Illuminated **(BSI)**. Page 46 3. Modify 'Table 11.5: MIPI timing characteristics'. Page 47 4. Modify 'Table 11.7: Parallel interface timing characteristics'. Page 50 5. Add CH '13. Quantum Efficiency'.
05	2018/11/27	Page 12 1. Modify 'Table 2.1: CSP pin description'. **(ID_SEL: Remove "Internal pulling low" wording.)**

Revision History

November, 2018

Version	Date	Description of changes
		Page 46 2. Modify 'Table 11.3: DC characteristic'. Page 48 3. Modify 'Table 11.7: Parallel interface timing characteristic'.

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Disclaimer

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1. Sensor Overview

The HM2140 is a low power Full High Definition **(FHD)** CMOS Image Sensor which employs advanced 2μm UltraSense™ BSI pixel that delivers excellent low light sensitivity, uniformity and crosstalk performance. The sensor has an active array of 1920 x1080 and operates up to 30 frames per second **(FPS**).

The sensor is available in extremely small Chip Scale Package **(CSP)** allowing camera modules to be designed as small as possible.

The sensor operates up to 30FPS over 1-lane MIPI CSI-2 interface and up to 30FPS over 10-bit parallel interface. All sensor parameters can be programmed and accessed through standard serial interface.

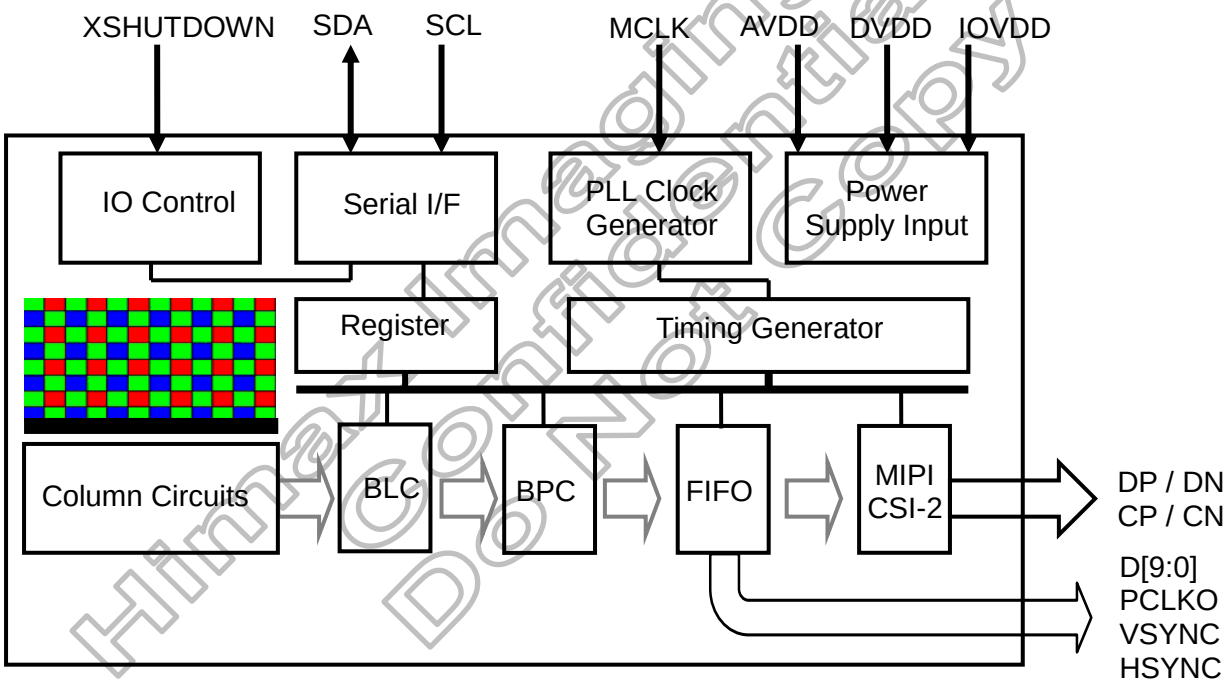


Figure 1.1: HM2140 block diagram

2. Package Information

2.1 CSP pin assignment

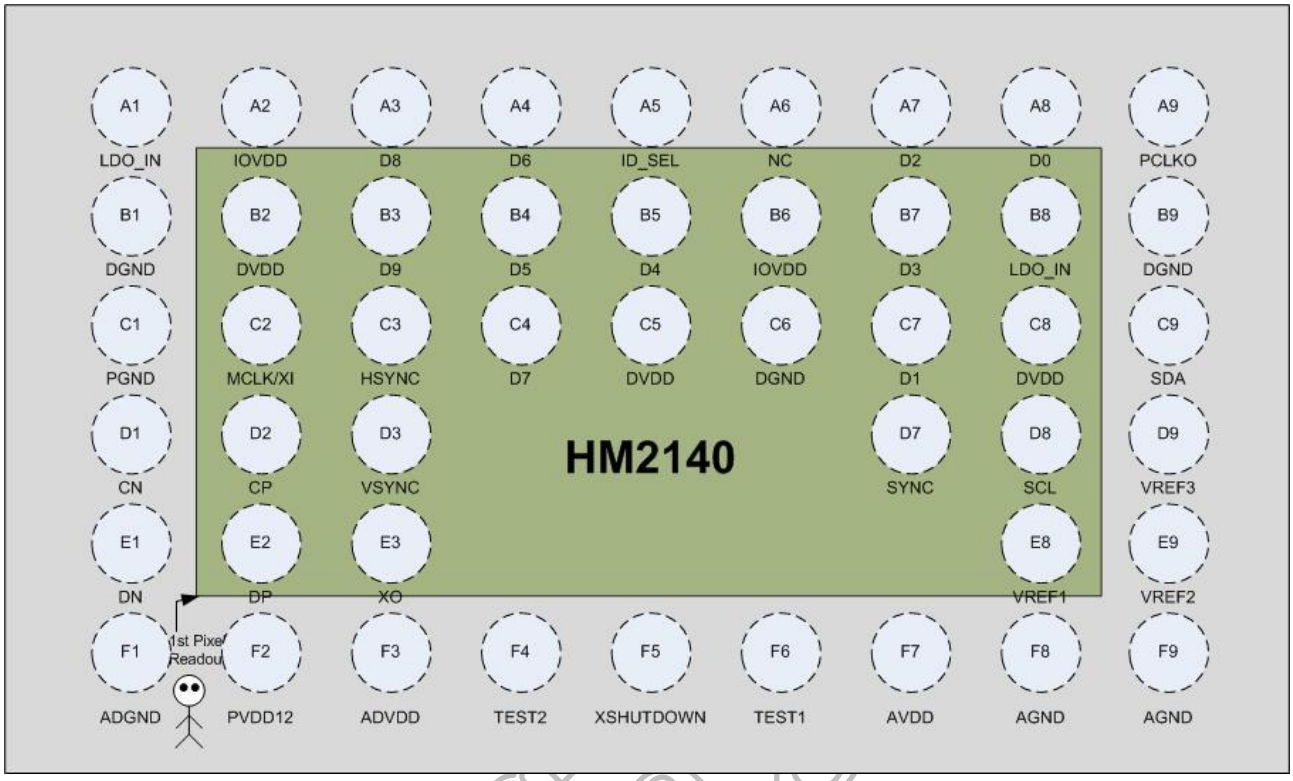


Figure 2.1: CSP pin assignment (Top view)

2.2 CSP pin description

Pin no.	Pad name	Type	Description
A1	LDO_IN	Power	If using bypass mode. LDO: 1.2V; Otherwise LDO: 1.7V~3.6V.
A2	IOVDD	Power	I/O power. **(1.8V / 3.3V)**
A3	D8	Out	Video data output.
A4	D6	Out	Video data output.
A5	ID_SEL	In	I2C Device Address selection. Low: Address=0x24 **(7-bit)**, High: Address=0x34 **(7-bit).**
A6	NC	-	No connection.
A7	D2	Out	Video data output.
A8	D0	Out	Video data output.
A9	PCLKO	Out	Pixel clock output.
B1	DGND	Ground	Digital ground.
B2	DVDD	Power	Digital power. **(1.2V)**
B3	D9	Out	Video data output.
B4	D5	Out	Video data output.
B5	D4	Out	Video data output.
B6	IOVDD	Power	I/O power. **(1.8V / 3.3V)**
B7	D3	Out	Video data output.
B8	LDO_IN	Power	If using bypass mode, LDO: 1.2V. Otherwise LDO: 1.7V~3.6V
B9	DGND	Ground	Digital ground.
C1	PGND	Ground	MIPI ground.
C2	MCLK/XI	In	Master clock input. This pin can be connected to an oscillator **(In this case, XO is connected to IOVDD)** or connected to a crystal.
C3	HSYNC	Out	Horizontal sync output.
C4	D7	Out	Video data output.
C5	DVDD	Power	Digital power. **(1.2V)**
C6	DGND	Ground	Digital ground.
C7	D1	Out	Video data output.
C8	DVDD	Power	Digital power. **(1.2V)**
C9	SDA	In/Out	Serial data bus. **(Open Drain)(I2C)**
D1	CN	Out	MIPI clock negative output.
D2	CP	Out	MIPI clock positive output.
D3	VSYNC	Out	Vertical sync output.
D7	SYNC	In/Out	3D sync input / sync output.
D8	SCL	In	Serial clock input. **(I2C)**
D9	VREF3	Reference	Voltage reference.
E1	DN	Out	MIPI data negative output
E2	DP	Out	MIPI data positive output
E3	XO	Out	If MCLK/XI is connected to an oscillator, this pin should be connected to IOVDD. Otherwise, this pin should be connected to the other pin of crystal.
E8	VREF1	Reference	Voltage reference.
E9	VREF2	Reference	Voltage reference.
F1	ADGND	Ground	Analog ground.
F2	PVDD12	Power	MIPI power. **(1.2V)**
F3	ADVDD	Power	Analog power. **(3.3V)**
F4	TEST2	Out	No connection. **(It must be floating)**
F5	XSHUTDOWN	In	Reset and power down control pin. **(Active low)**
F6	TEST1	Out	No connection. **(It must be floating)**
F7	AVDD	Power	Analog power. **(3.3V)**
F8	AGND	Ground	Analog ground.
F9	AGND	Ground	Analog ground.

Table 2.1: CSP pin description

3. Sensor Core Description

3.1 Sensor array

The HM2140 has an active pixel array of 1920 x 1080, and image array of 1928 x 1088. The even numbered rows contain the Blue **(B)** and Green **(G_1)** pixel, and the odd numbered row contains the Red **(R)** and Green **(G_2)** pixels. The even numbered columns contain the Green **(G_2)** and Blue **(B)** pixels, and the odd column contains the Red **(R)** and Green **(G_1)** pixels. There are 12 black rows used by the sensor for black level calibration. Programmable horizontal and vertical blanking time adjusts the line width and frame height, respectively.

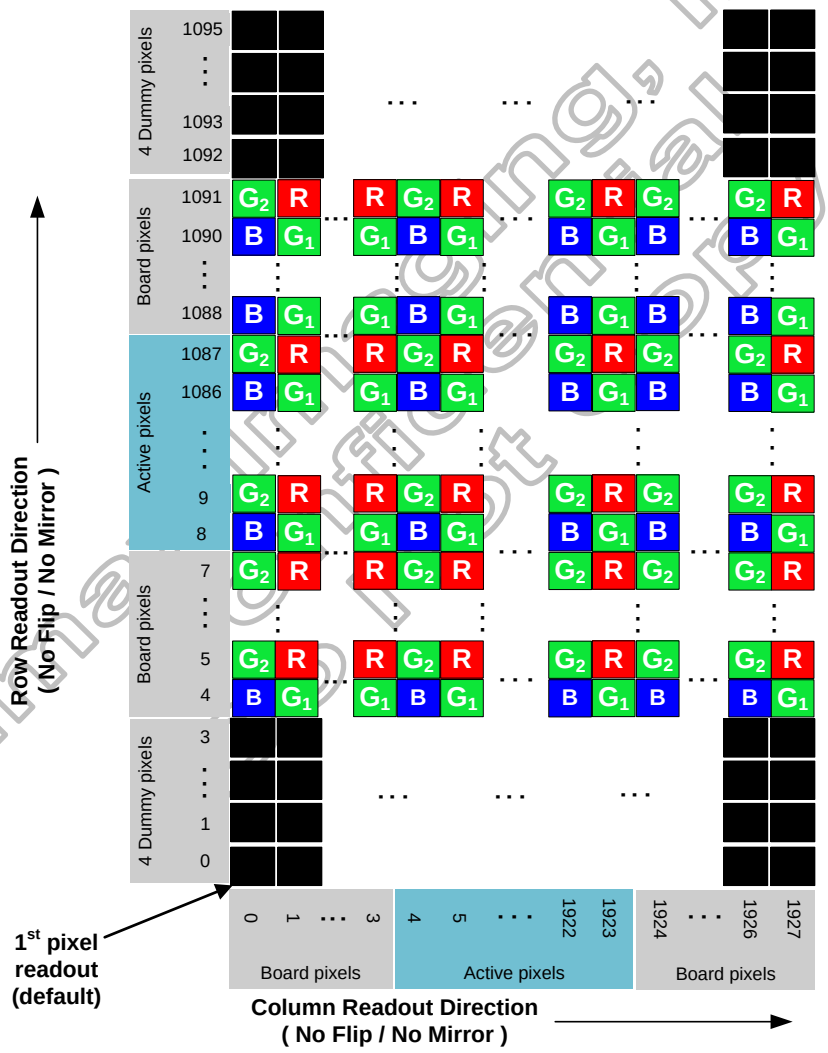


Figure 3.1: Full resolution pixel readout

The optical center of the sensor array is set to the center of the visible pixel **(Active + Dummy)**. The frame center can be aligned to the optical center by maintaining the same number of cropped pixels on all four sides of the frame.

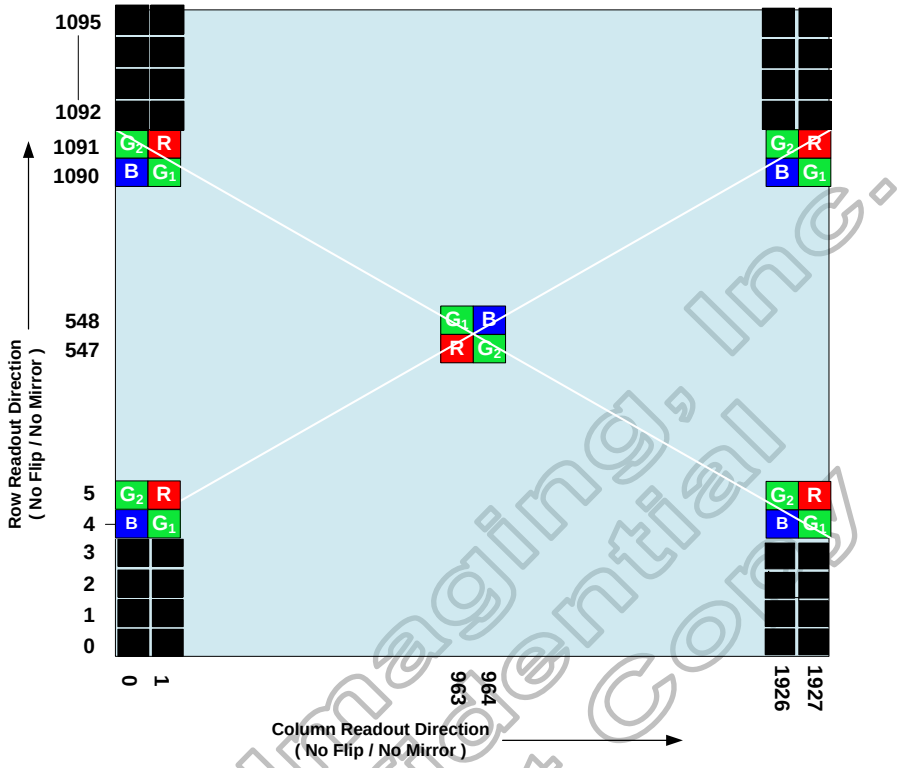


Figure 3.2: Optical center

3.2 Horizontal mirror and vertical flip readout

The sensor readout can be mirrored in the horizontal direction and flipped in the vertical direction

- In vertical flip readout mode, the rows are readout in reverse order, which will result in the appearance of the image being flipped upside down.
- In vertical flip readout mode, it will duplicate last two columns and skip the first column to let the first pixel be blue.
- In horizontal mirror readout mode, the columns are readout in reverse order, which will result in the appearance of the image being flipped along the vertical axis.
- In horizontal mirror readout mode, it will duplicate last two rows and skip the first row to let the first pixel be blue.
- Horizontal and vertical mirror readout can be used in all readout modes.
- Using digital window crop 1928 x 1088 output same color for normal, mirror and flip or both.

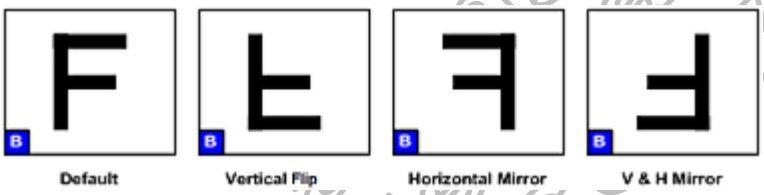


Figure 3.3: Horizontal mirror and vertical flip readout mode

3.3 Sub-sampling readout

Row and column Sub-sampling can be used to reduce the sensor resolution while preserving the field of view.

- The sensor can perform 4:2 Sub-sampling independently in the vertical and horizontal direction.
- In order to preserve the native 16:9 aspect ratio of the imager, the number of rows skipped should equal the number of columns skipped.

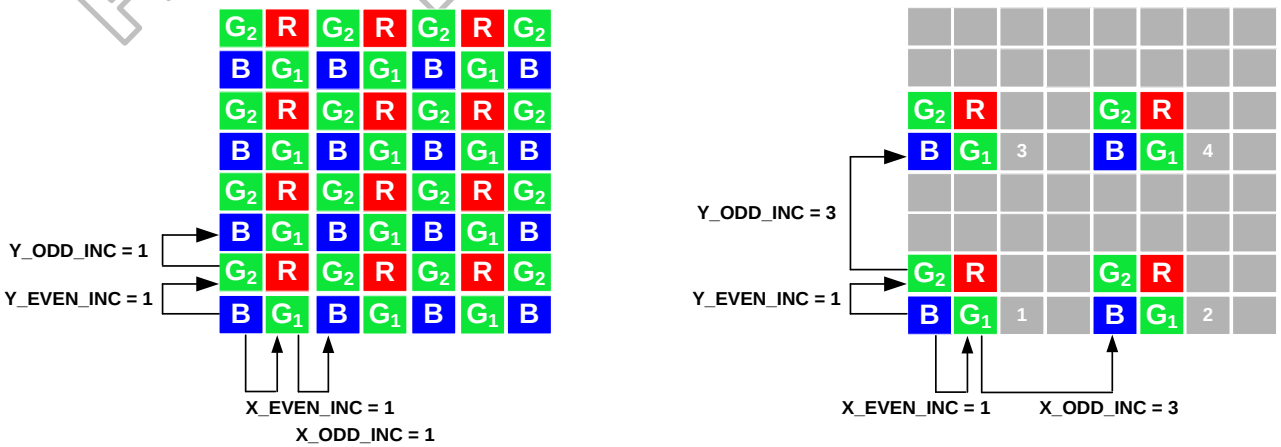


Figure 3.4: Sub-sampling 4:2

3.4 Window readout

The sensor window can be set by specifying the row starting address **(Y_ADDR_START)**, row ending address **(Y_ADDR_END)**, column starting address **(X_ADDR_START)**, and column ending address **(X_ADDR_END)**. The visible pixels of the window readout are programmed by setting the X_OUTPUT_SIZE_H, X_OUTPUT_SIZE_L and Y_OUTPUT_SIZE_H, Y_OUTPUT_SIZE_L register.

In Sub-sampling 4:2 mode, the row and column ending address should be reduced by two pixels, and the output size should follow the equation shown in Figure 3.5.

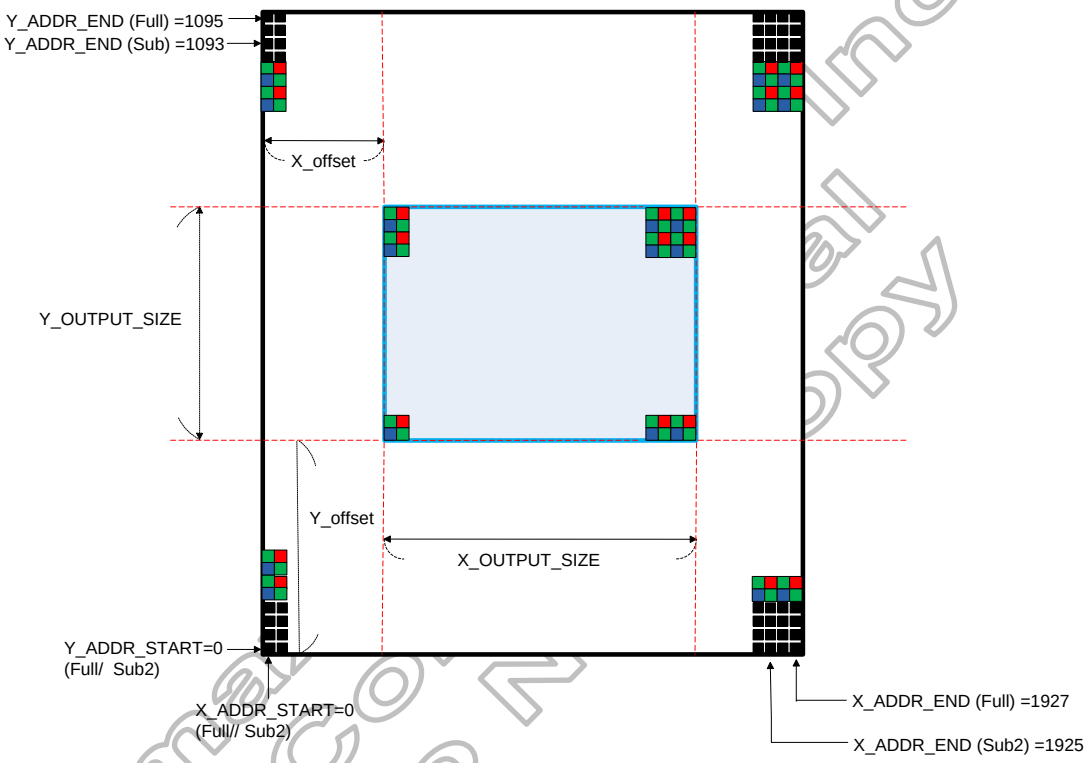


Figure 3.5: Window readout for Sub-sampling 4:2

3.4.1 Digital window

Digital window adjusts the frame output to an arbitrary size and location without change to the frame timing. The window size is programmed by specifying x **(Horizontal)** and y **(Vertical)** starting and size.

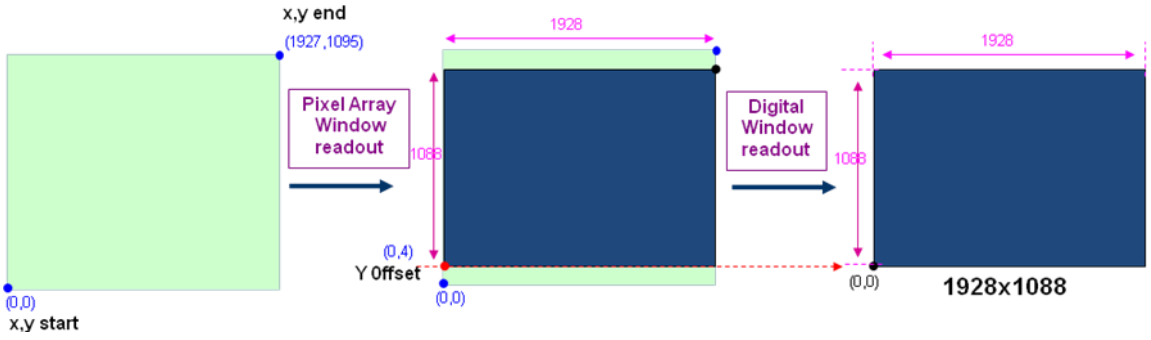


Figure 3.6: Spatial illustration of default digital window readout

3.4.2 Window readout programming constraint

The starting and ending address of the window is required to follow the programming constraints in Table 3.1.

A. x_skip_factor = (x_odd_inc + x_even_inc) / 2

B. y_skip_factor = (y_odd_inc + x_even_inc) / 2

x_addr_start/y_address_start should be a multiple of x_skip_factor * 4
(x_addr_end - x_addr_start + x_odd_inc) should be a multiple of x_skip_factor * 4
(y_addr_end - y_addr_start + y_odd_inc) should be a multiple of y_skip_factor * 4

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0344	[3:0]	X_ADDR_START_H	RW	x_addr_start **(12-bit UINT)**	Y	0x00
0x0345	[7:0]	X_ADDR_START_L	RW		Y	0x00
0x0346	[3:0]	Y_ADDR_START_H	RW	y_addr_start **(12-bit UINT)**	Y	0x00
0x0347	[7:0]	Y_ADDR_START_L	RW		Y	0x00
0x0348	[3:0]	X_ADDR_END_H	RW	x_addr_end **(12-bit UINT)**	Y	0x07
0x0349	[7:0]	X_ADDR_END_L	RW		Y	0x87
0x034A	[3:0]	Y_ADDR_END_H	RW	y_addr_end **(12-bit UINT)**	Y	0x04
0x034B	[7:0]	Y_ADDR_END_L	RW		Y	0x47
0x034C	[7:0]	X_OUTPUT_SIZE_H	RW	Output image size X size **(High byte)**	Y	0x07
0x034D	[7:0]	X_OUTPUT_SIZE_L	RW	Output image size X size **(Low byte)**	Y	0x88
0x034E	[7:0]	Y_OUTPUT_SIZE_H	RW	Output image size Y size **(High byte)**	Y	0x04
0x034F	[7:0]	Y_OUTPUT_SIZE_L	RW	Output image size Y size **(Low byte)**	Y	0x40
0x0360	[7:0]	X_OFFSET_H	RW	X_OFFSET **(High byte)**	Y	0x00
0x0361	[7:0]	X_OFFSET_L	RW	X_OFFSET **(Low byte)**	Y	0x00
0x0362	[7:0]	Y_OFFSET_H	RW	Y_OFFSET **(High byte)**	Y	0x00
0x0363	[7:0]	Y_OFFSET_L	RW	Y_OFFSET **(Low byte)**	Y	0x04

Table 3.1: Window horizontal (x) and vertical (y) address programming constraints

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0383	[1:0]	X_ODD_INC	RW	x_odd_increment Datasheet show [1:0]; 1: full 3: sub2 Others : invalid	Y	0x01
0x0387	[1:0]	Y_ODD_INC	RW	Y_odd_increment Datasheet show [1:0]; 1: full 3: sub2 Others: invalid sub2_en_d =**(0x5020=1 OR 0x0387=3)** vbin_en_left_d =vbin_en_right_d =**((0x5020[0]=1 OR 0x0387=3)** AND 0x0390[0]=1**)**	Y	0x01

Table 3.2: Sub-sampling register

3.5 Frame rate control

The notes for the setting of frame length:

- The minimum value of frame length is 1112 in full frame mode.
- The minimum value of frame length is 560 in sub2 mode.
- Frame length ≥ integration time+2.

3.5.1 Full frame readout

In full frame readout mode, the frame rate of the sensor is calculated using the following equations:

A. MAX_LINE_LENGTH_PCK ≥ LINE_LENGTH_PCK (Register 0x0342, 0x0343) ≥ MIN_LINE_LENGTH_PCK

B. MAX_FRAME_LENGTH_LINES ≥ FRAME_LENGTH_LINES (Register 0x0340, 0x0341) ≥ MIN_FRAME_LENGTH_LINES

C. Frame rate = vt_pix_clk MHz x 1 x 10^6 / (FRAME_LENGTH_LINES x LINE_LENGTH_PCK)

Frame Timing Parameter Limit Registers are defined in the registers range from 0x1142 to 0x1147.

3.5.2 Sub2 frame readout

In sub2 frame readout mode, the frame rate of the sensor is calculated using the following equations:

A. MAX_LINE_LENGTH_PCK ≥ LINE_LENGTH_PCK (Register 0x0342, 0x0343) ≥ MIN_LINE_LENGTH_PCK

B. MAX_FRAME_LENGTH_LINES ≥ FRAME_LENGTH_LINES (Register 0x0340, 0x0341) ≥ MIN_FRAME_LENGTH_LINES

C. Frame rate = vt_pix_clk MHz x 1 x 10^6 / (FRAME_LENGTH_LINES x LINE_LENGTH_PCK)

4. Function Description

Image processing and automatic control loop functions are performed by the Image Processor Pipeline **(IPP)**. The IPP can be configured by the host through the serial register interface. The IPP includes Automatic Exposure function which controls dynamic range, exposure, and gamma, as well as blending parameters.

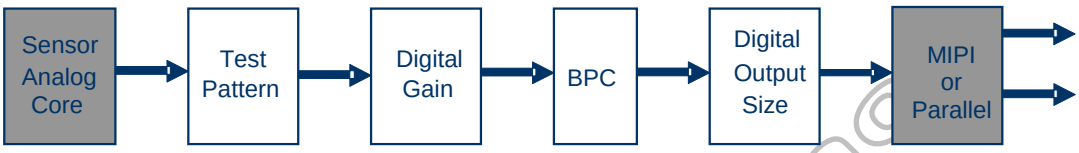


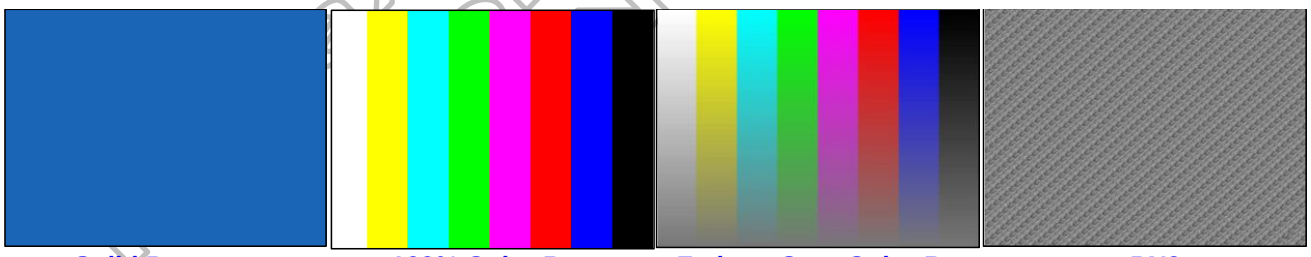
Figure 4.1: Digital signal chain

4.1 Test pattern

On-chip test patterns can be enabled and using test_pattern_mode **(Reg0x0601)**. The test patterns are listed below.

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0601	[2:0]	TEST_PATTERN_MODE	RW	Test Pattern Mode 0: No pattern **(Default)** 1: Solid color **(Test Data defined in 0x0602 - 0x0609)** 2: 100% color bars 3: Color bar blending 4: PN9 **(TEST_PN9_SEED defined in 0x060A - 0x060B)**	-	0x00

Table 4.1: Test pattern control register



Solid Pattern | 100% Color Bar | Fade to Grey Color Bar | PN9

Figure 4.2: Test image pattern (Sample image shown after post-processing demosaic)

4.2 Bad pixel correction

On-the-fly bad pixel correction masks hot and cold single pixel defects by comparing each pixel to BPC threshold value derived from a region of neighboring same-color pixels. The BPC algorithm detects presence of edge within the neighboring pixel window and filters out the detected edge pixels from the threshold computation to minimize false detection.

4.3 Black level (data pedestal) control

The data pedestal defines the black level of the frame when there is no light signal present. The level is programmed as an 8-bit value using register 0x5010. To ensure that black level is maintained with changing global digital gain, register 0x4132 should be programmed to the same value as BLCTGT 0x5010.

The data pedestal of the current frame can be read back from register 0x0009.

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x5010	[7:0]	BLCTGT	RW	BLC target	-	0x20
0x5282	[7:0]	HOTPXLFTH _Lb	RW	Hot pixel threshold LB [7:0]: BLCTGT_Lb[7:0]	-	0x00
0x5283	[2:0]	HOTPXLFTH_Hb	RW	Hot pixel threshold LB [2:0]: BLCTGT_Lb[10:8]	-	0x00

Table 4.2: Black level control registers (Single exposure)

4.4 Lens shading correction

The lens and module assembly can reduce the illumination and induce visible hue shift at the peripheries of the sensor array. To minimize this effect, the Lens Shading Correction **(LSC)** circuit compensates this effect by applying a multi-channel polynomial correction factor to the pixel data as a function of distance from the lens center. Programmable coefficients adjust the behavior of the compensation curve and the center offset. Additional strength adjustment scales the compensation curve from 0 to full compensation in step sizes of 1/16.

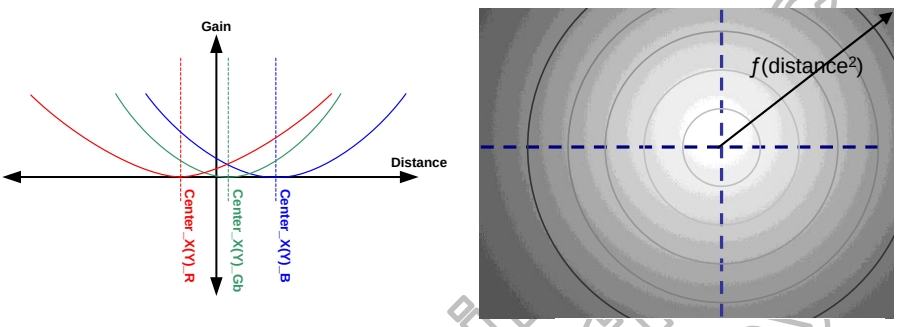


Figure 4.3: Lens shading correction

4.5 SSCG

4.5.1 Introduction of SSCG

HM2140 SSCG is a fractional-N type PLL with a function of spread spectrum clock **(SSC)**. The fractional-N PLL, which implemented by sigma-delta modulation **(SDM)** technique, allows the input clock such provided by crystal to achieve an integer output frequency. The output frequency is equal to a fractional multiplier of input frequency, which is widely used to generate a desired frequency clock. While, the SSC function is also implemented, this intends to reduce EMI **(Electromagnetic Interference)** that has been a problem while increasing system clock speed.
SSCG block diagram is depicted in Figure 4.4.

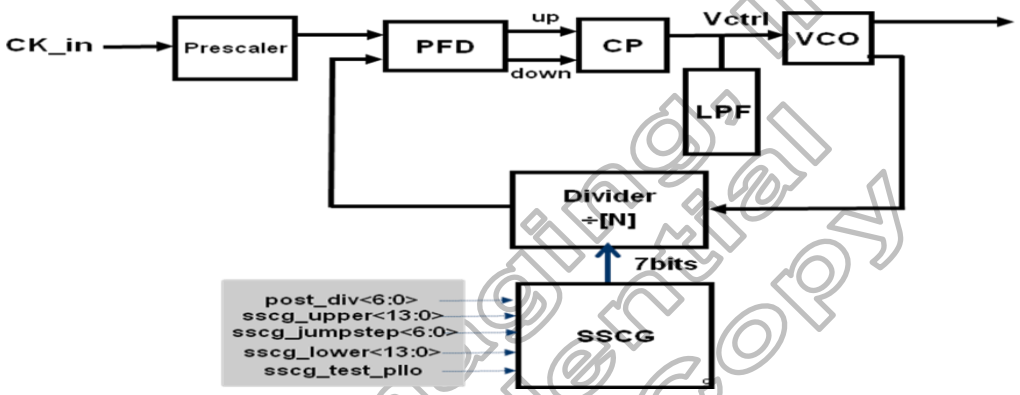
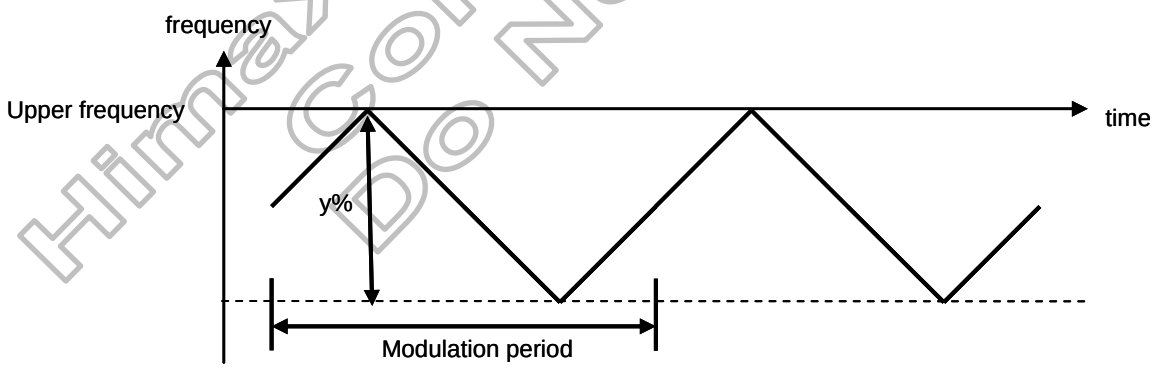


Figure 4.4: SSCG block diagram

4.5.2 SSC modulation rate and spread range configuration



$UPPER[13:0] = 9362(Fixed\ vaule)$

(a) $Upper\_frequency = Fref \times [M]$

(b) $Modulation amount\ y\% = \dfrac{(4 - \frac{LOWER[13:0]}{16383} \times 7)}{M}$

(c) $Modulation period = \dfrac{2 \times (UPPER[13:0] - LOWER[13:0])}{Fref \times STEP[6:0]}$

$Make \dfrac{(UPPER[13:0] - LOWER[13:0])}{STEP[6:0]}$ dividable

4.6 3D SYNC

4.6.1 Synchronize with slave image sensor

The master image sensor transmits four different kinds of signals via SYNC pin and the slave image sensor receives the signals to synchronize with the master sensor's timing. The four signals are distinguished by different lengths of pluses. The signals of "Trigger ON" and "Trigger Off" are used to enable and disable streaming respectively. The signal of "CMU" is used to synchronize the "command update timing" and then the settings can take effect simultaneously in the master and slave sensors.

In streaming mode, the signal of "FSYNC" is auto generated by the master sensor and the slave sensor uses this signal to synchronize timing with the master sensor. If the deviation between "FSYNC" and the slave sensor's timing is greater than the set threshold, the slave sensor will adjust the vertical blank timing automatically to eliminate the deviation. The four kinds of signals are depicted in Figure 4.5.

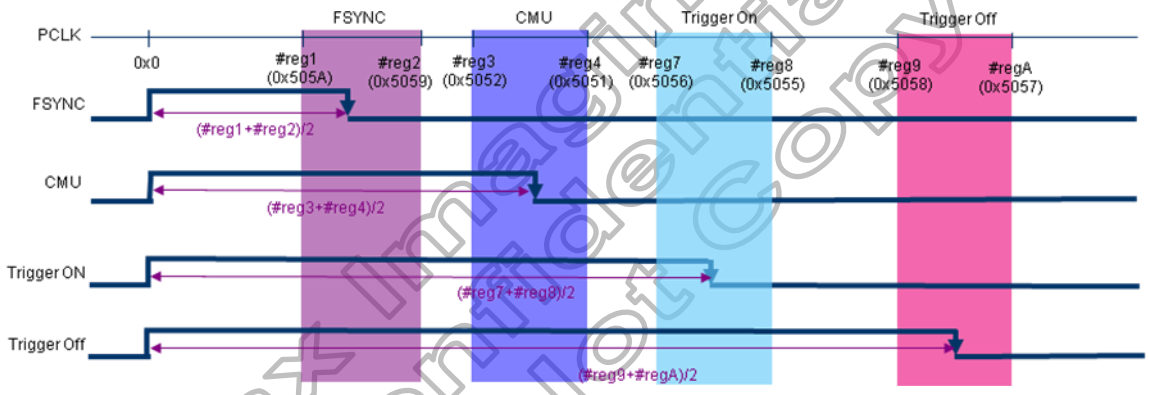


Figure 4.5: The depiction of four kinds of signal

5. Camera System Description

5.1 Clock generation

The HM2140 uses one PLL design to provide clock to the digital logic and MIPI. The output clock generation is based on the following equations:

A. Video Timing Pixel Clock = MCLK x PLL_MIPI_MULTIPLIER_D[7:0] *2 / MIPI_PLL_CLK_DIV_D[4:0] / VT_SYS_DIV_D[1:0] /5

B. MIPI clock = MCLK x PLL_MIPI_MULTIPLIER_D [7:0] *2 / MIPI_PLL_CLK_DIV_D[4:0] OP_PIX_DIV_D[1:0]

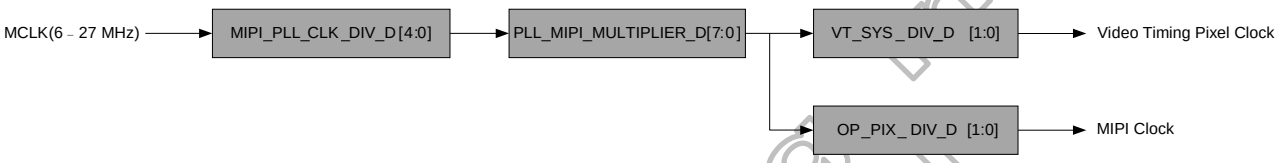


Figure 5.1: Clock generator

5.2 Integration time control

The HM2140 supports coarse integration control with a programmable resolution of 1 row. The exposure time of the sensor is calculated using the following equation:

A. Integration time (Seconds) = coarse_integration x line_length_pck / vt_pix_clk (MHz) x 1 x 10^6

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0202	[7:0]	COARSE_INTEGRATION_H [15:8]	RW	Coarse integration time in lines **(16-bit UINT)**	Y	0x01
0x0203	[7:0]	COARSE_INTEGRATION_L [7:0]	RW		Y	0x08

Table 5.1: Coarse integration control setting

5.2.1 50Hz / 60Hz flicker avoidance

The sensor integration time should be set in intervals of 1/100 seconds or 1/120 seconds for 50Hz or 60Hz flicker avoidance, respectively.

A. Integration step size (60Hz Avoidance) = vt_pix_clk (MHz) x 1 x 10^6 / line_length_pck / 120

B. Integration step size (50Hz Avoidance) = vt_pix_clk (MHz) x 1 x 10^6 / line_length_pck / 100

5.3 Analog gain control

The HM2140 provides two kinds of gain codes to analog gain and uses register 0x50DD to switch gain codes. The settings of different analog gain base on the follow equations

A. SMIA gain code = (M_0x+ C_0)/ (M_1x+ C_1), where x = ANALOG_GLOBAL_GAIN [7:0], M_0 = 1, C_0 = 16, M_1 = 0, C_1 = 16
Analog gain = (x + 16) / 16, where the valid programmable values for the analog gain register are defined in Table 5.3.

B. HII gain code : = 2^ (ANALOG_GLOBAL_GAIN [7:4]) * (1+ ANALOG_GLOBAL_GAIN [3:0]/16)

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0205	[7:0]	ANALOG_GLOBAL_GAIN	RW	Analog Global Gain code	Y	0x00
0x50DD	[0]	GAIN STRATEGY	RW	0: SMIA gain code 1: HII gain code	-	0x00

Table 5.2: Single analog gain control setting

X (hex)	Gain (x)	Gain (dB)	X (hex)	Gain (x)	Gain (dB)
0x00	1	0.0	0x30	4	12.0
0x01	1.0625	0.5	0x34	4.25	12.6
0x02	1.125	1.0	0x38	4.5	13.1
0x03	1.1875	1.5	0x3C	4.75	13.5
0x04	1.25	1.9	0x40	5	14.0
0x05	1.3125	2.4	0x44	5.25	14.4
0x06	1.375	2.8	0x48	5.5	14.8
0x07	1.4375	3.2	0x4C	5.75	15.2
0x08	1.5	3.5	0x50	6	15.6
0x09	1.5625	3.9	0x54	6.25	15.9
0x0A	1.625	4.2	0x58	6.5	16.3
0x0B	1.6875	4.5	0x5C	6.75	16.6
0x0C	1.75	4.9	0x60	7	16.9
0x0D	1.8125	5.2	0x64	7.25	17.2
0x0E	1.875	5.5	0x68	7.5	17.5
0x0F	1.9375	5.7	0x6C	7.75	17.8
0x10	2	6.0	0x70	8	18.1
0x12	2.125	6.5	0x78	8.5	18.6
0x14	2.25	7.0	0x80	9	19.1
0x16	2.375	7.5	0x88	9.5	19.6
0x18	2.5	8.0	0x90	10	20.0
0x1A	2.625	8.4	0x98	10.5	20.4
0x1C	2.75	8.8	0xA0	11	20.8
0x1E	2.875	9.2	0xA8	11.5	21.2
0x20	3	9.5	0xB0	12	21.6
0x22	3.125	9.9	0xB8	12.5	21.9
0x24	3.25	10.2	0xC0	13	22.3
0x26	3.375	10.6	0xC8	13.5	22.6
0x28	3.5	10.9	0xD0	14	22.9
0x2A	3.625	11.2	0xD8	14.5	23.2
0x2C	3.75	11.5	0xE0	15	23.5
0x2E	3.875	11.8	0xE8	15.5	23.8

Table 5.3: Valid global analog gain setting

5.4 Digital gain control

The HM2140 provides global digital gain capability and is programmed in as 2-bit integer **(Digital_Global_Gain_H)** and 6-bit fractional number **(Digital_Global_Gain_L)**.

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x020E	[1:0]	DIGITAL_GLOBAL_GAIN_H [7:6]	RW	Digital Global Gain code **(2.6 fixed point number 2 integer bits,6 fractional bits)**	Y	0x01
0x020F	[7:2]	DIGITAL_GLOBAL_GAIN_L [5:0]	RW		Y	0x00

Table 5.4: Digital gain control register

5.5 Total gain control

The total gain of HM2140 is combined with both analog and digital gain .Various combinations can lead to the same total gain, but the performance could be different. For better image quality, please contact Himax Imaging CSD for the application of high total gain.

Total Gain (x)	Analog Gain (x)	Digital Gain (x)
1	1	1
2	2	1
3	3	1
4	4	1
5	5	1
6	6	1
7	7	1
8	8	1
9	9	1
10	10	1
11	11	1
12	12	1
13	13	1
14	14	1
15	15	1
15.5	15.5	1
16	15.5	1.03
>16	Please contact Himax CSD (Customer Service Department)	

Table 5.5: Total gain control

5.6 Streaming control

The HM2140 streams live video. This mode is entered by writing 0x01 to the mode control register **(0x0100)** and stopped by writing 0x02 to the mode control register **(0x0100)**.

6. Digital Output Format and IO Control

The HM2140 supports both MIPI and parallel interface.

6.1 MIPI serial data interface

The sensor supports 1-lane MIPI CSI-2 interface **(Forward link in High Speed and Low Power mode)** following MIPI Alliance D-PHY specification v1.00.00 and CSI-2 standard v1.00. The sensor can be configured for 10-bit RAW data output, and 1 operation with each lane operating up to 768Mbps.

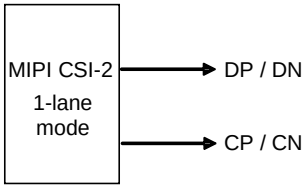


Figure 6.1: MIPI interface lane

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x4024	[6:0]	PCKCTRL	RW	[6]: MIPI enable [5:4]: NA [3]: pclk gated by hsync [2]: pclk gated by vsync [1:0]: pclk gated power down	-	0x00
0x4B20	[7:0]	MIPI_PKT_CTRL	RW	[7]: CLK_LANE_ON [6:5]: CLK_LANE_OPTION 00: Clock is always turn on 01: Clock is on while sending packet 10: Clock is on during whole frame 11: Clock is on between LS & LE [4]: USE_LS_LE 1: Use LS/LE 0: Not use LS/LE [3]: ECC_ON 1: Enable ECC 0: Not use ECC [2]: CRC_ON 1: Enable CRC 0: No CRC generation [1]: F_OPTION 1: Use frame number 1/2/3/4 0: Use frame number 1/2 [0]: CLR_F_NUM 1: Reset frame number to start	-	0xDE

Table 6.1: MIPI control register

6.1.1 Frame format

The format of the frame follows Figure 6.2. The Line Start **(LS)** and Line End **(LE)** marker are enabled by setting MIPI_PKT_CTRL [4]=1.

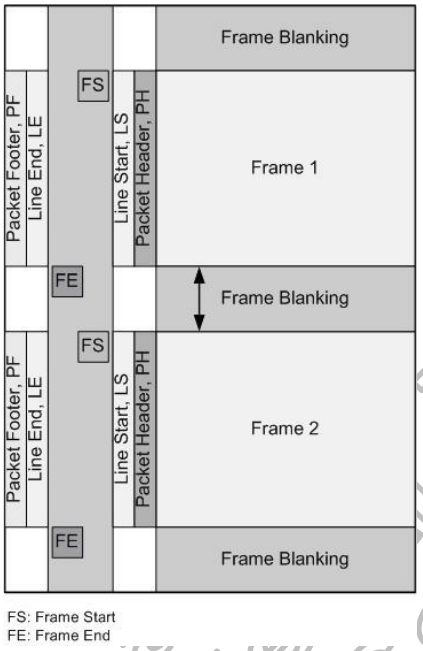


Figure 6.2: Frame format

6.1.2 MIPI clock mode

The HM2140 supports continuous and gated clock mode as shown in Figure 6.3. The clock mode is programmed through the MIPI_PKT_CTRL [6:5] register bits.

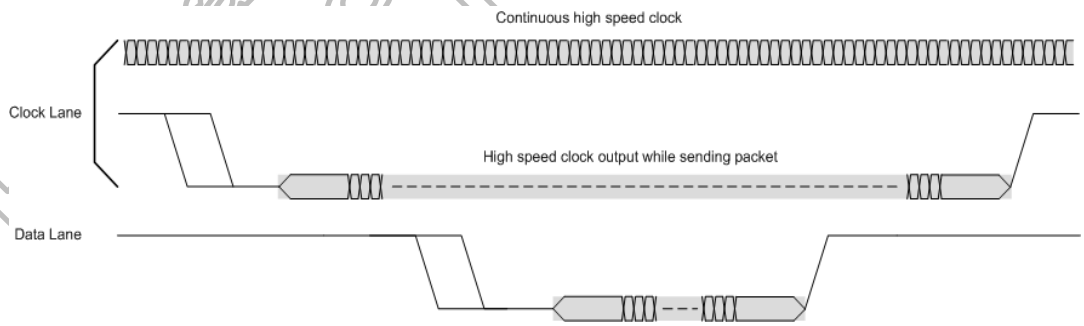


Figure 6.3: MIPI clock lane option

6.2 Parallel interface

The HM2140 supports RAW10 output format. The IO drive current and polarity can be configured to meet a wide array of system requirements. The IO signals are synchronized to the PCLKO output. By default, the data signal transitions on the falling edge of PCLKO. This allows the user to latch data on the subsequent rising edge of PCLKO.

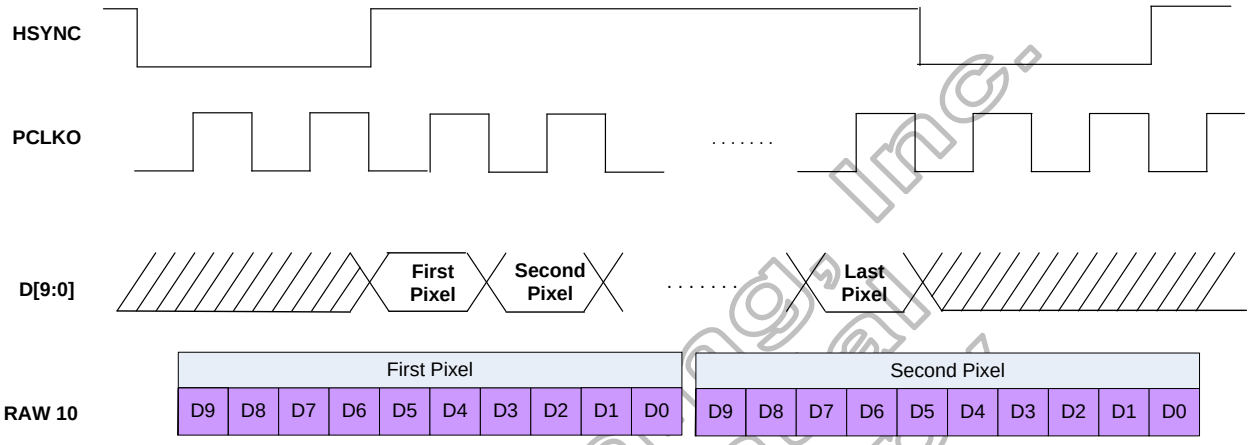


Figure 6.4: RAW output format

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x4020	[7:0]	OPRTCFG	RW	[7]: hsync display polarity [6]: vsync display polarity [5]: pclk display polarity [4:0]: NA	-	0x00

Table 6.2: Parallel control register

7. Serial Control Interface

The 2-Wire serial interface provides read/write access to the sensor registers

- 2-Wire serial interface consists of SDA **(Bidirectional serial data)** and SCL **(Serial clock)** pins.
- If IDSEL pin is pulled down, the slave device ID is 8-bit 0x48h **(Write ID)** and 0x49h **(Read ID)**.
- If IDSEL pin is pulled up, the slave device ID is 8-bit 0x68h **(Write ID)** and 0x69h **(Read ID)**.
- HM2140 uses 16-bit register address and 8-bit register data.
- The sensor uses double-buffered registers to ensure that register changes that affect sensor operation takes place at the beginning of the next valid video frame.
- The host generates SCL clock signal to the sensor and uses the signal to synchronize all data transfer.

7.1 Start / Stop condition

The Start and Stop conditions on the serial bus is issued by the Host.

SDA Transition	SCL	Condition
High to Low	High	Start
Low to High	High	Stop

Table 7.1: 2-Wire serial interface Start / Stop truth table

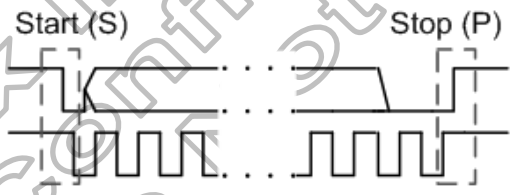


Figure 7.1: 2-Wire serial interface Start / Stop condition

7.2 Data valid

One SCL pulse is generated for each data bit transferred. The host should ensure that the SDA signal must be stable when SCL in High. The SDA signal can transition when SCL is Low.

7.3 Data format

Data is transferred one byte at a time. The most significant bit should always be transferred first. Each byte is followed by an Acknowledge **(ACK)** or a No-Acknowledge bit **(NO ACK)**.

7.4 Acknowledge / No-Acknowledge

Each 8-bit is followed by an Acknowledge **(ACK)** or No-Acknowledge **(NO ACK)** bit.

- Acknowledge: The Host will release the SDA line. The sensor will drive the SDA line low.
- No-Acknowledge: The Host will release the SDA line. The sensor will not drive the SDA pin **(Pulled high)**. The NO ACK bit is used to terminate a read sequence.

7.5 Write sequence

- Initiated by Host with Start **(S)** condition, followed by 8-bit device slave ID **(write ID)**
- If the slave ID is recognized by the sensor, the ACK bit will be sent to the Host.
- Once the Host receives an ACK from the sensor, it can begin to transmit the register address **(High byte first, then low byte)**, then the register data. After each byte, the sensor will issue an ACK or NO ACK signal.
- The write operation is completed when the Host asserts a stop condition

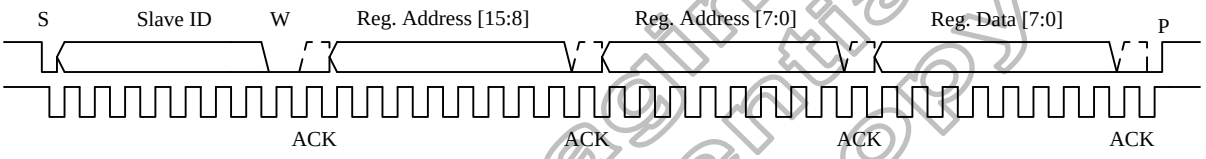


Figure 7.2: 2-Wire serial interface 16-bit address write

7.6 Read sequence

- Initiated by Host with Start **(S)** condition, followed by the 8-bit device slave ID **(write ID)**.
- If the slave ID is recognized by the sensor, the ACK bit will be sent to the Host.
- Once the Host receives an ACK from the sensor, it can begin to transmit the register address **(High byte first, then low byte)**, then the register data. After each byte, the sensor will issue an ACK or NO ACK bit.
- The write operation is completed when the Host asserts a Stop condition.
- The Host must issue another Start condition, followed by the 8-bit device slave ID **(Read ID)**.
- If the register ID is recognized by the sensor, the ACK bit will be sent to the Host.
- The sensor will respond with the Register Data Out.
- The Host will issue an ACK, and then asserts the Stop condition.

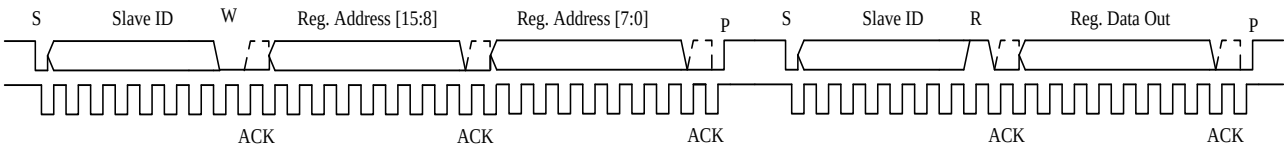
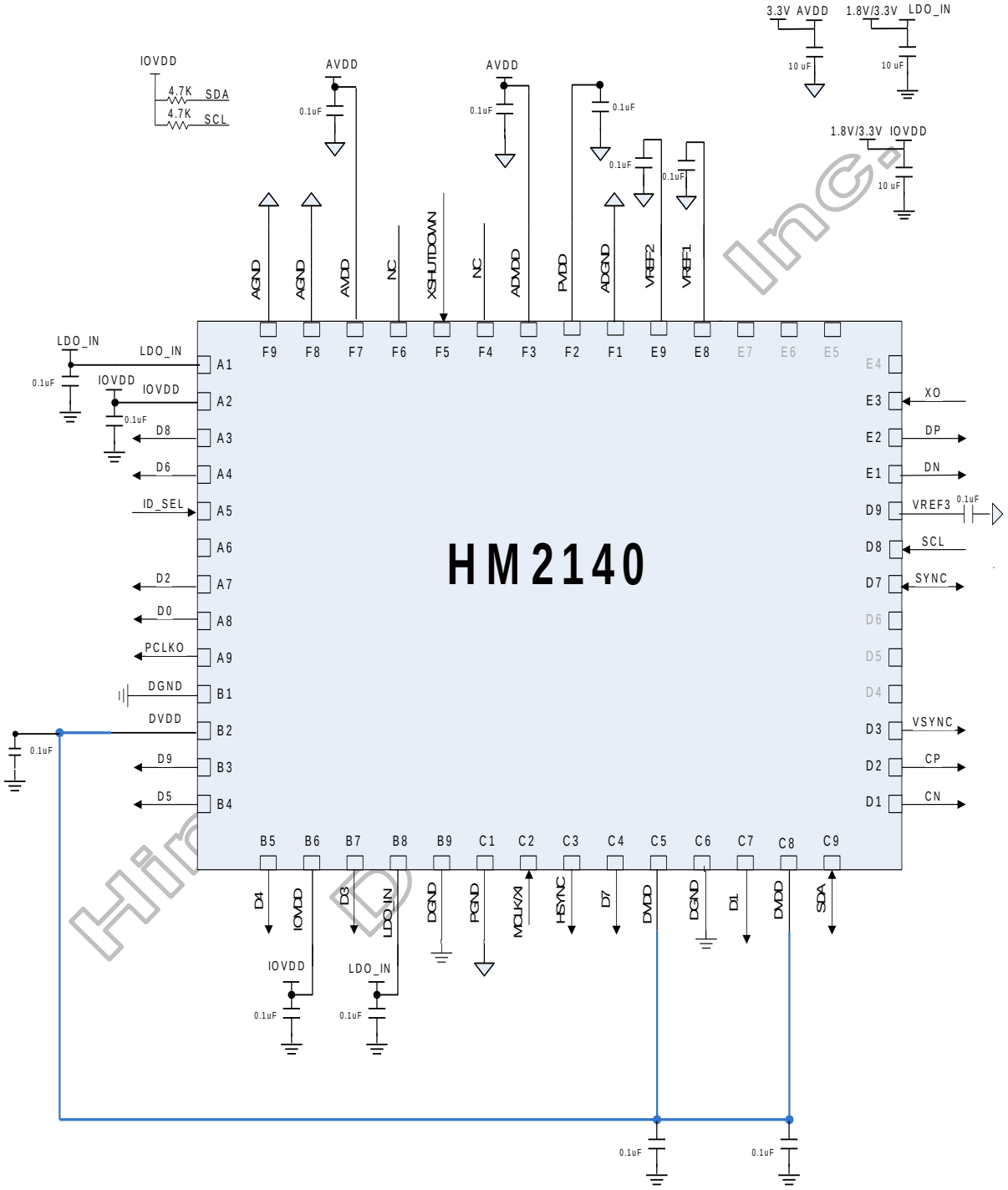


Figure 7.3: 2-Wire serial interface 16-bit address read

8. Typical Configuration

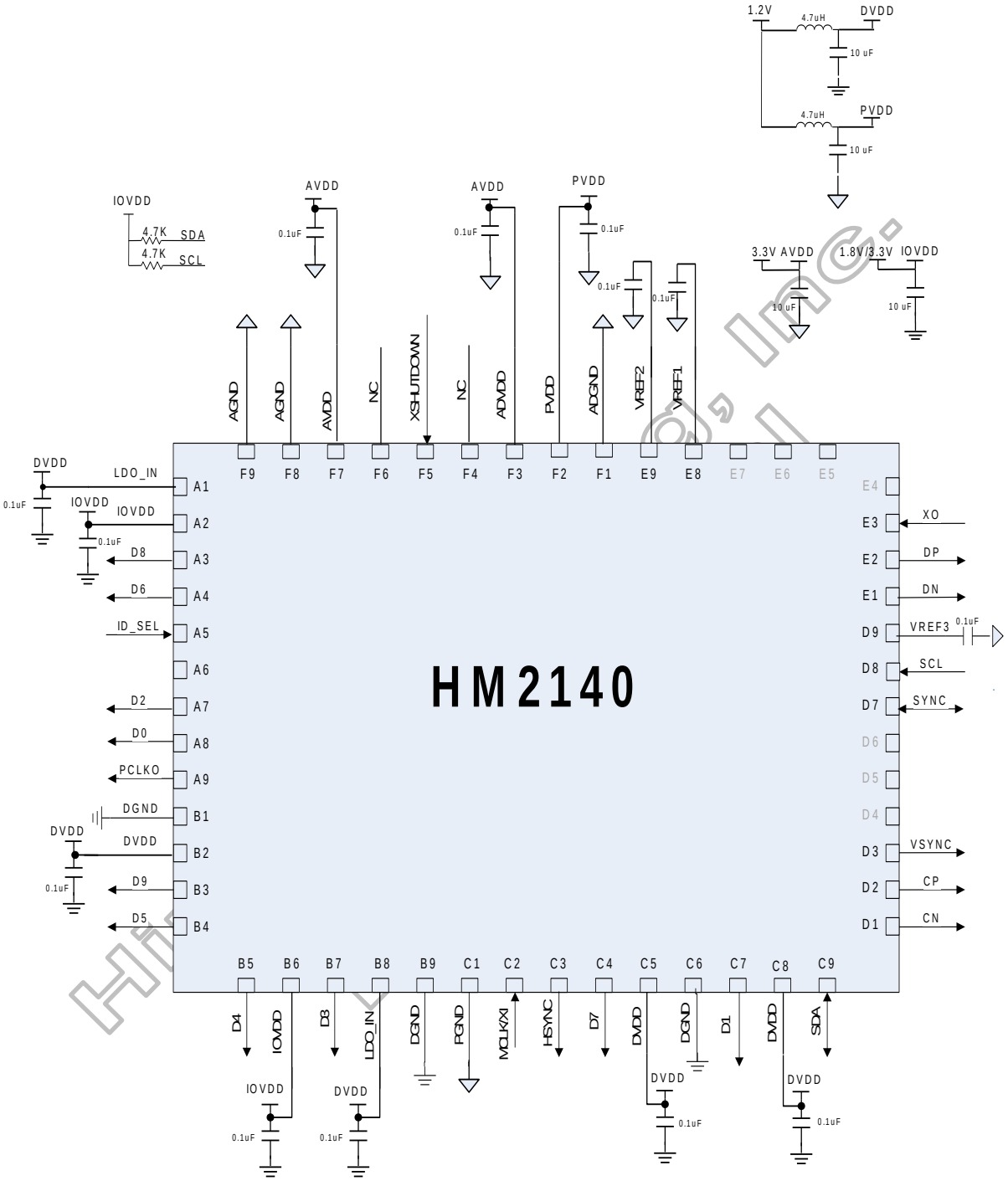
8.1 Internal LDO mode (CSP)



Note: **(1) XO should be connected to IOVDD when using MCLK.**
(2) CCI pull-up resistors should have a value based on the CCI specification **(Typically 4k7 ohms)**.
(3) CP/CN, DP/DN are differential signals.
(4) Decoupling capacitors should be kept as physically close to the die as possible.
(5) AGND and DGND should be separated and connected to a single point outside the module.

Figure 8.1: HM2140 typical configuration (Internal LDO mode)

8.2 Bypass internal LDO mode (CSP)



Note: (1) XO should be connected to IOVDD when using MCLK.
(2) CCI pull-up resistors should have a value based on the CCI specification **(Typically 4k7 ohms)**.
(3) CP/CN, DP/DN are differential signals.
(4) Decoupling capacitors should be kept as physically close to the die as possible.
(5) AGND and DGND should be separated and connected to a single point outside the module.

Figure 8.2: HM2140 typical configuration (Bypass internal LDO mode)

9. Operating Mode

The HM2140 has five operating modes, including Hardware Shutdown **(XSHUTDOWN pin control)**. Depending on the configuration of XSHUTDOWN pin, the power up and power down sequence will be different.

Operating mode	Power supply	XSHUTDOWN pin	MODE_SELECT[1:0] register control	POR	MIPI O/P
Power off	Off	X	X	X	X
Hardware shutdown	On	Low	X	Yes	LP00
Software standby	On	High	2'b00	No	LP11 w/o ULPS LP00 w/ ULPS
STOP streaming mode(1)	On	High	2'b10	No	LP11 / LP00
Pixel data streaming	On	High	2'bx1	No	Data

Note: (1) Please contact Himax Imaging CSD on details of ULPS mode and sequence.

Table 9.1: Operating modes

Operating mode	SDA / SCL power down	PLL power down	Clk Pad power down	ASC / BGP power down	MIPI PHY power down
Power off	X	X	X	X	X
Hardware shutdown	Yes	Yes	Yes	Yes	Yes
Software standby	No	Yes	No	Yes	Yes
STOP streaming mode(1)	No	No	No	No	Yes
Pixel data streaming	No	No	No	No	No

Note: (1) Please contact Himax Imaging CSD on details of ULPS mode and sequence.

Table 9.2: Operating mode block power down

9.1 Power on reset

The sensor will apply an internal system reset when DVDD supply reaches a supply voltage threshold or when XSHUTDOWN is asserted.

9.2 Software reset register

Software reset can be applied by writing register value 1 to the SW_RESET [0] register. When reset is applied, the sensor will be placed in Software standby mode and reset all serial interface registers to its default values.

9.3 Frame count register

The frame count register **(Read only)** increment by 1 at the end of each frame. Once the counter reaches 255, it will roll over to 0. When software reset is applied, the frame count defaults to 0 **(0x00h)**.

9.4 System configuration

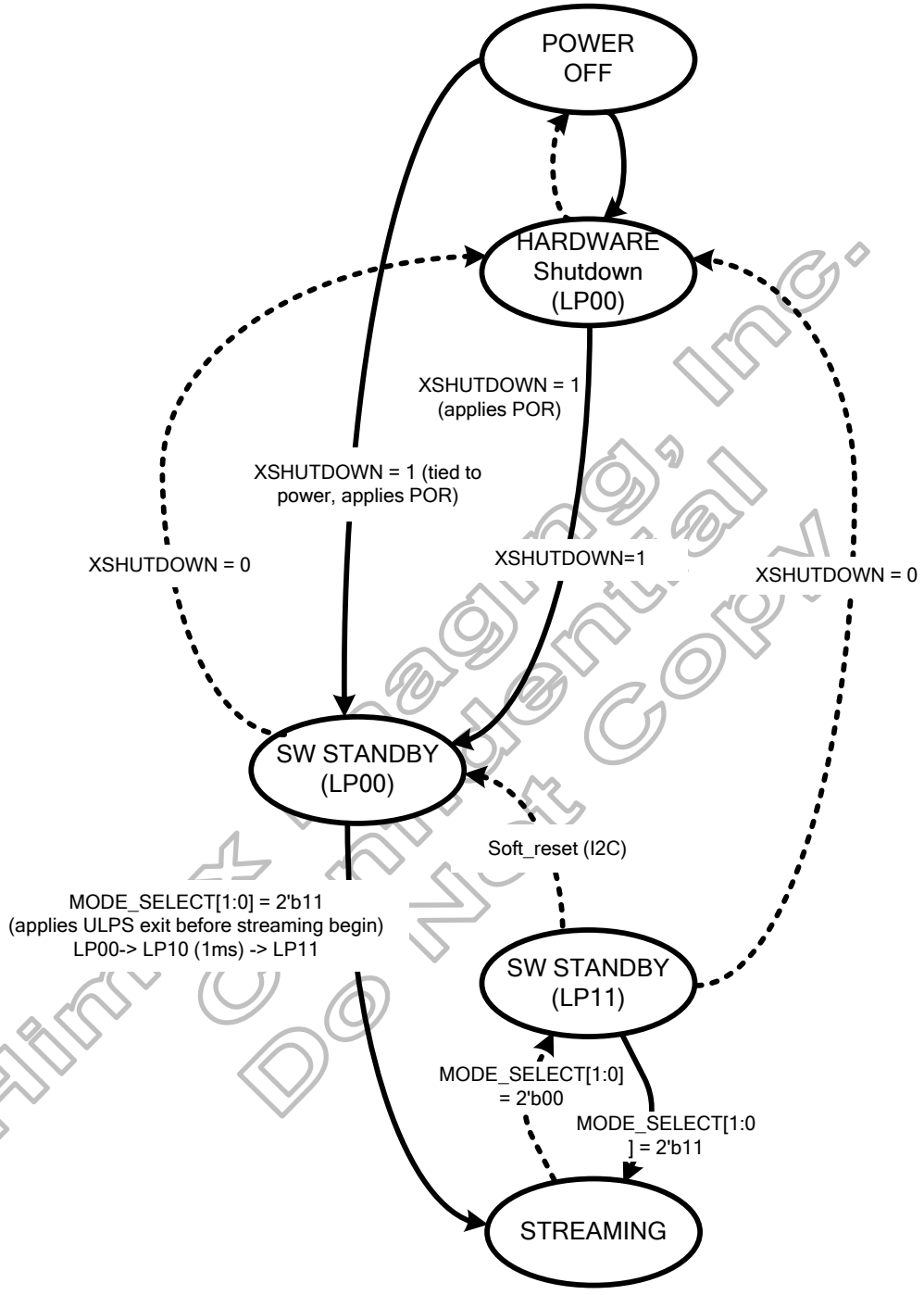
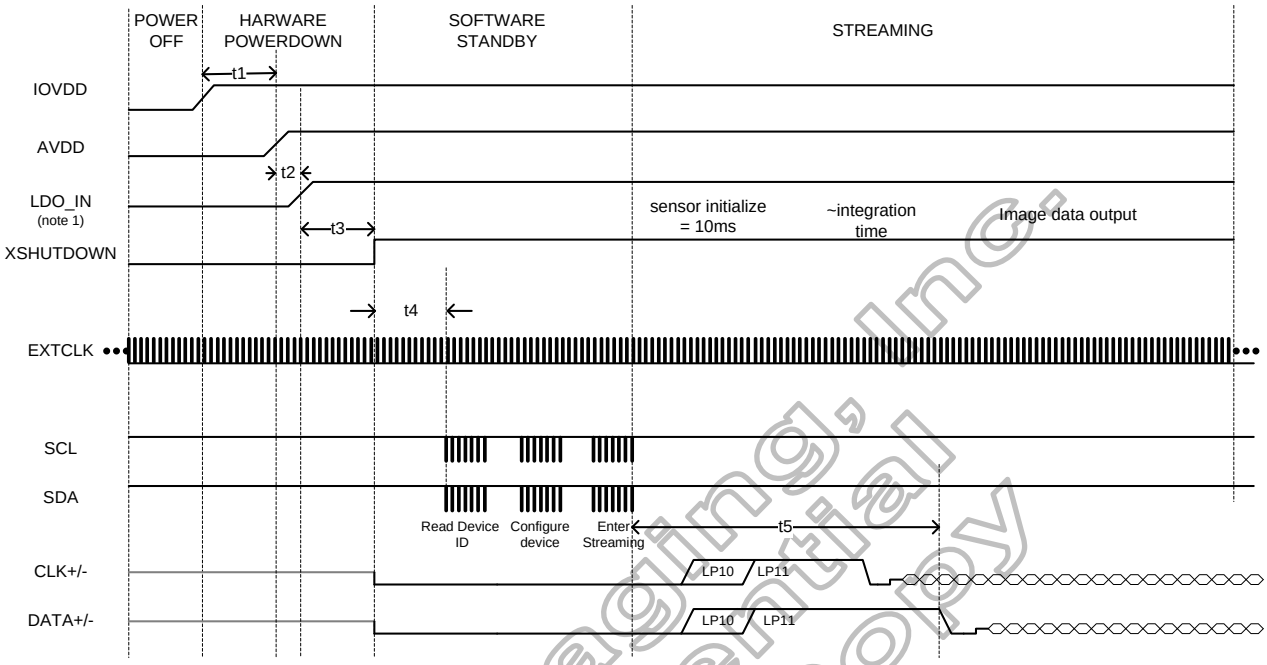


Figure 9.1: System states using hardware shutdown (XSHUTDOWN)

9.5 Power-up sequence

9.5.1 Power-up sequence with hardware shutdown



Note: (1) When using bypass LDO mode, supply DVDD / LDO_IN to 1.2V;
When using internal LDO mode, supply LDO_IN to 1.8V and DVDD is only connected to bypass capacitors.

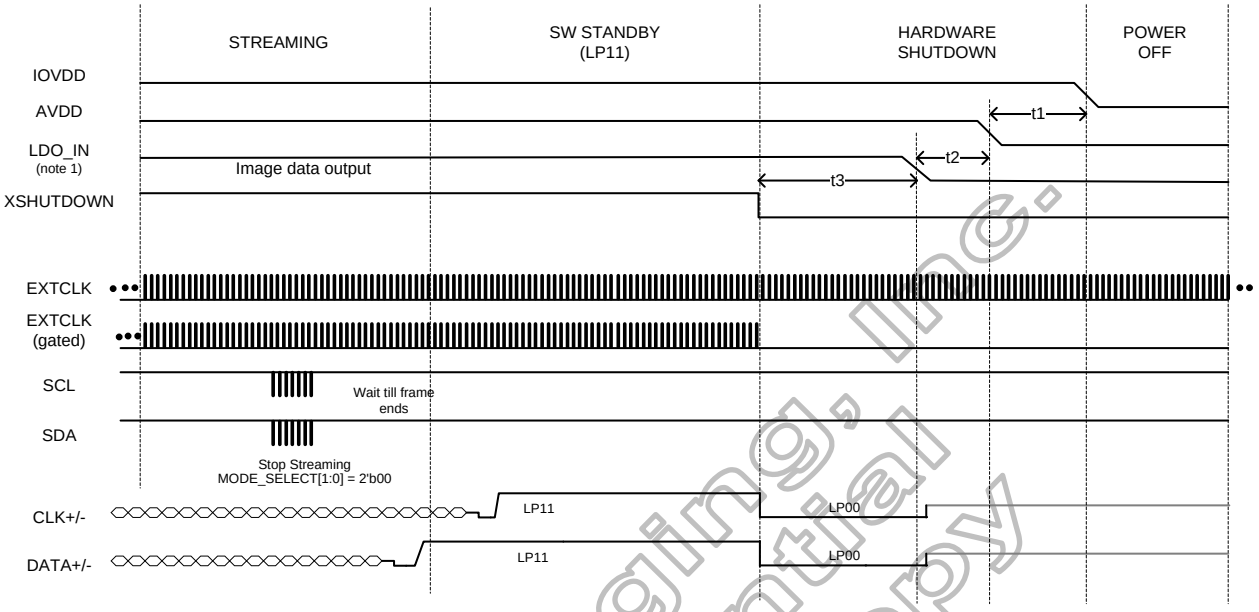
Figure 9.2: Power-up sequence with hardware shutdown (XSHUTDOWN)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
IOVDD to AVDD	t1	0	-	∞	s
AVDD to LDO_IN	t2	0	-	∞	s
LDO_IN to XSHUTDOWN	t3	0	-	∞	s
XSHUTDOWN to SDA / SCL transaction	t4	100	-	-	μs
Enter streaming time	t5	1.8	-	-	ms

Table 9.3: Power-up sequence timing (XSHUTDOWN)

9.6 Power-down sequence

9.6.1 Power-down sequence with hardware shutdown



Note: (1) When using bypass LDO mode, supply DVDD / LDO_IN to 1.2V;
When using internal LDO mode, supply LDO_IN to 1.8V and DVDD is only connected to bypass capacitors.

Figure 9.3: Power-down without ULPS sequence (XSHUTDOWN)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
AVDD to IOVDD	t1	0	-	∞	s
LDO_IN to AVDD	t2	0	-	∞	s
XSHUTDOWN to LDO_IN	t3	0	-	∞	s

Table 9.4: Power-down without ULPS sequence timing (XSHUTDOWN)

10. Register Table

- There are 3 types of registers, Read-Write **(RW)**, Read-Only **(RO)** and Write-Only **(WO)** registers.
- Registers that require Command Update are indicated in the 'CMU' column**.**
- Writing to reserved and unlisted registers will cause undefined sensor behavior.

10.1 Status register [0x0000 – 0x0006]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0000	[7:0]	MODEL_ID_H [15:8]	RO	16-bit sensor part number **(HM2140)**	-	0x21
0x0001	[7:0]	MODEL_ID_L [7:0]	RO		-	0x40
0x0002	[7:0]	SILICON_REV	RO	Silicon revision number	-	0x00
0x0005	[7:0]	FRAME_COUNT	RO	8-bit frame counter value; reset to 0xFF during SW standby	-	0xFF
0x0006	[1:0]	PIXEL_ORDER	RO	[1:0]: Color pixel order 0: GR 1: RG 2: BG 3: GB	-	0x02

10.2 General setup register [0x0100 – 0x0104]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0100	[1:0]	MODE_SELECT	RW	[1:0]: Sensor mode selection 00: SW standby mode 01: Streaming mode 10: Stop mode	Y	0x00
0x0101	[1:0]	IMAGE_ORIENTATION	RW	Image orientation [1]: Vertical flip En [0]: Horizontal mirror En	Y	0x00
0x0102	[0]	EMBEDDED_ENABLE	RW	[0]: Embedded data line enable 0: Disable 1: Enable	Y	0x00
0x0103	[0]	SW_RESET	WO	Software reset	N	0xFF
0x0104	[0]	CMU_UPDATE_Normal	WO	CMU update	-	0x00

10.3 Output setup register [0x0202 – 0x020F]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0202	[7:0]	COARSE_INTEGRATION_H [15:8]	RW	Coarse integration time in lines **(16-bit UINT)**	Y	0x01
0x0203	[7:0]	COARSE_INTEGRATION_L [7:0]	RW		Y	0x08
0x0205	[7:0]	ANALOG_GLOBAL_GAIN	RW	Analog Global Gain code **(8-bit UINT)**	Y	0x00
0x020E	[1:0]	DIGITAL_GLOBAL_GAIN_H	RW	Digital Global Gain code **(10-bit UINT)**	Y	0x01
0x020F	[7:0]	DIGITAL_GLOBAL_GAIN_L	RW		Y	0x00

10.4 Clock setup register [0x0307 – 0x030A]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0307	[7:0]	vt_sys_div_d	RW	[7:0]: vt_sys_div_d<7:0>	N	0x34
0x0309	[1:0]	op_pix_div_d	RW	[1:0]: op_pix_div_d<1:0> For mipi clk 00= /1 01= /2 10= /4 11= /8	N	0x01
0x030A	[7:0]	mipi_pll3_d	RW	[7:0]: mipi_pll3_d<7:0> [7:6]: For pkt_clk_d delay [5]: For CP_ctrl<2> [4]: For bypass PLL [3:2]: For RP_ctrl<1:0> [1:0]: For CP_ctrl<1:0>	N	0x09

10.5 Frame timing register [0x0340 – 0x0343]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0340	[7:0]	FRAME_LENGTH_LINES_H [15:8]	RW	frame_length_lines **(16-bit UINT)**	Y	0x04
0x0341	[7:0]	FRAME_LENGTH_LINES_L [7:0]	RW		Y	0x56
0x0342	[7:0]	LINE_LENGTH_PCK_H [15:8]	RW	line_length_pck **(16-bit UINT)**	Y	0x00
0x0343	[7:0]	LINE_LENGTH_PCK_L [7:0]	RW		Y	0x84

10.6 Image size register [0x0344 – 0x0363]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0344	[3:0]	X_ADDR_START_H	RW	x_addr_start **(12-bit UINT)**	Y	0x00
0x0345	[7:0]	X_ADDR_START_L	RW		Y	0x00
0x0346	[3:0]	Y_ADDR_START_H	RW	y_addr_start **(12-bit UINT)**	Y	0x00
0x0347	[7:0]	Y_ADDR_START_L	RW		Y	0x00
0x0348	[3:0]	X_ADDR_END_H	RW	x_addr_end **(12-bit UINT)**	Y	0x07
0x0349	[7:0]	X_ADDR_END_L	RW		Y	0x87
0x034A	[3:0]	Y_ADDR_END_H	RW	y_addr_end **(12-bit UINT)**	Y	0x04
0x034B	[7:0]	Y_ADDR_END_L	RW		Y	0x47
0x034C	[7:0]	X_OUTPUT_SIZE_H	RW	Output image size X size **(High byte)**	Y	0x07
0x034D	[7:0]	X_OUTPUT_SIZE_L	RW	Output image size X size **(Low byte)**	Y	0x88
0x034E	[7:0]	Y_OUTPUT_SIZE_H	RW	Output image size Y size **(High byte)**	Y	0x04
0x034F	[7:0]	Y_OUTPUT_SIZE_L	RW	Output image size Y size **(Low byte)**	Y	0x40
0x0360	[7:0]	X_OFFSET_H	RW	X_OFFSET **(High byte)**	Y	0x00
0x0361	[7:0]	X_OFFSET_L	RW	X_OFFSET **(Low byte)**	Y	0x00
0x0362	[7:0]	Y_OFFSET_H	RW	Y_OFFSET **(High byte)**	Y	0x00
0x0363	[7:0]	Y_OFFSET_L	RW	Y_OFFSET **(Low byte)**	Y	0x04

10.7 Sub-sampling register [0x0383 – 0x0387]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0383	[1:0]	X_ODD_INC	RW	x_odd_increment Datasheet show [1:0]; 1: Full 3: Sub2 Others: Invalid	Y	0x01
0x0387	[1:0]	Y_ODD_INC	RW	y_odd_increment Datasheet show [1:0]; 1: Full 3: Sub2 Others : Invalid	Y	0x01

10.8 Binning mode register [0x0390]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0390	[2:0]	BINNING_MODE	RW	[2]: Digital summing [1]: Horizontal binning [0]: Vertical binning	Y	0x00

10.9 Test pattern register [0x0601 – 0x060B]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0601	[3:0]	TEST_PATTERN_MODE	RW	Test pattern mode [3:0]: 0: Test pattern disable 1: Solid color 2: Color bar 3: Color bar blending 4: PN9	N	0x00
0x0602	[1:0]	TEST_DATA_RED_H	RW	Test data RED	N	0x00
0x0603	[7:0]	TEST_DATA_RED_L	RW	**(10-bit UINT)**	N	0x80
0x0604	[1:0]	TEST_DATA_GR_H	RW	Test data greenR	N	0x00
0x0605	[7:0]	TEST_DATA_GR_L	RW	**(10-bit UINT)**	N	0x80
0x0606	[1:0]	TEST_DATA_BLUE_H	RW	Test data BLUE	N	0x00
0x0607	[7:0]	TEST_DATA_BLUE_L	RW	**(10-bit UINT)**	N	0x80
0x0608	[1:0]	TEST_DATA_GB_H	RW	Test data greenB	N	0x00
0x0609	[7:0]	TEST_DATA_GB_L	RW	**(10-bit UINT)**	N	0x80
0x060A	[1:0]	TEST_PN9_SEED_H	RW	PN9 random seed	N	0x00
0x060B	[7:0]	TEST_PN9_SEED_L	RW	**(10-bit UINT)**	N	0x01

10.10 Frame timing parameter limit register [0x1142 – 0x1147]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x1142	[7:0]	MAX_FRAME_LENGTH_LINES_H	RO	Maximum frame length **(16-bit UINT)**	-	0xFF
0x1143	[7:0]	MAX_FRAME_LENGTH_LINES_L	RO		-	0xFF
0x1144	[7:0]	MIN_LINE_LENGTH_PCK_H	RO	Minimum line length **(16-bit UINT)**	-	0xFF
0x1145	[7:0]	MIN_LINE_LENGTH_PCK_L	RO		-	0xFF
0x1146	[7:0]	MAX_LINE_LENGTH_PCK_H	RO	Maximum line length **(16-bit UINT)**	-	0xFF
0x1147	[7:0]	MAX_LINE_LENGTH_PCK_L	RO		-	0xFF

10.11 Raw domain control register [0x4132 – 0x414A]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x4132	[7:0]	RAWCtrlByte7	RW	[7:0]: BLI target for digital gain blocks	-	0x20
0x414A	[1:0]	BLCCFG3	RW	[1:0]: Inter-frame weighting control 0: 1/8 1: 1/16 2: 1/32 3: NA	-	0x03

10.12 BLC programming register [0x5010 – 0x5283]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x5010	[7:0]	BLCTGT	RW	BLC target	-	0x20
0x5282	[7:0]	HOTPXLFTH _Lb	RW	Hot pixel threshold LB [7:0]: BLCTGT_Lb[7:0]	-	0x00
0x5283	[2:0]	HOTPXLFTH_Hb	RW	Hot pixel threshold LB [2:0]: BLCTGT_Lb[10:8]	-	0x00

10.13 LSC prarmeter control register [0x3420 – 0x3458]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x3420	[7:0]	COE_sign	RW	Coefficient sign [7]: COE_B_X1_sign [6]: COE_Gb_X1_sign [5]: COE_Gr_X1_sign [4]: COE_R_X1_sign [3]: COE_B_X0_sign [2]: COE_Gb_X0_sign [1]: COE_Gr_X0_sign [0]: COE_R_X0_sign	N	0x00
0x3421	[7:0]	COE_R_X2	RW	COE_R_X2	N	0xB0
0x3422	[7:0]	COE_R_X1	RW	COE_R_X1	N	0x00
0x3423	[7:0]	COE_R_X0	RW	COE_R_X0	N	0x80
0x3424	[7:0]	COE_GB_X2	RW	COE_GB_X2	N	0x8E
0x3425	[7:0]	COE_GB_X1	RW	COE_GB_X1	N	0x00
0x3426	[7:0]	COE_GB_X0	RW	COE_GB_X0	N	0x80
0x3427	[7:0]	COE_GR_X2	RW	COE_GR_X2	N	0x8E
0x3428	[7:0]	COE_GR_X1	RW	COE_GR_X1	N	0x00
0x3429	[7:0]	COE_GR_X0	RW	COE_GR_X0	N	0x80
0x342A	[7:0]	COE_B_X2	RW	COE_B_X2	N	0x88
0x342B	[7:0]	COE_B_X1	RW	COE_B_X1	N	0x00
0x342C	[7:0]	COE_B_X0	RW	COE_B_X0	N	0x88
0x342D	[4:0]	Shift_R_X2	RW	Shift_R_X2	N	0x14
0x342E	[4:0]	Shift_R_X1	RW	Shift_R_X1	N	0x09
0x342F	[4:0]	Shift_GB_X2	RW	Shift_GB_X2	N	0x14
0x3430	[4:0]	Shift_GB_X1	RW	Shift_GB_X1	N	0x09
0x3431	[4:0]	Shift_GR_X2	RW	Shift_GR_X2	N	0x14
0x3432	[4:0]	Shift_GR_X1	RW	Shift_GR_X1	N	0x09
0x3433	[4:0]	Shift_B_X2	RW	Shift_B_X2	N	0x14
0x3434	[4:0]	Shift_B_X1	RW	Shift_B_X1	N	0x09
0x3440	[2:0]	B_Center_X_H[10:8]	RW	B_Center_X **(High byte)**	N	0x03
0x3441	[7:0]	B_Center_X_L[7:0]	RW	B_Center_X **(Low byte)**	N	0xC4
0x3442	[2:0]	B_Center_Y_H[10:8]	RW	B_Center_Y **(High byte)**	N	0x02
0x3443	[7:0]	B_Center_Y_L[7:0]	RW	B_Center_Y **(Low byte)**	N	0x20
0x3444	[2:0]	Gb_Center_X_H[10:8]	RW	Gb_Center_X **(High byte)**	N	0x03
0x3445	[7:0]	Gb_Center_X_L[7:0]	RW	Gb_Center_X **(Low byte)**	N	0xC4
0x3446	[2:0]	Gb_Center_Y_H[10:8]	RW	Gb_Center_Y **(High byte)**	N	0x02
0x3447	[7:0]	Gb_Center_Y_L[7:0]	RW	Gb_Center_Y **(Low byte)**	N	0x20
0x3448	[2:0]	Gr_Center_X_H[10:8]	RW	Gr_Center_X **(High byte)**	N	0x03
0x3449	[7:0]	Gr_Center_X_L[7:0]	RW	Gr_Center_X **(Low byte)**	N	0xC4
0x344A	[2:0]	Gr_Center_Y_H[10:8]	RW	Gr_Center_Y **(High byte)**	N	0x02
0x344B	[7:0]	Gr_Center_Y_L[7:0]	RW	Gr_Center_Y **(Low byte)**	N	0x20
0x344C	[2:0]	R_Center_X_H[10:8]	RW	R_Center_X **(High byte)**	N	0x03
0x344D	[7:0]	R_Center_X_L[7:0]	RW	R_Center_X **(Low byte)**	N	0xC4
0x344E	[2:0]	R_Center_Y_H[10:8]	RW	R_Center_Y **(High byte)**	N	0x02
0x344F	[7:0]	R_Center_Y_L[7:0]	RW	R_Center_Y **(Low byte)**	N	0x20
0x3450	[1:0]	D_WIN_MODE	RW	Dwin mode enable	N	0x00
0x3451	[0]	BW_MODE	RW	Black/White mode enable	N	0x00
0x3452	[0]	G1G2_SAME_CURVE	RW	Gr and Gb same curve enable	N	0x00
0x3453	[4:0]	LSC_ALPHA_REG	RW	LSC_ALPHA_REG	N	0x0E
0x3455	[2:0]	LSC_AST_X_H[10:8]	RW	LSC_AST_X **(High byte)**	N	0x00
0x3456	[7:0]	LSC_AST_X_L[7:0]	RW	LSC_AST_X **(Low byte)**	N	0x00
0x3457	[2:0]	LSC_AST_Y_H[10:8]	RW	LSC_AST_Y **(High byte)**	N	0x00
0x3458	[7:0]	LSC_AST_Y_L[7:0]	RW	LSC_AST_Y **(Low byte)**	N	0x00

10.14 Timing control register [0x5090 – 0x5093]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x5090	[7:0]	PWR_SAVE_THH	RW	BGP power saving mode threshold	N	0x00
0x5091	[7:0]	PWR_SAVE_THL	RW	BGP power saving mode threshold	N	0x40
0x5092	[7:0]	PWR_SAVE_DLY	RW	BGP power saving mode adjustment register	N	0x20
0x5093	[7:0]	PWR_SAVE_TAIL	RW	BGP power saving mode adjustment register	N	0x10

10.15 MIPI programming register [0x4B20]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x4B20	[7:0]	MIPI_PKT_CTRL	RW	[7]: CLK_LANE_ON [6:5]: CLK_LANE_OPTION 00: Clock is always turn on 01: Clock is on while sending packet 10: Clock is on during whole frame 11: Clock is on between LS & LE [4]: USE_LS_LE 1: Use LS/LE 0: No use LS/LE [3]: ECC_ON 1: Enable ECC 0: Not use ECC [2]: CRC_ON 1: Enable CRC 0: No CRC generation [1]: F_OPTION 1: Use frame number 1/2/3/4 0: Use frame number 1/2 [0]: CLR_F_NUM 1: Reset frame number to start	-	0xDE

10.16 3D SYNC register [0x5050 – 0x505F]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x5050	[7:0]	3D Sync Control Byte	RW	{[7][6]} 00: Mux_TriggerEnableIn {01,11}: TriggerEnable In 10: Mux_TriggerEnable In & Slave mode [5]: 3D sync Mode Select 0: From i2c 1: Re-generate by slave mode [3]:Auto correction [2]: FSIN enable [1]: slave / master 0:master 1:slave For master mode: SYNC pin is output For slave mode: SYNC pin is input [0]: sel_3d	-	0x00
0x5051	[7:0]	3D CMU Pulse Width High Byte	RW	3D Sync CMU update **(Hb)**	-	0x14
0x5052	[7:0]	3D CMU pulse Width Low Byte	RW	3D Sync CMU update **(Lb)**	-	0x0F
0x5055	[7:0]	3D Sync Trigger ON High Byte	RW	3D Sync Trigger ON **(Hb)**	-	0x30
0x5056	[7:0]	3D Sync Trigger ON Low Byte	RW	3D Sync Trigger ON **(Lb)**	-	0x24
0x5057	[7:0]	3D Sync Trigger OFF High Byte	RW	3D Sync Trigger OFF **(Hb)**	-	0x40
0x5058	[7:0]	3D Sync Trigger OFF Low Byte	RW	3D Sync Trigger OFF **(Lb)**	-	0x34
0x5059	[7:0]	3DSYNC_CALI_H	RW	Programmable adjustment indicator	N	0x0C
0x505A	[7:0]	3DSYNC_CALI_L	RW	Programmable adjustment indicator	N	0x07
0x505C	[7:0]	MAX_COUNTER_H	RW	Maximum of alignment counter	N	0x04
0x505D	[7:0]	MAX_COUNTER_L	RW	Maximum of alignment counter	N	0x00
0x505E	[7:0]	FSIN_CORR_H	RW	Threshold of FSIN correction	N	0x01
0x505F	[7:0]	FSIN_CORR_L	RW	Threshold of FSIN correction	N	0xE0

10.17 SSCG control register [0x5235 – 0x5239]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x5235	[7:0]	SSCG_ UPPER _H	RW	[7]: sscg_sel_postdiv [5:0]: sscg_upper_hb	-	0x27
0x5236	[7:0]	SSCG_ UPPER _L	RW	[7:0]: sscg_upper_lb	-	0x80
0x5237	[5:0]	SSCG_ LOWER _H	RW	[5:0]: sscg_lower_hb	-	0x21
0x5238	[7:0]	SSCG_ LOWER _L	RW	[7:0]: sscg_lower_lb	-	0xA4
0x5239	[7:0]	SSCG_JUMPSTEP	RW	[7]: sscg_enb [6:0]: sscg_jumpstep	-	0x0F

11. Electrical Specification

11.1 Absolute maximum rating

Parameter		Symbol	Spec.			Unit
			Min.	Typ.	Max.	
Ambient storage temperature		T_{STLIM}	-40	-	125	°C
Operating temperature **(Junction temperature)**		T_{OPLIM}	-30	-	85	°C
Stable image temperature **(Junction temperature)**		T_{SI}	0	-	70	°C
Analog supply voltage		$V_{DD\_A\_MAX}$	-0.3	-	4.0	V
Digital supply voltage		$V_{DD\_D\_MAX}$	-0.3	-	2.0	V
IO supply voltage		$V_{DD\_IO\_MAX}$	-0.3	-	4.0	V
DC input voltage		DC_{IN}	-0.3	-	V_{DD}+0.3	V
ESD rating	Human body model	ESD	-	2000	-	V
	Machine model		-	200	-	V

Note: (1) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 11.1: Absolute maximum rating

11.2 Operating rating

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Analog supply voltage	VDD-AVDD	3.0	3.3	3.6	V
LDO supply voltage	VDD-LDO_IN	1.7	1.8	3.6	V
Digital supply voltage	VDD-DVDD	1.08	1.2	1.32	V
MIPI supply voltage	VDD-PVDD	1.08	1.2	1.32	V
IO supply voltage	VDD-IOVDD	1.7	1.8	3.6	V

Table 11.2: Operating rating

11.3 DC characteristic

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Power Consumption- Bypass LDO mode(1)						
Active current **(MIPI)**	I_{DD_AVDD}	Video@30FPS full resolution PN9	-	13.11	-	mA
	I_{DD_DVDD}		-	38.49	-	mA
	I_{DD_IOVDD}		-	0.04	-	mA
Active current **(Parallel)**	I_{DD_AVDD}	Video@30FPS full resolution PN9	-	12.82	-	mA
	I_{DD_DVDD}		-	31.35	-	mA
	I_{DD_IOVDD}		-	8.23	-	mA
Hardware shutdown current	I_{DD}	MCLK off	-	0	-	µA
Power Consumption- Internal LDO mode(2)						
Active current **(MIPI)**	I_{DD_AVDD}	Video@30FPS full resolution PN9	-	29.57	-	mA
	I_{DD_DVDD}		-	25.62	-	mA
	I_{DD_IOVDD}		-	0.03	-	mA
Active current **(Parallel)**	I_{DD_AVDD}	Video@30FPS full resolution PN9	-	24.59	-	mA
	I_{DD_DVDD}		-	21.87	-	mA
	I_{DD_IOVDD}		-	8.3	-	mA
Hardware shutdown current	I_{DD}	MCLK off	-	0	-	µA
Digital Inputs (MCLK, SCL, XSHUTDOWN, ID_SEL)						
Input voltage low	V_{IL}	-	GND-0.3	-	$0.3V_{IOVDD}$	V
Input voltage high	V_{IH}	-	$0.7V_{IOVDD}$	-	V_{IOVDD}+0.3	V
Input capacitance	C_{IN}	-	-	4	-	pF
Digital Output (Parallel Data)						
Output voltage low	V_{OL}	-	-	-	$0.2V_{IOVDD}$	V
Output voltage high	V_{OH}	-	$0.8V_{IOVDD}$	-	-	V

Note: (1) Supply used in measure based on nominal supply of AVDD=3.3V, DVDD= 1.2V, IOVDD=3.3V.
(2) Supply used in measure based on nominal supply of AVDD=3.3V, LDO-IN =1.8V, IOVDD=3.3V.

Table 11.3: DC characteristic

11.4 Master clock input characteristic

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Input frequency	MCLK	6	-	27	MHz
Input clock duty cycle	$MCLK_{DUTY}$	45	-	55	%

Table 11.4: Master clock input characteristic

11.5 MIPI characteristic

(T_A=25ºC, C_L<10pF, UI_{INST}=1.3ns)

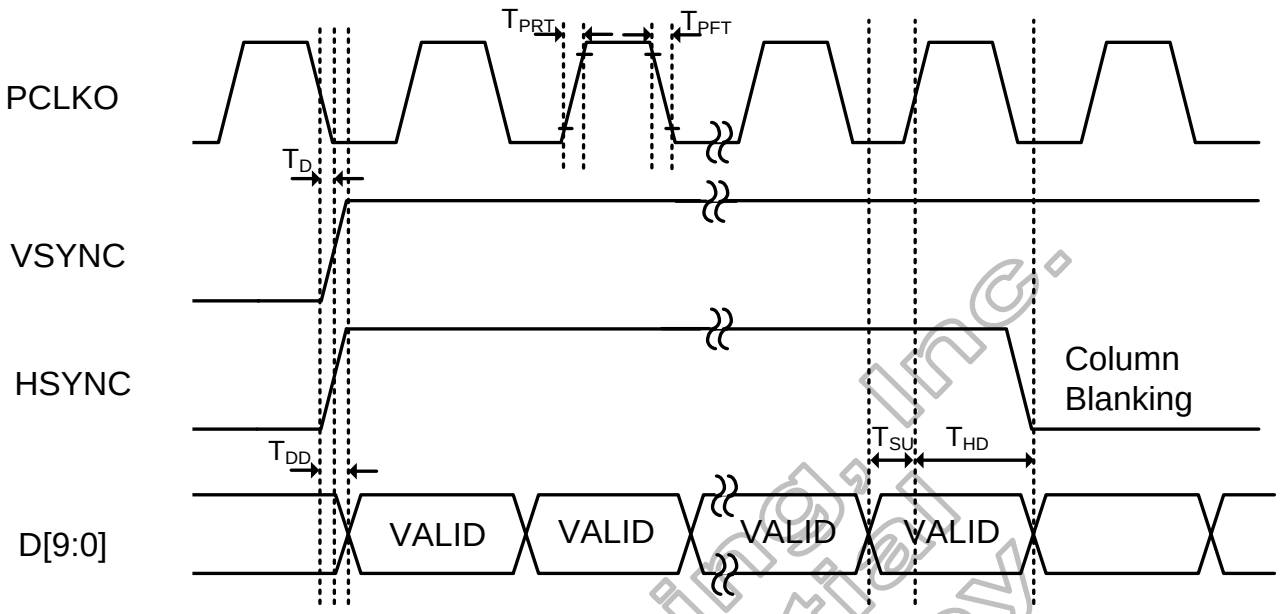
Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
MIPI HS Transmitter Output					
UI instantaneous	UI_{INST}	-	1.3	-	ns
High speed transmitter 20%-80% rise / fall time	T_R	150	-	-	ps
	T_F	-	-	0.3	UI_{INST}
Data to clock skew	T_{SKEW}	-0.15	-	0.15	UI_{INST}
MIPI LP Transmitter Output					
Period of the LP exclusive-OR clock	$T_{LP-PER-TX}$	90	-	-	ns
Low power transmitter 15%-85% rise / fall time	T_{RLP}, T_{FLP}	-	-	25	ns
30%-85% rise / fall time	T_{REOT}	-	-	35	ns

Table 11.5: MIPI timing characteristic

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
MIPI HS Transmitter Output						
HS static common-mode voltage	V_{CMTX}	Range of ZID is 85~120Ω	150	200	250	mV
HS differential voltage	|VOD|	Range of ZID is 85~120Ω	140	200	270	mV
HS output high voltage	V_{OHHS}	Range of ZID is 85~120Ω	-	-	360	mV
Single ended output impedance	Z_{OS}	-	40	50	62.5	Ω
MIPI LP Transmitter Output						
Single-ended output voltage low	V_{OSL}	-	-50	-	50	mV
Single-ended output voltage high	V_{OSH}	-	1.1	1.2	1.3	V

Table 11.6: MIPI interface characteristic

11.6 Parallel characteristic



Note : (1) Conditions: T_A = 25ºC, C_L = 15pF, F_{PLCKO} = 74.25MHz

Figure 11.1: Parallel timing diagram

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
PCLKO period	T_{PLCKO}	-	13.46	-	ns
PCLKO rise time	T_{PRT}	-	4.6	-	ns
PCLKO fall time	T_{PFT}	-	2.67	-	ns
PCLKO falling edge to HSYNC, VSYNC rising edge delay	T_D	-	-1.9	-	ns
PCLKO falling edge to DATA transition delay	T_{DD}	-	1.58	-	ns
Data bus setup time	T_{SU}	-	7.14	-	ns
Data bus hold time	T_{HD}	-	5.54	-	ns

Table 11.7: Parallel timing characteristic

11.7 Serial bus characteristic

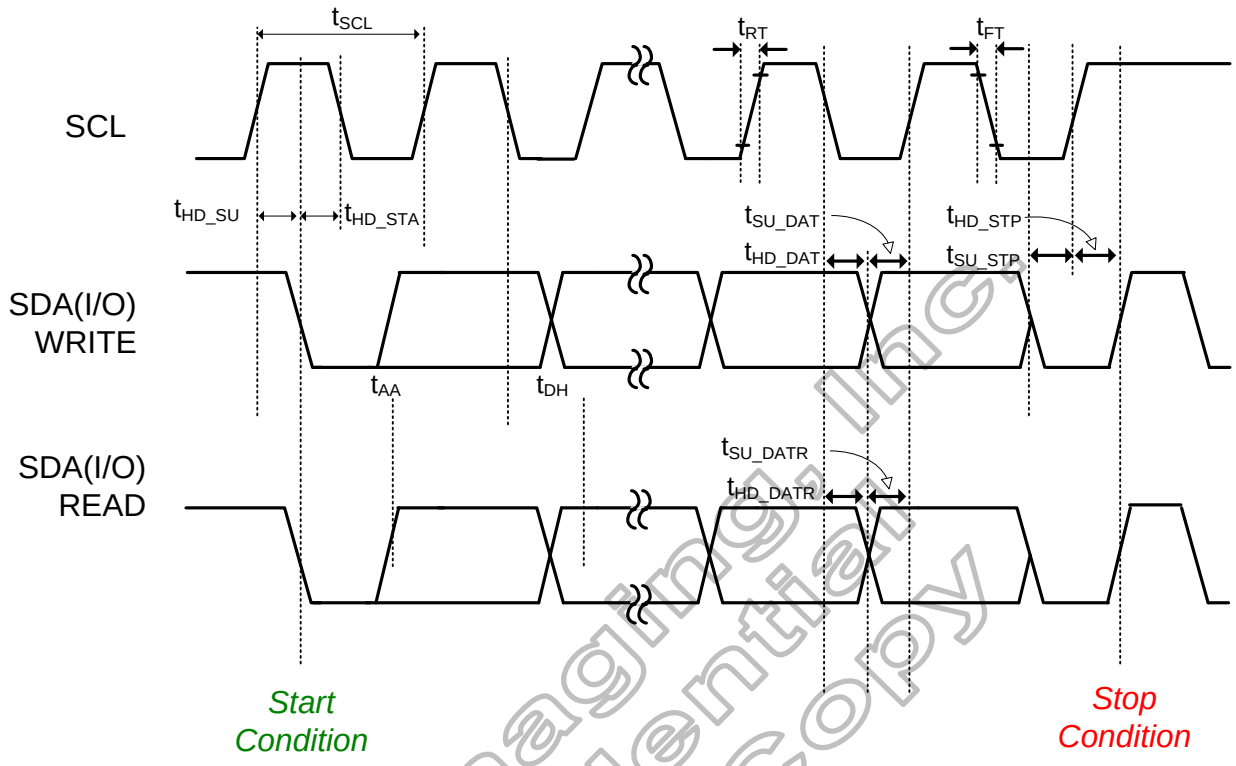


Figure 11.2 2-Wire serial interface timing diagram

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Input clock frequency	F_{SCL}	-	100	-	400	kHz
Input clock period	t_{SCL}	-	2.5	-	10	µs
Input clock duty cycle	-	-	40	50	60	%
Rise time of SCL/SDA	t_{RT}	-	-	-	$0.12t_{SCL}$(1)	ns
Fall time of SCL/SDA	t_{FT}	-	-	-	$0.12t_{SCL}$(1)	ns
Start setup time	t_{HD_SU}	Write	t_{MCLK}(2)	-	-	ns
Start hold time	t_{HD_STA}	Write	$3t_{MCLK}$(2)	-	-	ns
Data hold time	t_{HD_DAT}	Write	5	-	-	ns
Data setup time	t_{SU_DAT}	Write	$3t_{MCLK}$(2)	-	-	ns
Stop setup time	t_{SU_STP}	Write	$3t_{MCLK}$(2)	-	-	ns
Stop hold time	t_{HD_STP}	Write	t_{MCLK}(2)	-	-	ns
Data hold time	t_{HD_DATR}	Read	$3t_{MCLK}$(2)	-	-	ns
Data setup time	t_{SU_DATR}	Read	t_{SCL}(1)/ 2-t_{HD_DATR}	-	-	ns
SDA maximum load capacitance	C_{SDA_LOAD}	-	-	-	4.2	pF
SDA pull-up resistor	R_{SDA}	-	500	-	-	Ω

Note: (1) T_{SCL} = Cycle time of SCL
(2) T_{MCLK}=Cycle time of MCLK.

Table 11.8: SDA / SCL timing characteristic

12. Sensor Chief Ray Angle (CRA)

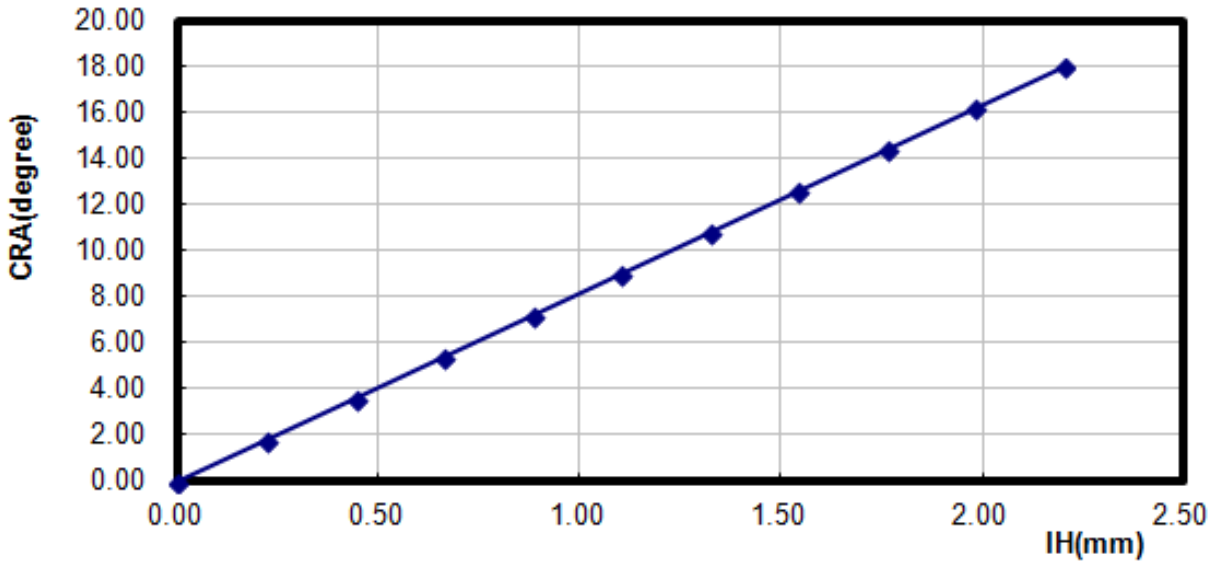


Figure 12.1: Lens CRA profile

Field (%)	Image Height (mm)	CRA (degree)
0.0	0.00	0.00
0.1	0.22	1.80
0.2	0.44	3.60
0.3	0.66	5.40
0.4	0.88	7.20
0.5	1.10	9.00
0.6	1.32	10.80
0.7	1.54	12.60
0.8	1.76	14.40
0.9	1.98	16.20
1.0	2.20	18.00

Table 12.1: CRA profile

13. Quantum Efficiency (QE)

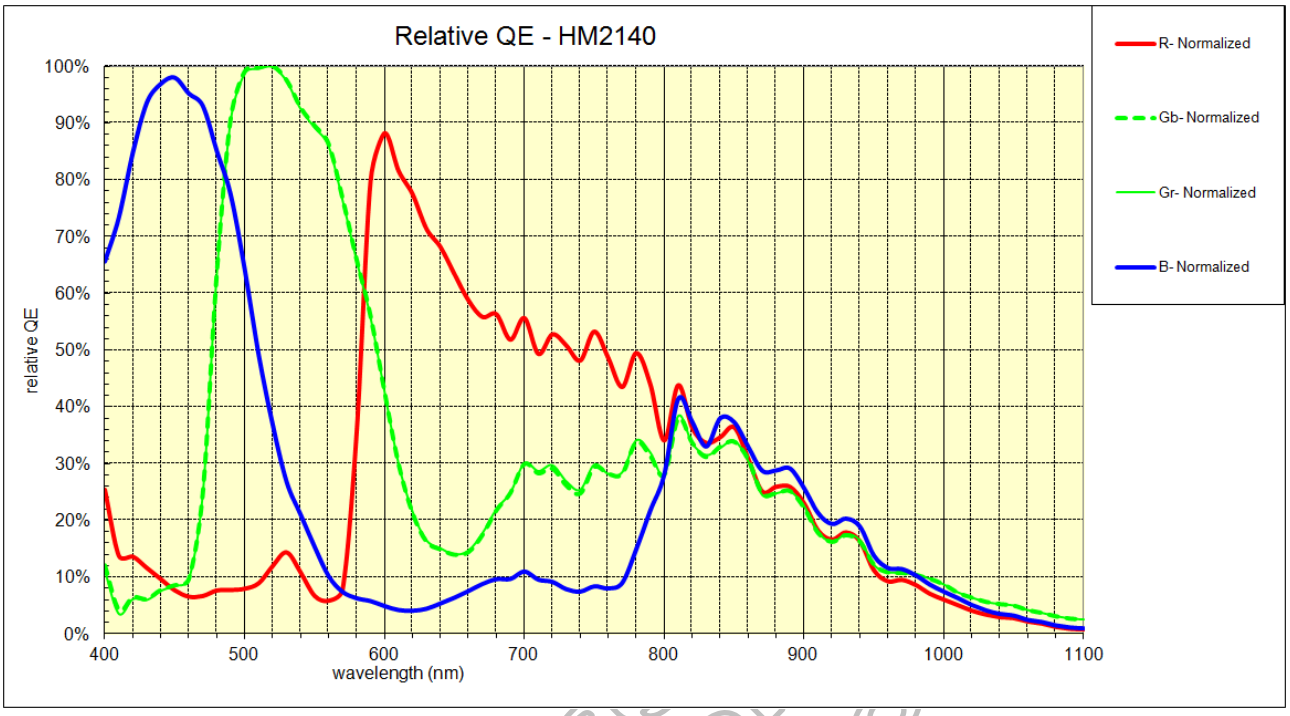


Figure 13.1: Relative QE