GC4103-C62YA CSP

1/3’’ 4Mega CMOS Image Sensor

Assembly Guide

V1.1

2024-11-18

Ordering Information

◆ **GC4103-C62YA**

(Colored, 62PIN-CSP)

GENERATION REVISION HISTORY

Version.	Effective Date	Description of Changes	Prepared by
V1.0	2024-04-23	Document Release	DSC-AE Dept.
V1.1	2024-11-18	Fix Typical application circuit and correct the errors in CSP pin top view	DSC-AE Dept.

Galaxycore Incorporation

Galaxycore Inc. reserves the right to change the contents in this document without prior notice

Content

Figure Content

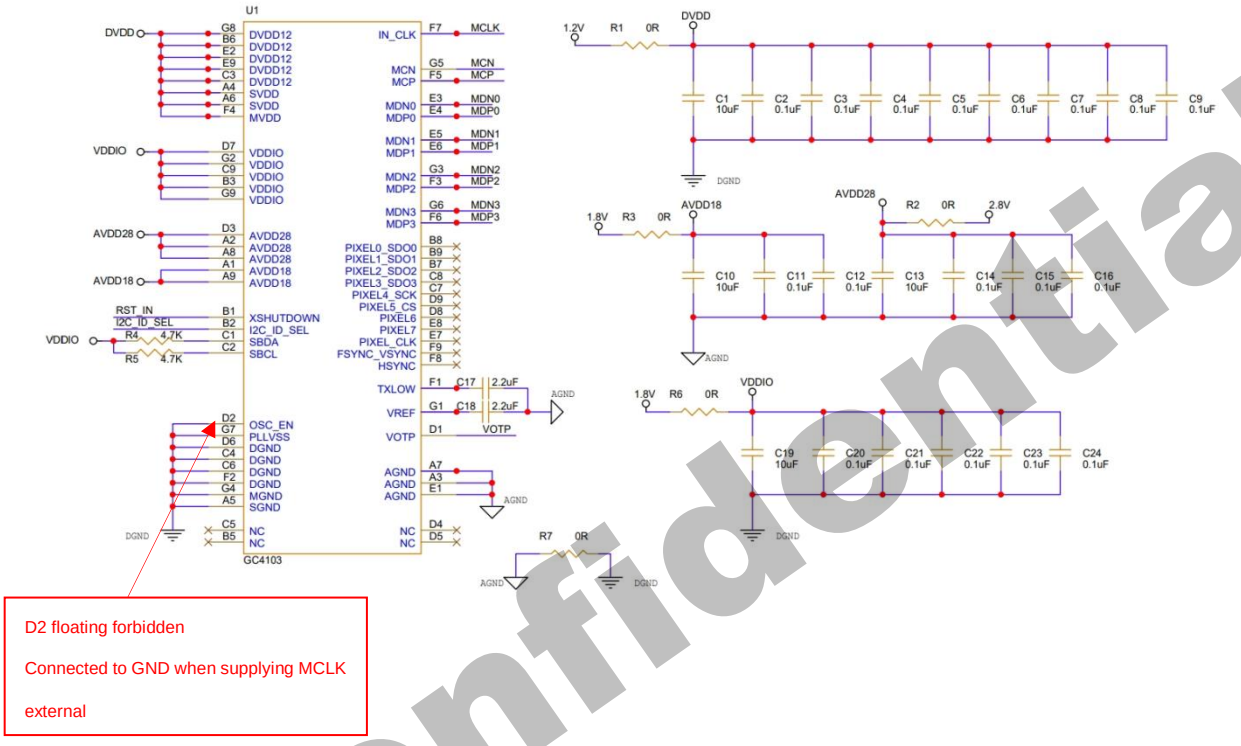
Table content

1. Peripheral circuit reference design

1.1 MIPI 4 lane & DVP & SPI

Figure 1: MIPI 4 lane & DVP & SPI Typical application circuit

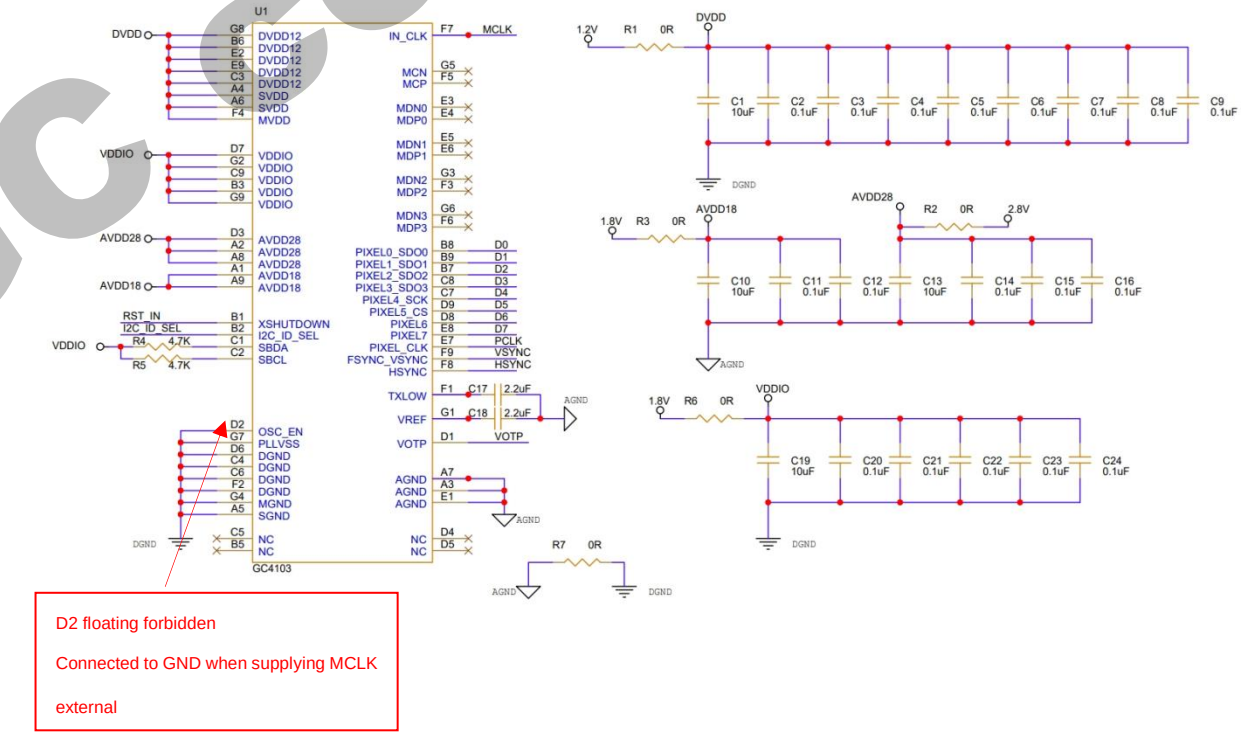
- MIPI



D2 floating forbidden

Connected to GND when supplying MCLK external

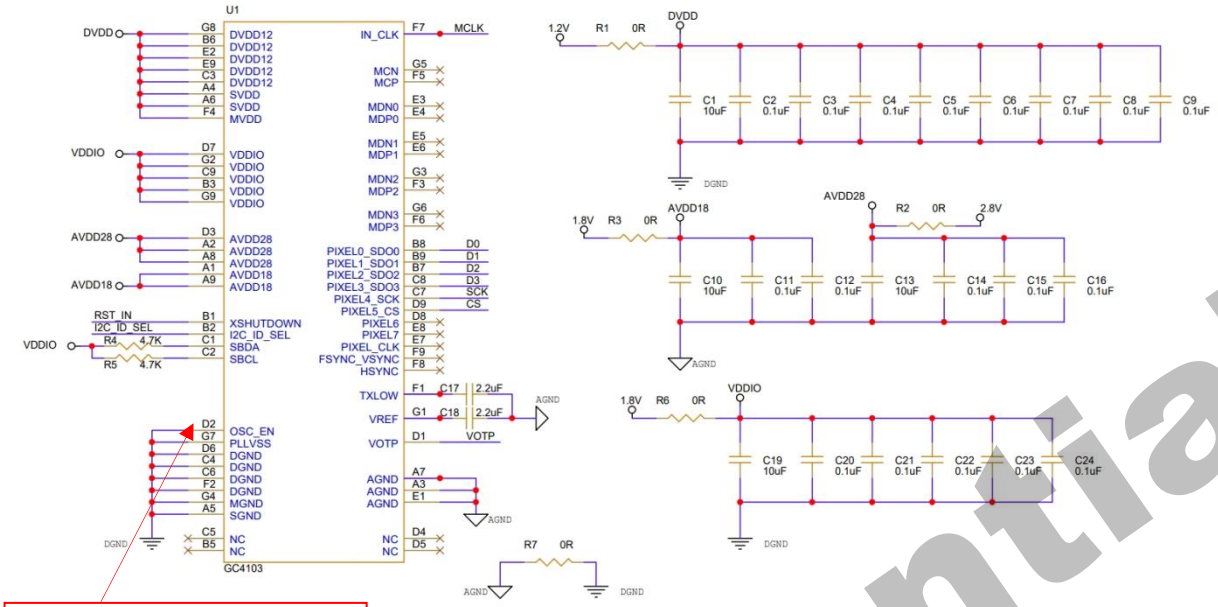
- DVP



D2 floating forbidden

Connected to GND when supplying MCLK external

- SPI



D2 floating forbidden

Connected to GND when supplying MCLK external

2. Peripheral circuit design instructions

- GC4103 Chip requires three power supplies:AVDD28、AVDD18、DVDD12、VDDIO；

  AVDD28 indicates analog power supply, 2.7~2.9V (Typ.2.8V).

  AVDD18 indicates analog power supply, 1.7~1.9V (Typ.1.8V).

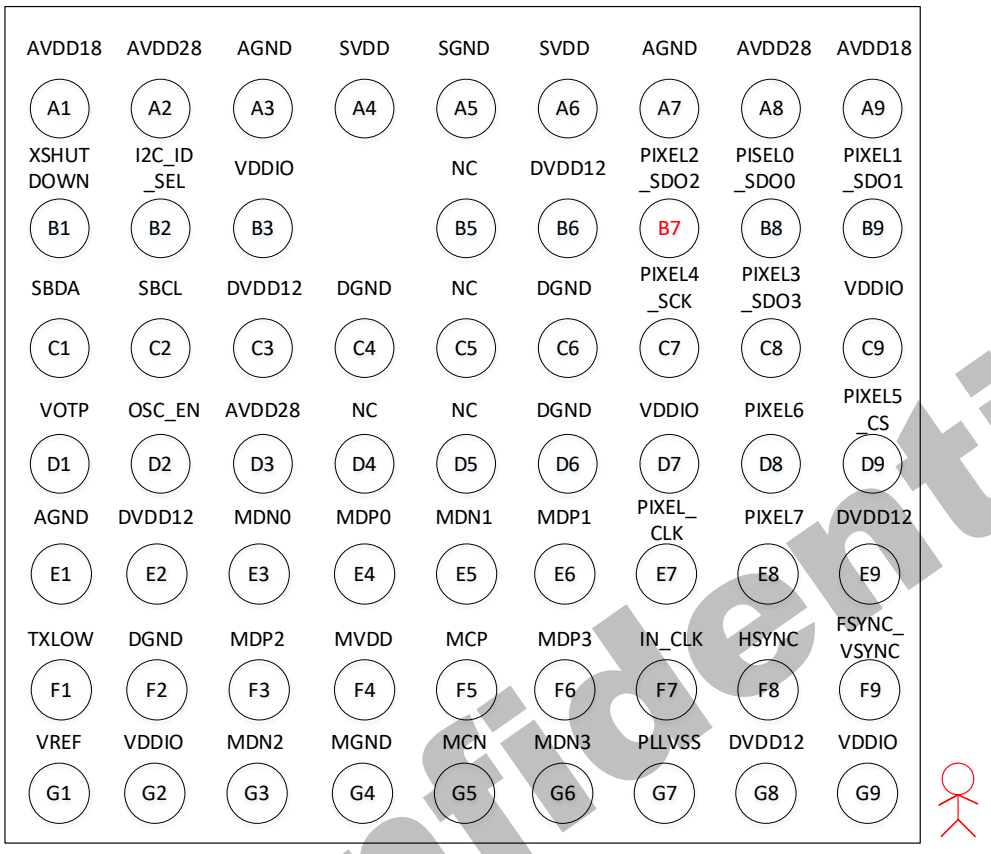
  DVDD12 indicates digital power supply, 1.15~1.25V (Typ. 1.2V)

  VDDIO indicates I/O power supply,1.7~1.9V (Typ.1.8V).
- Add filter capacitors as shown in the figure Close to the power supply, the capacitance value must be set strictly according to the capacitance value marked on the peripheral circuit diagram, otherwise the image quality will be affected;
- All current passes through a 10uf capacitor first, and Try to have a 0.1uf capacitor as close as possible to each power pin.
- The capacitor should be placed as close to the pin as possible;
- All capacitors should not be omitted, otherwise the image quality will be affected;
- AGND should wire separately from DGND, otherwise the image quality will be affected;
- The GND wiring width should be at least 0.2mm，Punch as many holes as possible;
- The power line wiring width should be at least 0.2mm；
- The chip has XSHUTDOWN pin, which need to be controlled;
- MCP、MCN、MDP and MDN should wire equal length lines parallelly; As few or no holes as possible; And away from high frequency signal lines (such as MCLK), it is best to use ground wire protection。And the back of differential pairs wiring is also using ground wire protection, and paving copper as a reference layer. The matching impedance of differential pairs is required to be 100Ω±10%;

- MCP、MCN should wire equal length lines with those of MDP and MDN of different groups;
- The distance between MDP and MDN of different groups should be at least twice the line width.

3. CSP Package Specifications

Figure 2: CSP Pin Top View



3.1 Pin Descriptions

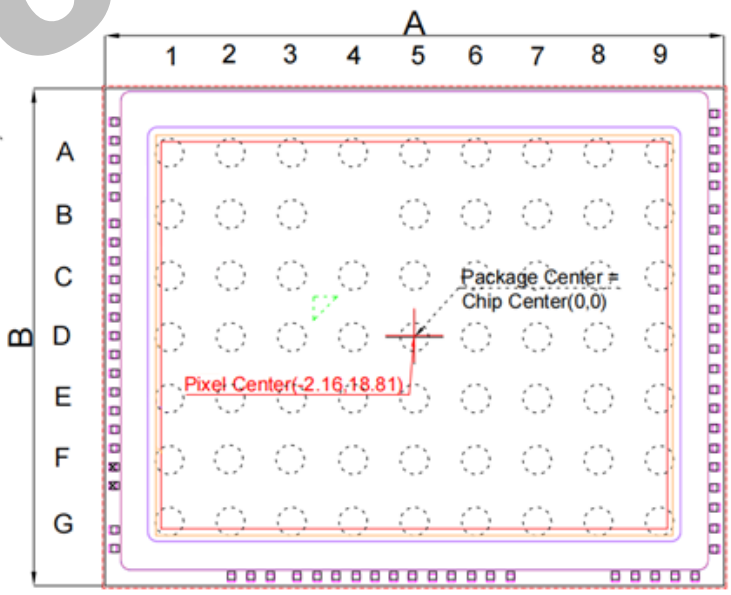
Table 1: Pin Descriptions

Pin	Name	Type	A/D	Description
A1	AVDD18	Power	D	Analog power supply:1.8V
A2	AVDD28	Power	A	Analog power supply:2.8V
A3	AGND	Ground	A	Ground for analog
A4	SVDD	Power	D	Digital power supply:1.2V
A5	SGND	Ground	D	Ground for digital
A6	SVDD	Power	D	Digital power supply:1.2V
A7	AGND	Ground	D	Ground for analog
A8	AVDD28	Power	A	Analog power supply:2.8V
A9	AVDD18	Power	A	Analog power supply:1.8V
B1	XSHUTDOWN	Input	D	Sensor power down control: (floating forbidden) 0: reset & standby; 1: normal work
B2	I2C_ID_SEL	Input	D	ID_SEL（floating forbidden）. 0:0x62, 1:0x20

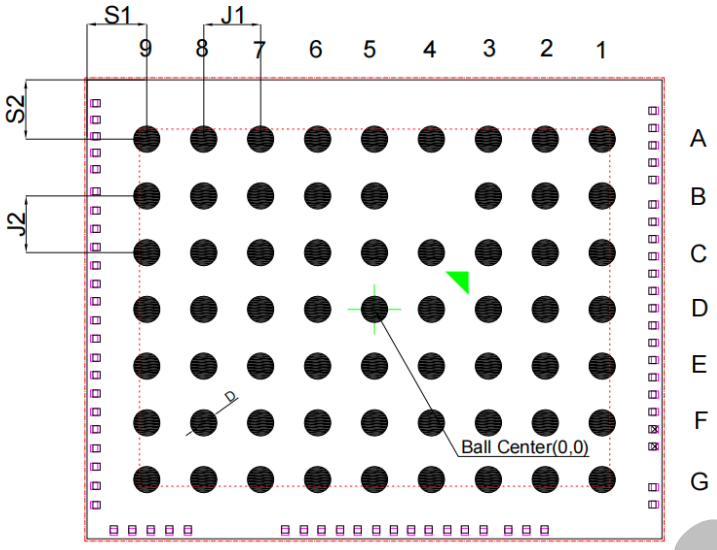
Pin	Name	Type	A/D	Description
B3	VDDIO	Power	D	I/O Power supply:1.8V
B4	/	/		/
B5	NC	NC		NC
B6	DVDD12	Power	D	Digital power supply:1.2V
B7	PIXEL2_SDO2	Output	D	DVP/SPI data <2>
B8	PIXEL0_SDO0	Output	D	DVP/SPI data <0>
B9	PIXEL1_SDO1	Output	D	DVP/SPI data <1>
C1	SBDA	Input/Output	D	Two-wire serial bus, data
C2	SBCL	Input	D	Two-wire serial bus, clock
C3	DVDD12	Power	D	Digital power supply:1.2V
C4	DGND	Ground	D	Ground for digital
C5	NC	NC		NC
C6	DGND	Ground	D	Ground for digital
C7	PIXEL4_SCK	Output	D	DVP data <4>/SPI clock
C8	PIXEL3_SDO3	Output	D	DVP/SPI data <3>
C9	VDDIO	Power	D	I/O Power supply:1.8V
D1	VOTP	Power	D	OTP power supply: 7V (floating available)
D2	OSC_EN	Input	D	Internal OSC supply (floating forbidden) Connected to GND when supplying MCLK external
D3	AVDD28	Power	A	Analog power supply:2.8V
D4	NC	NC		NC
D5	NC	NC		NC
D6	DGND	Ground	D	Ground for digital
D7	VDDIO	Power	D	I/O Power supply:1.8V
D8	PIXEL6	Output	D	DVP data <6>
D9	PIXEL5_CS	Output	D	DVP data <5>/SPI CS
E1	AGND	Ground	D	Ground for analog
E2	DVDD12	Power	D	Digital power supply:1.2V
E3	MDN0	Output	D	MIPI data <0> (-).
E4	MDP0	Output	D	MIPI data <0> (+).
E5	MDN1	Output	D	MIPI data <1> (-).
E6	MDP1	Output	D	MIPI data <1> (+).
E7	PIXEL_CLK	Output	D	DVP clock
E8	PIXEL7	Output	D	DVP data <7>

Pin	Name	Type	A/D	Description
E9	DVDD12	Power	D	Digital power supply:1.2V
F1	TXLOW	Power	A	Internal power supply.
F2	DGND	Ground	D	Ground for digital
F3	MDP2	Output	D	MIPI data <2> (+)
F4	MVDD	Power	D	Digital power supply:1.2V
F5	MCP	Output	D	MIPI clock (+)
F6	MDP3	Output	D	MIPI data <3> (+)
F7	IN_CLK	Input	D	Sensor input clock
F8	HSYNC	Output	D	Horizontal sync control
F9	FSYNC_VSYNC	Input/Output	D	Frame sync control/Vertical sync control
G1	VREF	Power	A	Internal power supply.
G2	VDDIO	Power	D	I/O power supply:1.8V
G3	MDN2	Output	D	MIPI data <2> (-)
G4	MGND	Ground	D	Ground for digital
G5	MCN	Output	D	MIPI clock (-)
G6	MDN3	Output	D	MIPI data <3> (-)
G7	PLLVSS	Ground	D	Ground for PLL
G8	DVDD12	Power	D	Digital power supply:1.2V
G9	VDDIO	Power	D	I/O power supply:1.8V

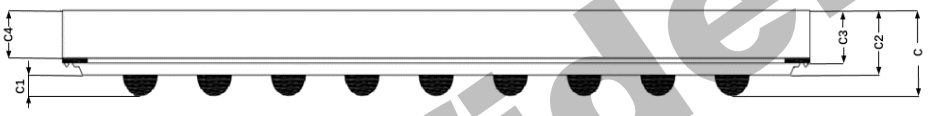
Figure 3: Mechanical Drawing View(μm)



Top View(Bumps Down)



Back View(Bumps Up)



Side View

Table 2: Package Specifications

Description	symbol	Nominal	Min	Max
		Millimeters		
Package Body Dimension X	A	6.564	6.539	6.589
Package Body Dimension Y	B	5.259	5.234	5.284
Package Height	C	0.676	0.621	0.731
Ball Height	C1	0.150	0.120	0.180
Package Body Thickness	C2	0.526	0.491	0.561
Thickness from top glass surface to wafer	C3	0.345	0.330	0.360
Glass Thickness	C4	0.300	0.290	0.310
Ball Diameter	D	0.300	0.270	0.330
Total Ball Count	N	62(4NC)		
Ball Count X axis	N1	9		
Ball Count Y axis	N2	7		
Pins pitch X axis	J1	0.650	0.640	0.660
Pins pitch Y axis	J2	0.650	0.640	0.660
BGA ball center to package center offset in X-	X	0.000	-0.025	0.025

Description	symbol	Nominal	Min	Max
		Millimeters		
direction				
BGA ball center to package center offset in Y-direction	Y	0.000	-0.025	0.025
BGA ball center to chip center offset in X-direction	X1	0.000	-0.025	0.025
BGA ball center to chip center offset in Y-direction	Y1	0.000	-0.025	0.025
Edge to Pin Center Distance along X1	S1	0.682	0.652	0.712
Edge to Pin Center Distance along Y1	S2	0.6795	0.6495	0.7095

Note: The package center, optical center, and BGA center of the chip are not coincident. If setting the package center as the origin (0, 0), the BGA center coordinate is (0, 0), the optical center coordinate is (-2.16, 18.81), with μm unit.

4. CSP Module Image Direction

Figure 4: Schematic diagram of module imaging