GC4033-C43YA CSP

1/3’’ 4Mega CMOS Image Sensor

Datasheet

Preliminary

V0.1

2024-05-30

Ordering Information

◆ **GC4033-C43YA**

(Colored, 43PIN-CSP)

GENERATION REVISION HISTORY

Version.	Effective Date	Description of Changes	Prepared by
V0.0	2024-03-01	Document Release	DSC-AE Dept.
V0.1	2024-05-30	Update P7 power supply requirement &P8 table2&P10 table6	DSC-AE Dept.

Galaxycore Incorporation

Content

Figure Content

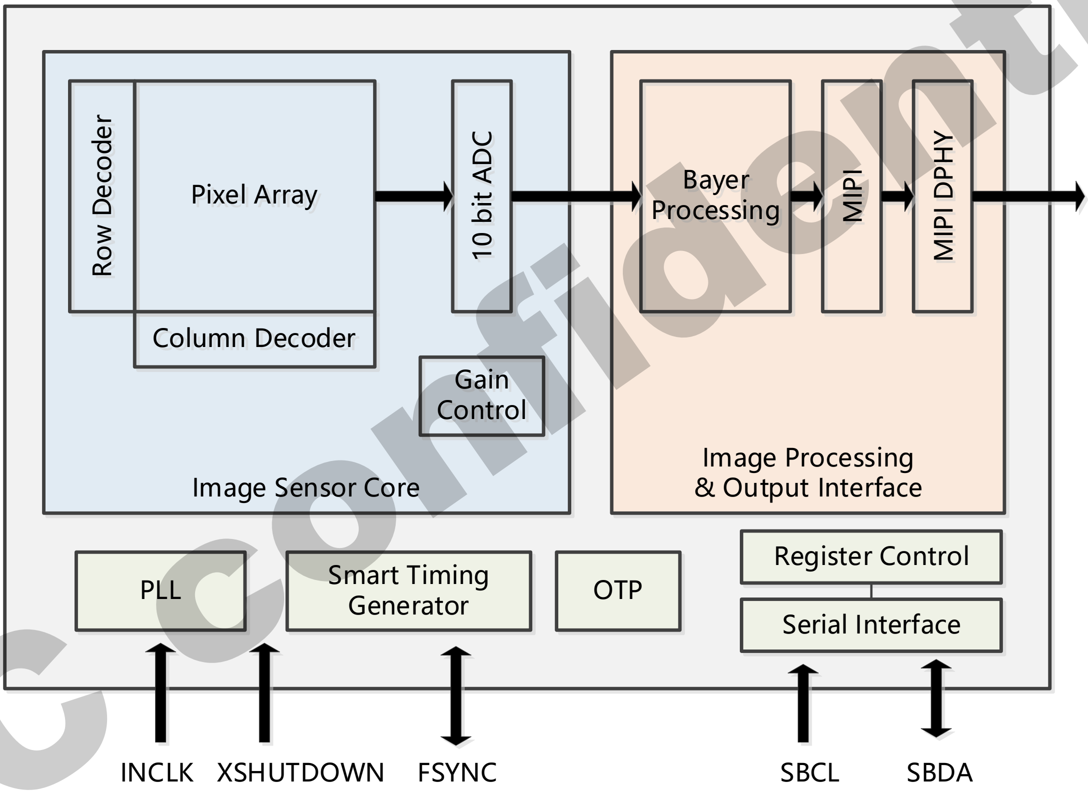
Table Content

1. Sensor Overview

1.1 General Description

GC4033 is a high quality 4Mega CMOS image sensor, for Smart Home Systems, IoT Cameras, Car Driving Recorders applications. GC4033 incorporates a 2560H x 1440V active pixel array, on-chip 10-bit ADC, and image signal processor. It is programmable through a simple two-wire serial interface and has very low power consumption. It provides RAW10 data formats with MIPI interface.

Figure 1: Block Diagram



1.2 Features

◆ Optical size:	1/3 inch
◆ Pixel size:	2.0μm x 2.0μm FSI
◆ Active image size:	2560 x 1440
◆ Color Filter:	RGB Bayer
◆ Output formats:	Raw Bayer 10bit
◆ Power supply requirement:	AVDD28: 2.7~2.9V (Typ. 2.8V)
	DVDD: 1.15~1.25V (Typ. 1.2V)
	IOVDD: 1.7~1.9V (Typ. 1.8V)
◆ Power Consumption:	122mW @Full Size @30fps
◆ Frame rate:	60fps@Full Size
◆ PLL support	
◆ Frame sync support (master/slave)	
◆ DAG HDR support	
◆ Windowing support	
◆ Mirror and Flip support	
◆ Binning Mode support	
◆ OTP support	
◆ Analog Gain:	64X(Max)
◆ Sensitivity:	TBD
◆ Dynamic range:	TBD
◆ MAX SNR:	37 dB
◆ Dark Current:	TBD
◆ Micro lens chief ray angle (CRA):	15°(linear)
◆ Operation Temperature:	-30~85℃
◆ Stable Image temperature:	-20~60℃
◆ Storage temperature:	-40~125℃
◆ Package:	CSP

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

Description	Symbol	Rating	Unit	Note
Analogue absolute max	V_{AVDD_MAX}	-0.3~3.9	V	Refer to GND
Digital absolute voltages	V_{DVDD_MAX}	-0.3~1.8	V	
IO absolute max	V_{IOVDD_MAX}	-0.3~3.6	V	
Digital input voltages	V_{IF_MAX}	-0.3~V_{IOVDD}+0.3	V	

Note: Digital input voltage: XCLK, SBCL, SBDA, XSHUTDOWN, FSYNC

2.2 Operation Conditions

Table 2: Operation Conditions

Description	Symbol	Min.	Typical	Max.	Unit
Analog power supply	V_{AVDD}	2.7	2.8	2.9	V
Digital power supply	V_{DVDD}	1.15	1.2	1.25	V
IO power supply	V_{IOVDD}	1.7	1.8	1.9	V
Digital input voltages	V_{IF}	0		IOVDD	V
Test temperature	T_{TEST}	21	25	27	℃

Note: 1. Digital input voltage: XCLK, SBCL, SBDA, XSHUTDOWN, FSYNC.
2. Test temperature: image quality test condition.

2.3 DC Characteristics

Table 3: DC Characteristics

Characteristics	Symbol	Min.	Typical	max	Unit
Input voltage HIGH	V_{IH}	0.7 x V_{IF}	-	-	V
Input voltage Low	V_{IL}	-	-	0.3 x V_{IF}	V
Output voltage HIGH	V_{OH}	0.7 x V_{IOVDD}	-	-	V
Output voltage LOW	V_{OL}	-	-	0.3 x V_{IOVDD}	V

Note: Input voltage apply to XCLK, SBCL, SBDA, XSHUTDOWN, FSYNC.

2.4 AC Characteristics

Figure 2: AC Characteristics

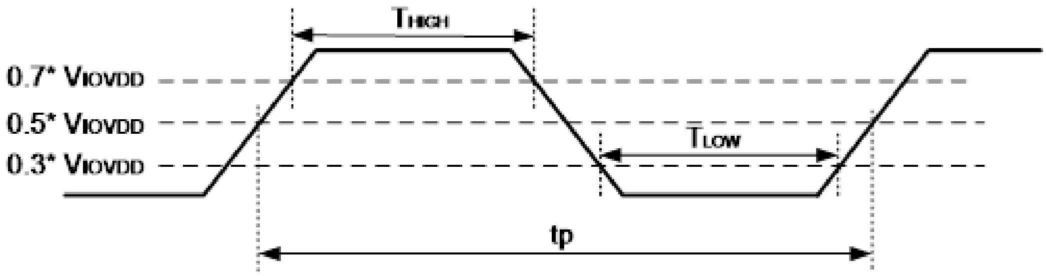


Table 4: AC Characteristics

Item	Symbol	Min.	Typ.	max	unit
Frequency	f_{SCK}	6	27	36	MHz
jitter (period, peak-to-peak)	T_{jitter}			600	ps
High level width	T_{HIGH}	0.4tp		0.6tp	ns
Low level width	T_{LOW}	0.4tp		0.6tp	ns
Duty Cycle	f_{DUTY}	40		60	%

2.5 Power Consumption

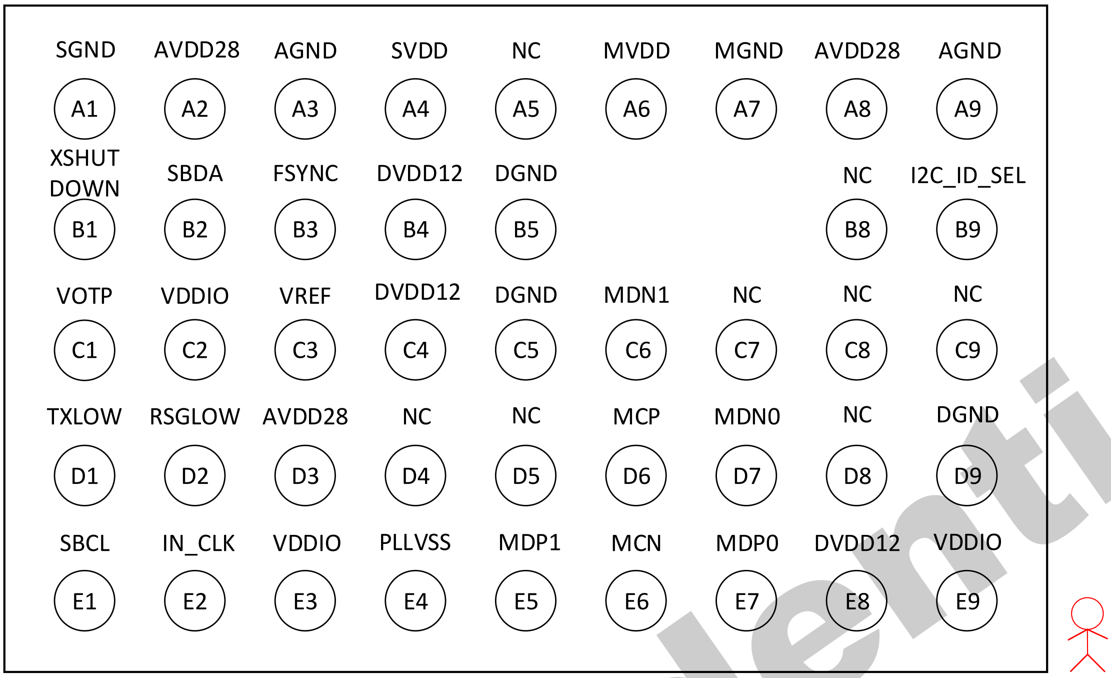
Table 5: Power Consumption

Item	Symbol	Min	Typ	Max	Unit
Full size @30fps MIPI 2lane	I_{AVDD}	-	13.5	-	mA
	I_{DVDD}		59		mA
	I_{IOVDD}	-	7.8	-	mA
Standby current	I_{AVDD}	-	0.3	-	μA
	I_{DVDD}		755		μA
	I_{IOVDD}	-	15	-	μA
Power off current	I_{total}	-	-	0	μA

Note: 1. All operate current are measured at 24MHz XCLK.
2. Standby current is measured at XSHUTDOWN = L, XCLK=24MHz.
3. We recommend that power should be turned off, when lower power consumption is required.

3. CSP Package Specifications

Figure 3: CSP Pin Top View



3.1 Pin Descriptions

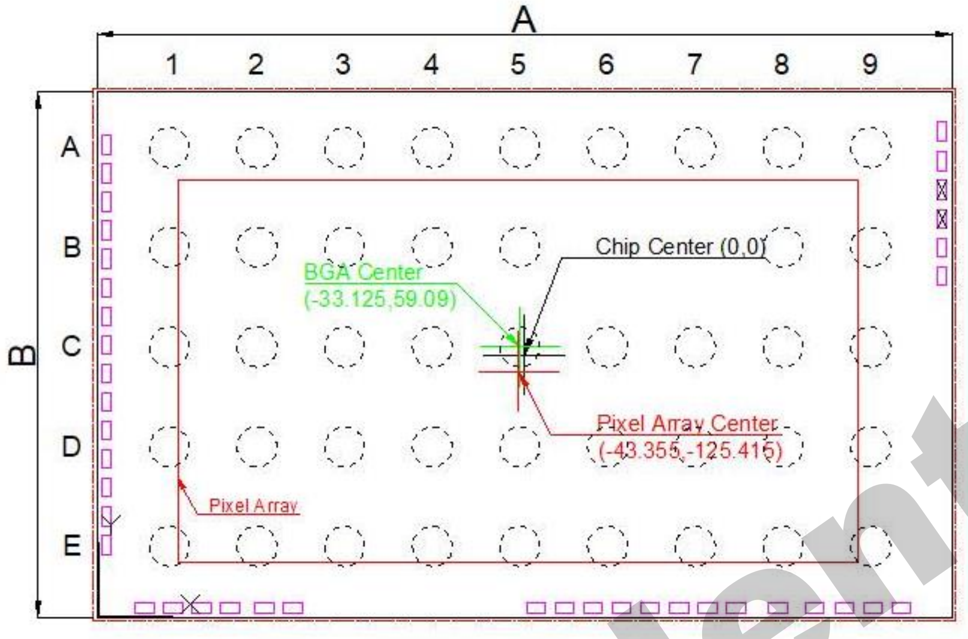
Table 6: Pin Descriptions

Pin	Name	Type	A/D	Description
A1	SGND	Ground	D	Ground for SRAM
A2	AVDD28	Power	A	Analog power supply:2.8V
A3	AGND	Ground	A	Ground for analog
A4	SVDD	Power	D	1.2V POWER for SRAM
A5	NC	NC		NC
A6	MVDD	Power	D	1.2V POWER for MIPI
A7	MGND	Ground	D	Ground for MIPI
A8	AVDD28	Power	A	Analog power supply:2.8V
A9	AGND	Ground	A	Ground for analog
B1	XSHUTDOWN	Input	D	Sensor power down control: (floating forbidden) 0: reset & standby; 1: normal work
B2	SBDA	Input\ Output	D	Two-wire serial bus, data.
B3	FSYNC	Input\ Output	D	Frame sync control
B4	DVDD12	Power	D	Digital power supply:1.2V
B5	DGND	Ground	D	Ground for digital
B6	\	\		\
B7	\	\		\
B8	NC	NC		NC

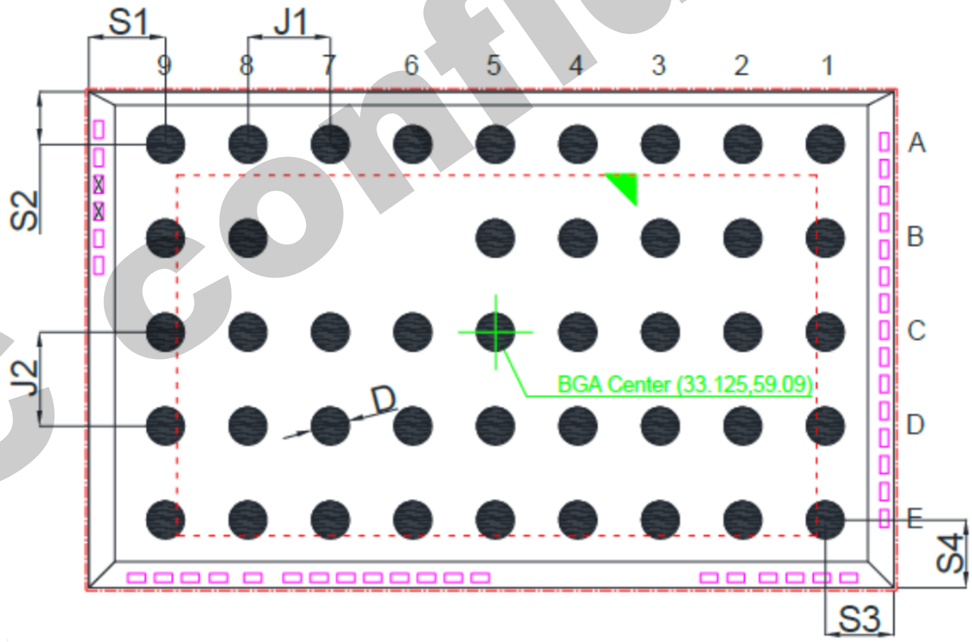
Pin	Name	Type	A/D	Description
B9	I2C_ID_SEL	Input	D	ID SEL(floating forbidden). 0(default):0x62/0x63；1:0x20/0x21
C1	VOTP	Power	D	OTP power supply: 6.5V (floating available)
C2	VDDIO	Power	D	I/O Power supply:1.8V
C3	VREF	Power	A	Internal power supply.
C4	DVDD12	Power	D	Digital power supply:1.2V
C5	DGND	Ground	D	Ground for digital
C6	MDN1	Output	D	MIPI OUTPUT
C7	NC	NC		NC
C8	NC	NC		NC
C9	NC	NC		NC
D1	TXLOW	Power	A	Internal power supply.
D2	RSGLOW	Power	A	Internal power supply.
D3	AVDD28	Power	A	Analog power supply:2.8V
D4	NC	NC		NC
D5	NC	NC		NC
D6	MCP	Output	D	MIPI OUTPUT
D7	MDN0	Output	D	MIPI OUTPUT
D8	NC	NC		NC
D9	DGND	Ground	D	Ground for digital
E1	SBCL	Input	D	Two-wire serial bus, clock.
E2	INCLK	Input	D	Sensor input clock
E3	VDDIO	Power	D	I/O Power supply:1.8V
E4	PLLVSS	Ground	D	Ground for PLL_MIPI
E5	MDP1	Output	D	MIPI OUTPUT
E6	MCN	Output	D	MIPI OUTPUT
E7	MDP0	Output	D	MIPI OUTPUT
E8	DVDD12	Power	D	Digital power supply:1.2V
E9	VDDIO	Power	D	I/O Power supply:1.8V

3.2 Package Specification

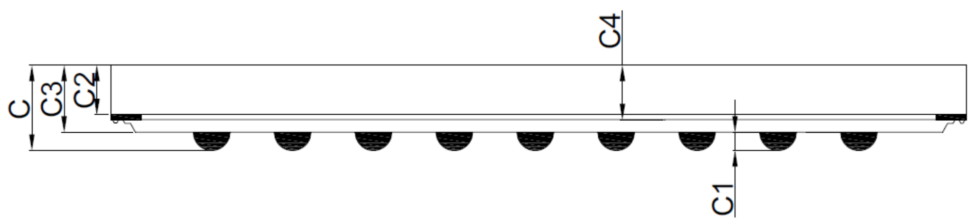
Figure 4: Mechanical Drawing View(μm)



Top View(Bumps Down)



Back View(Bumps Up)



Side View

Table 7: Package Specifications

Description	symbol	Nominal	Min	Max
		Millimeters		
Package Body Dimension X	A	6.437	6.412	6.462
Package Body Dimension Y	B	3.956	3.931	3.981
Package Height	C	0.650	0.595	0.705
Ball Height	C1	0.150	0.120	0.180
Glass Thickness	C2	0.300	0.290	0.310
Package Body Thickness	C3	0.500	0.465	0.535
Thickness from top glass surface to wafer	C4	0.345	0.325	0.365
Ball Diameter	D	0.300	0.270	0.330
Total Ball Count	N	43(8NC)		
Ball Count X axis	N1	9		
Ball Count Y axis	N2	5		
Pins pitch X axis	J1	0.660		
Pins pitch Y axis	J2	0.750		
BGA ball center to package center offset in X-direction	X	-0.033125	-0.0581	-0.0081
BGA ball center to package center offset in Y-direction	Y	0.05909	0.0341	0.0841
BGA ball center to chip center offset in X-direction	X1	-0.033125	-0.0581	-0.0081
BGA ball center to chip center offset in Y-direction	Y1	0.05909	0.0341	0.0841
Edge to Pin Center Distance along X	S1	0.611625	0.582	0.642
Edge to Pin Center Distance along Y	S2	0.41891	0.389	0.449
Edge to Pin Center Distance along X1	S3	0.545375	0.515	0.575
Edge to Pin Center Distance along Y1	S4	0.53709	0.507	0.567

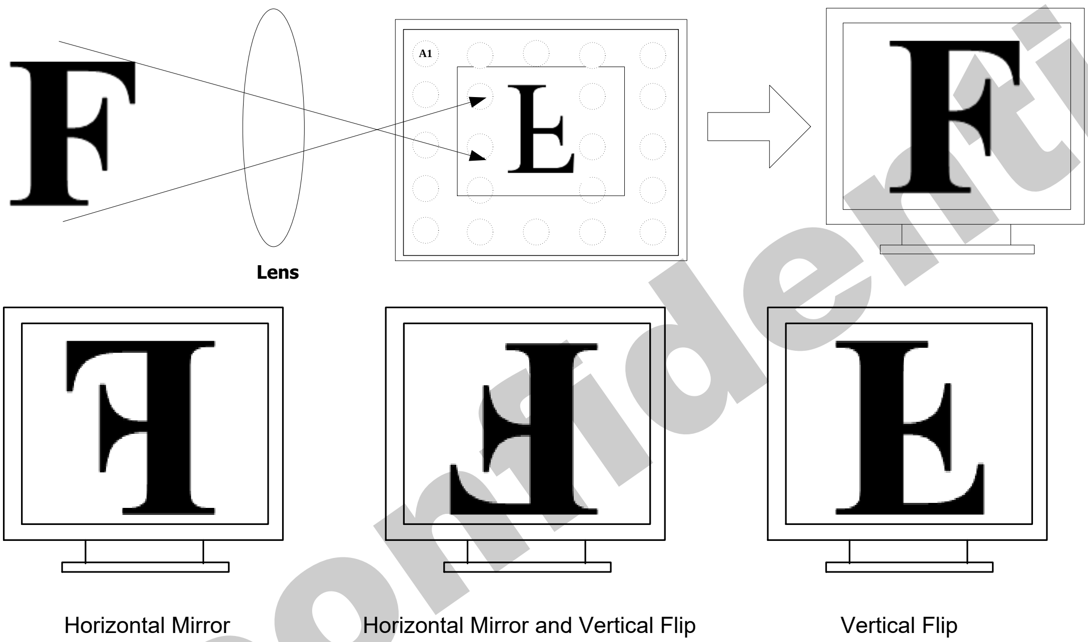
Note: The package center, optical center, and BGA center of the chip are not coincident. If setting the package center as the origin (0, 0), the BGA center coordinate is (-33.125, 59.09), the optical center coordinate is (-43.355, -125.415), with μm unit.

4. Optical Specifications

4.1 Readout Position

GC4033 default status is readout from the lower left corner with pin A1 located in the upper left corner. The image is inverted vertically and horizontally by the lens, so proper image output results when Pin A1 is located in the upper left corner.

Figure 5: Readout Position



Readout direction can be set by the registers.

Table 8: Mirror and Flip Information

Function	Register Address	Register Value	First Pixel
Normal	0x022c[1:0]	00	R
Horizontal mirror	0x022c[1:0]	01	Gr
Vertical Flip	0x022c[1:0]	10	Gb
Horizontal Mirror and Vertical Flip	0x022c[1:0]	11	B

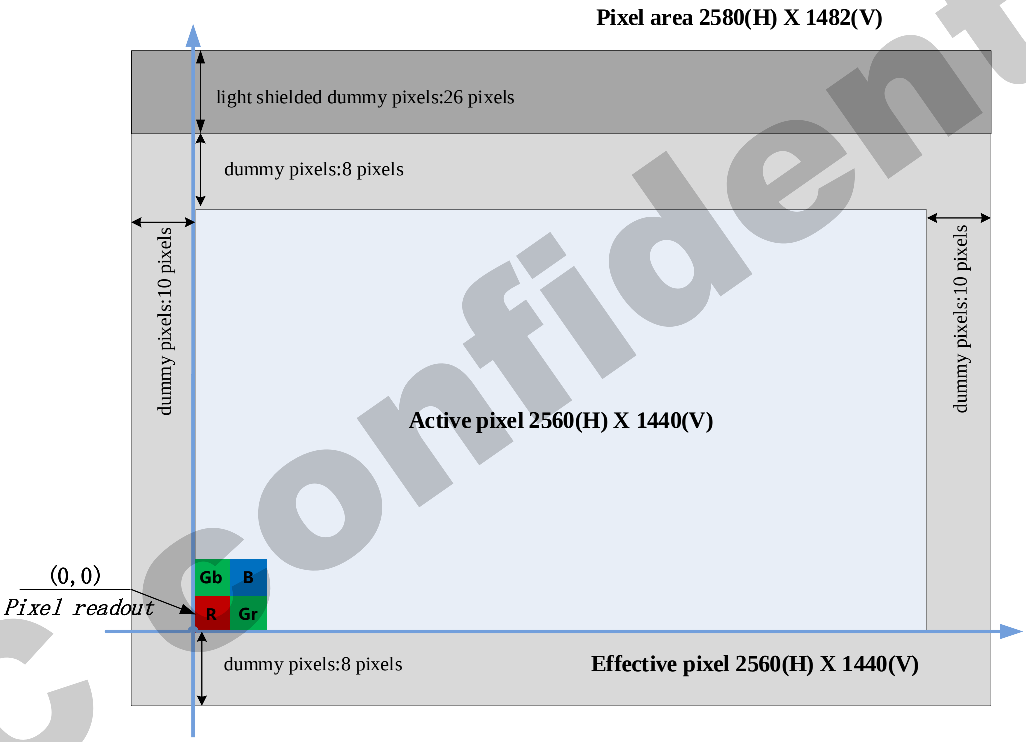
4.2 Pixel Array

Pixel array is covered by Bayer pattern color filters. The primary color GR/BG array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 2559. If flip in column, column is read out from 2559 to 0.

If no flip in row, row is read out from 0 to 1439. If flip in row, row is read out from 1439 to 0.

Figure 6: Pixel Array



4.3 Lens Chief Ray Angle (CRA)

Figure 7 CRA Information

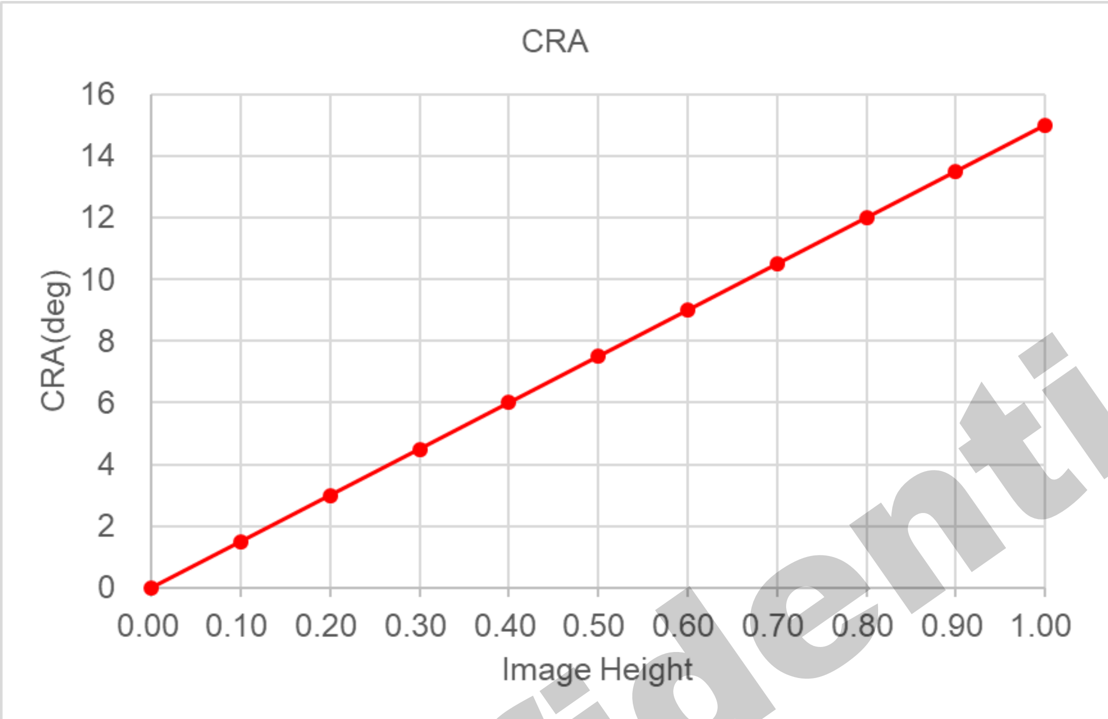


Table 9: CRA Information

Image Heigh (%)	Image Height (mm)	CRA (degree)
00	0.000	0.000
10	0.294	1.500
20	0.587	3.000
30	0.881	4.500
40	1.175	6.000
50	1.469	7.500
60	1.762	9.000
70	2.056	10.500
80	2.350	12.000
90	2.643	13.500
100	2.937	15.000

4.4 QE Spectral Characteristics

The optical spectrum of QE is below:

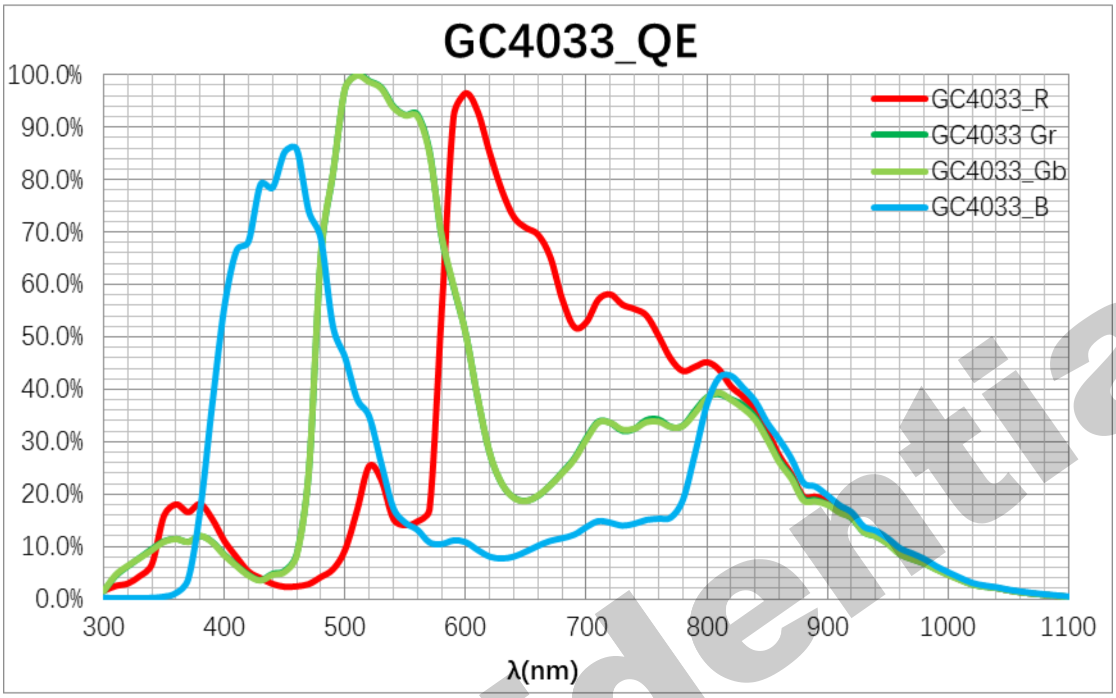


Figure 8 QE curve

5. Two-wire Serial Bus Communication

GC4033 Device Address:

Table 10: Device ID

ID_SEL	Slave address write mode	Slave address read mode
0(default)	0x62	0x63
1	0x20	0x21

NOTE: When IDSEL0/IDSEL1 is "High", it means connect to IOVDD. When IDSEL0/IDSEL1 is "Low", you should connect it to DGND.

5.1 Protocol

The host must perform the role of a communications master and GC4033 acts as either a slave receiver or transmitter. The master must do:

- Generate the Start(S)/Stop(P) condition
- Provide the serial clock on SBCL

Figure 9: Write operate (2 bytes address –1byte data format)

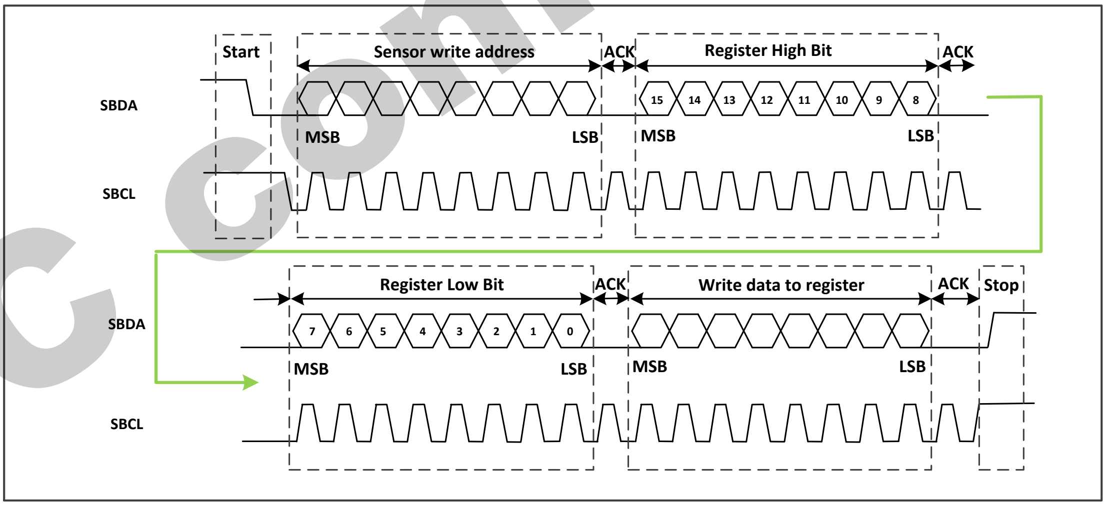
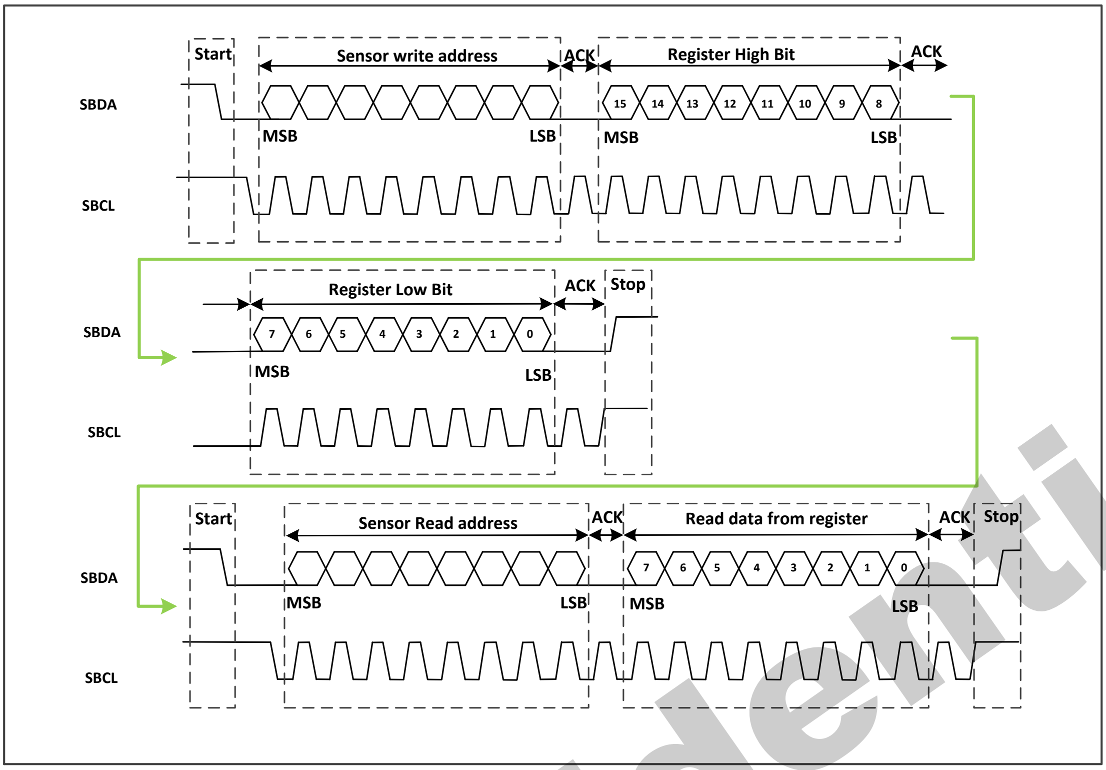


Figure 10: Read Operate (2 bytes address –1byte data format)



5.2 Serial Bus Timing

Figure 11: Serial Bus Timing

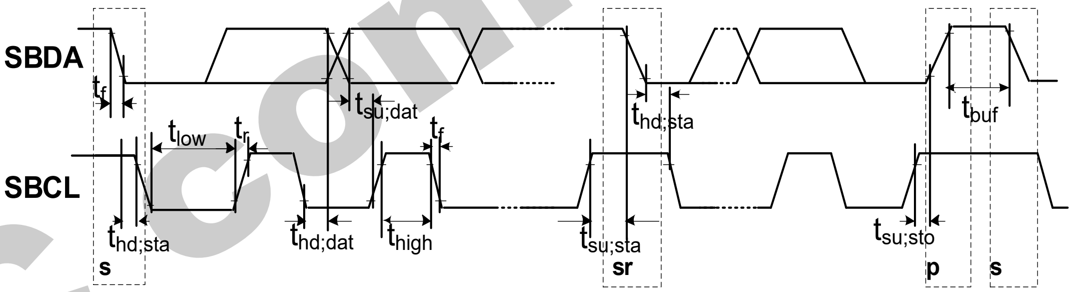


Table 11: Serial Bus Timing

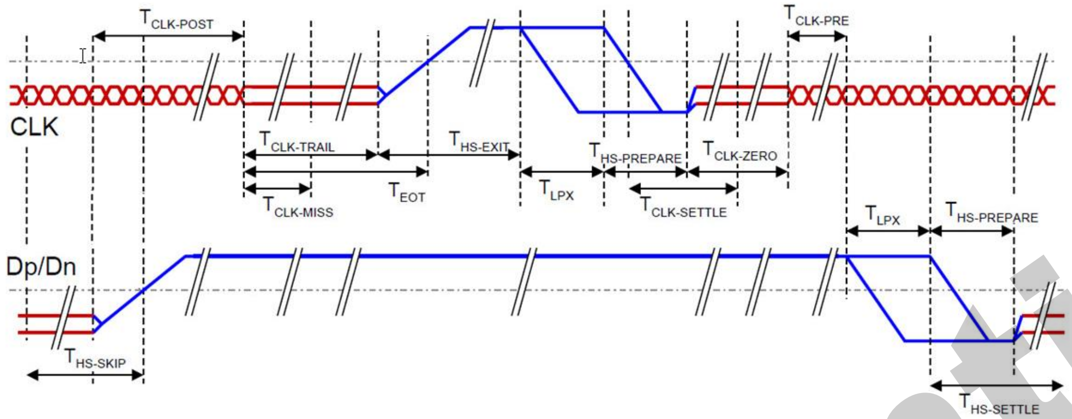
Parameter	Symbol	Min	Typ.	Max	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between a stop and a start	t_{buf}	1.3	--	--	µs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	µs
LOW period of SBCL	t_{low}	1.3	--	--	µs
HIGH period of SBCL	t_{high}	0.6	--	--	µs
Set-up time for a repeated start	$t_{su;sta}$	600	--	--	ns
Data hold time	$t_{hd;dat}$	0	--	900	ns

Data Set-up time	$t_{su;dat}$	100	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	300	ns
Fall time of SBCL, SBDA	t_f	--	--	300	ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	100	pf

6. MIPI Timing

6.1 Clock Lane Low-power

Figure 12: MIPI Clock Lane Time

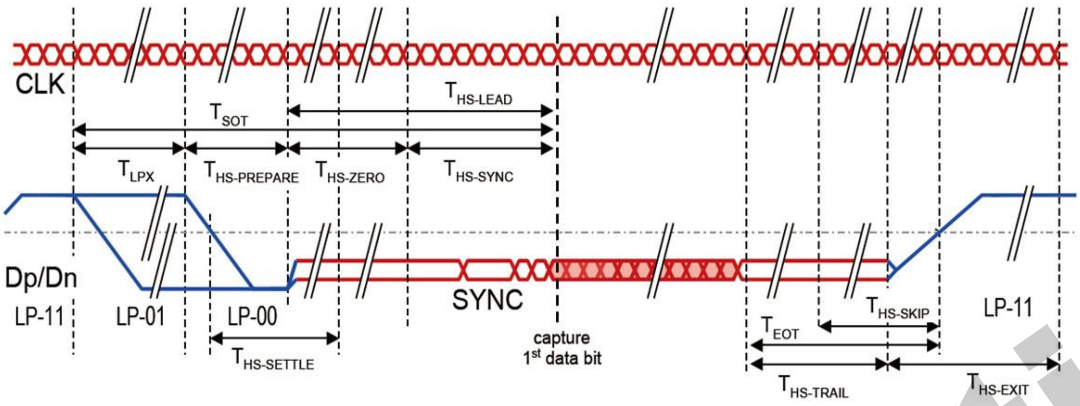


Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).
  - $T_{CLK\_HS\_PREPARE}$: setting by Register 0x0122
  - T_{CLK_ZERO}: setting by Register 0x0123
  - T_{CLK_PRE}: setting by Register 0x0124
  - T_{CLK_POST}: setting by Register 0x0125
  - T_{CLK_TRAIL}: setting by Register 0x0126

6.2 Data Burst

Figure 13: MIPI Data Lane Time



Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.
  - T_{LPX}: setting by Register 0x0121
  - $T_{HS\_PREPARE}$: setting by Register 0x0129
  - T_{HS_ZERO}: setting by Register 0x012a
  - T_{HS_TRAIL}: setting by Register 0x012b
  - T_{HS_EXIT}: setting by Register 0x0127

7. Function Description

7.1 Operation Mode

Figure 14: Operation Mode

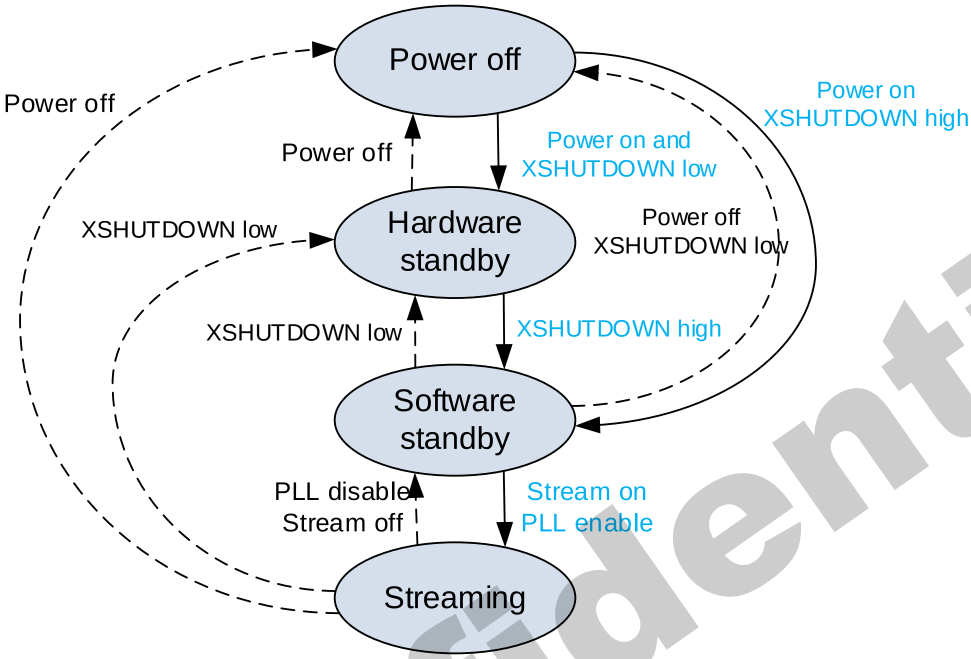


Table 12: Operate State

Power state	Description	Activate
Power off	Power supplies are turned off	None
Hardware standby	No communication with sensor, low level on XSHUTDOWN	XSHUTDOWN low
Software standby	Two- wire serial communication with sensor is possible, pll is ready for fast return to streaming mode	Stream mode off PLL disable XSHUTDOWN high
Streaming	Sensor is fully powered and streaming image data on the MIPI CSI-2 bus	All Pad Enabled

7.2 Power on Sequence

Figure 15: Power on Timing

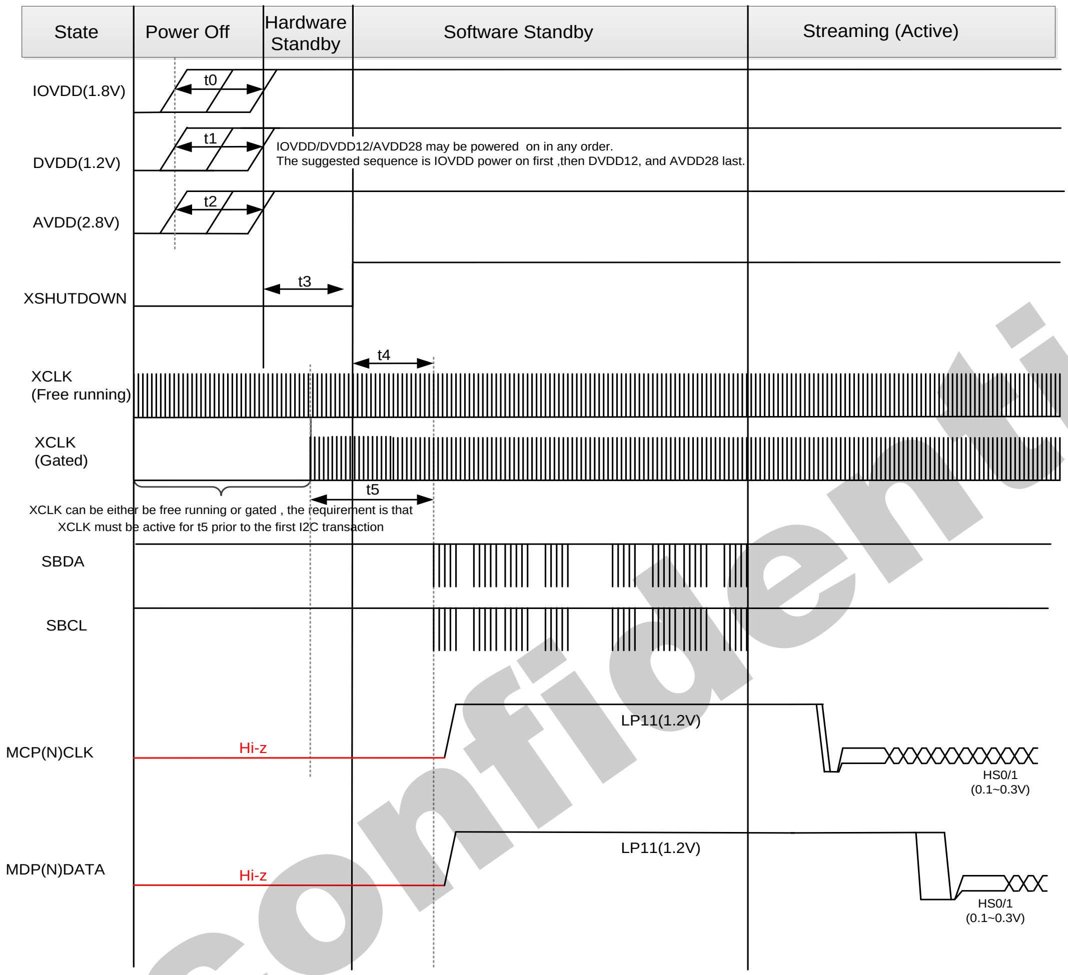


Table 13: Power on Timing

Parameter	Description	Min.	Max.	Unit
t0	IOVDD/DVDD12/AVDD28 may rise in any order. The rising separation can vary from 0μs to indefinite.	0	-	μs
t1				
t2				
t3	From power on to XSHUTDOWN pull high	0	-	μs
t4	XSHUTDOWN rising to first I2C transaction	50	-	μs
t5	Minimum No. of XCLK cycles prior to the first I2C transaction	1200	-	XCLK

Note: 1. IOVDD/DVDD12/AVDD28 may rise in any order.
2. The suggested sequence is IOVDD powered on first, then DVDD12, and AVDD28 last.
3. Register should be reloaded before works.

7.3 Power off Sequence

Figure 16: Power off Timing

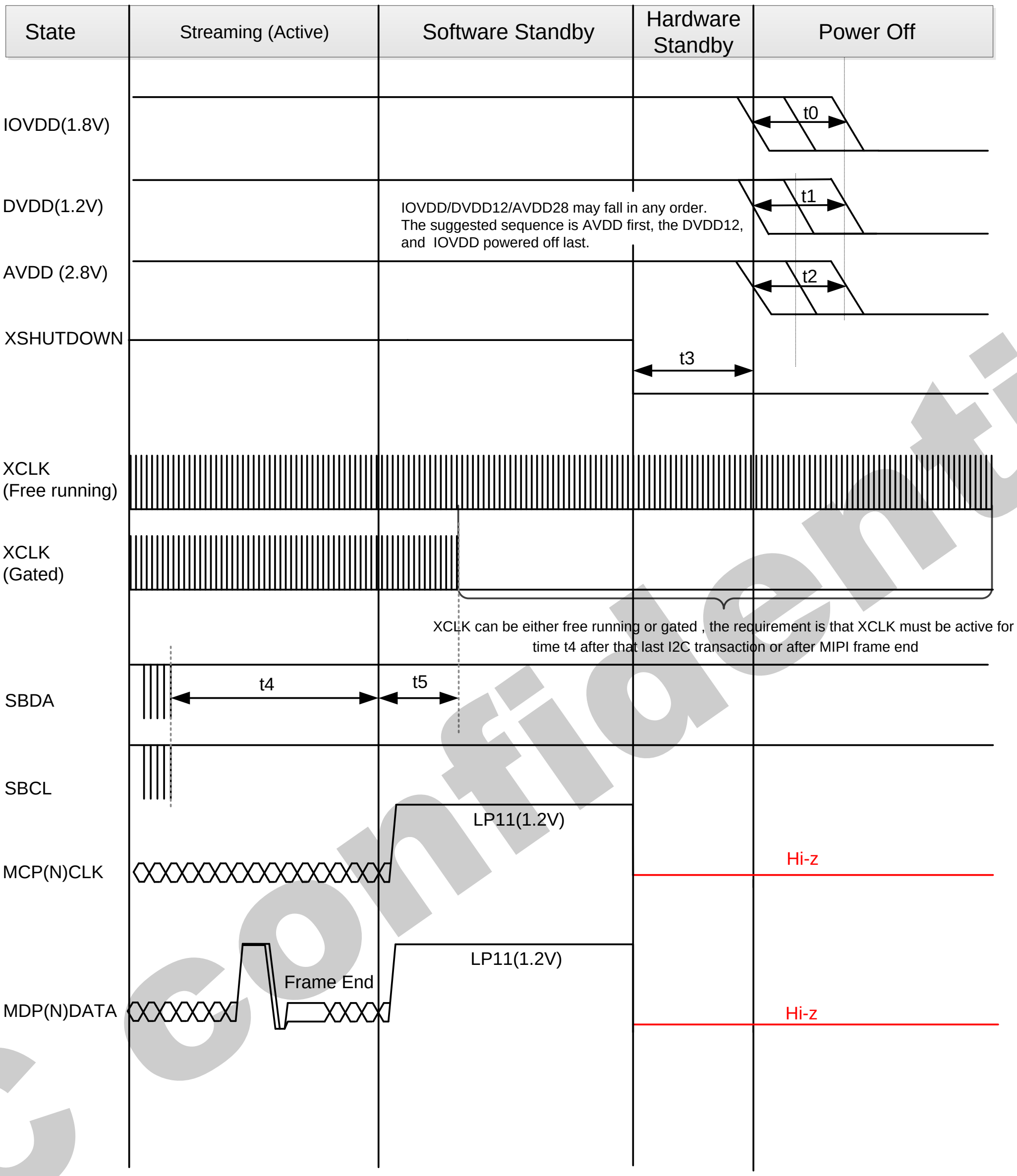


Table 14: Power off Timing

Parameter	Description	Min.	Max.	Unit
t0	IOVDD/DVDD12/AVDD28 may fall in any order. The fall separation can Vary from 0μs to indefinite.	0	-	μs
t1				
t2				
t3	From XSHUTDOWN pull down to power off	0		μs
t4	Enter Software Standby command – Device in Software Standby mode	0	-	μs
t5	Minimum number of XCLK cycles after the	2000		XCLK

	last transaction or MIPI frame end code.			

Note: 1. IOVDD/DVDD12/AVDD28 may fall in any order. The suggested sequence is AVDD first, the DVDD12, and IOVDD powered off last.
2. If the sensor’s power cannot be cut off, please keep power supply, then set XSHUTDOWN pin low. It will make sensor standby.
3. If the standby sequence needs to be modified, please contact FAE of *Galaxycore Inc*.

7.4 Black Level Calibration

Black level is caused by pixel characteristics and analog channel offset, which makes poor image quality in dark condition and color balance, to reduce these, sensor automatically calibrates the black level every frame with light shield pixel array.

7.5 Integration Time

The integration time is controlled by the shutter time registers. When you want to set an exposure value that is bigger than the current frame length value, you should first set a new frame length and make sure that it’s bigger than the exposure value you’d like to set.

Table 15: Shutter Time Register

Addr.	Register name	Description
0x0202	Shutter time	[5:0] shutter time[13:8]
0x0203		[7:0] shutter time[7:0]

7.6 Windowing

GC4033 has a rectangular pixel array 2560 x 1440, it can be windowed by output size control, the output image windowing can be used to adjust output size, and it will affect field angle.

Figure 17: Windowing Mode

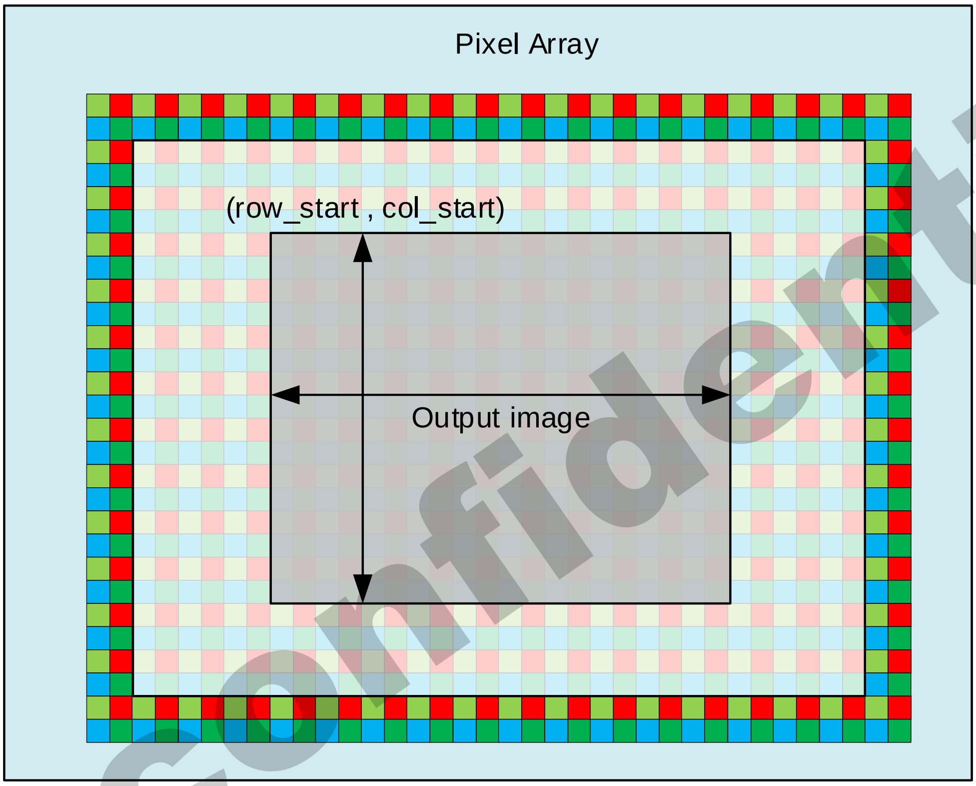


Table 16: Window Set Register

Addr.	Register name	Description
0x034a	win_height	[2:0] win_height[10:8]
0x034b		[7:0] win_height[7:0]
0x0348	win_width	[3:0] win_width[11:8]
0x0349		[7:0] win_width[7:0]
0x0346	Row start	[2:0] row_start[11:8]
0x0347		[7:0] row_start [7:0]
0x070c	Col start	[7:0] col_start [10:8]
0x070d		[7:0] col_start [7:0]

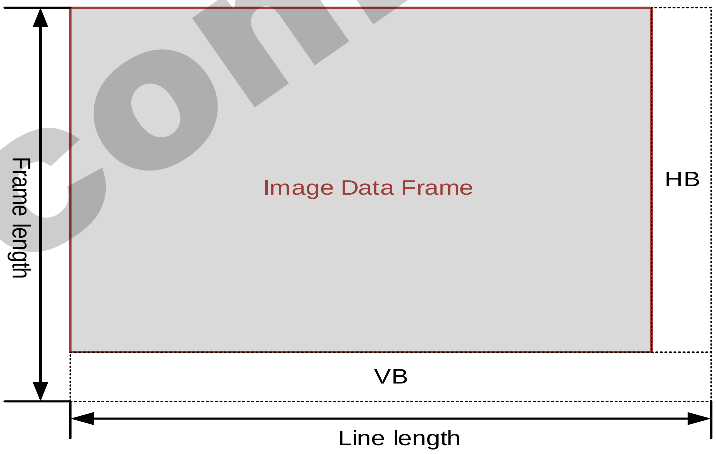
Table 17: Out Window Set Register

Addr.	Register name	Description
0x009a	out_win_x1	[3:0] out_win_x1[11:8]
0x009b		[7:0] out_win_x1[7:0]
0x0098	out_win_y1	[3:0] out_win_y1[10:8]
0x0099		[7:0] out_win_y1[7:0]
0x0094	out_win_width	[3:0] out_win_width[11:8]
0x0095		[7:0] out_win_width[7:0]
0x0096	out_win_height	[3:0] out_win_height[10:8]
0x0097		[7:0] out_win_height[7:0]

7.7 Frame Sync Mode

GC4033 can support hardware frame sync for dual camera application. It can be set both master and slave sensor. When use this mode, the two sensor's FSYNC pin must connect to each other.

Figure 18: Frame Sync Configuration



Master Mode:

When GC4033 operates as a master device, it controls vertical synchronous timings and outputs synchronous signal called Vsync signal or Fsync signal from the FSYNC pin.

Slave Mode:

GC4033 can be worked as a slave and automatically synchronized within a certain VSYNC time period. It is important to control two image sensors' rolling shutters with the same timing.

7.8 Binning Mode

GC4033 has Binning mode which support a lower resolution output with high frame rate. The row or col can be independent controlled. However, only the row binning can increase frame rate.

Table 18: Binning mode Register

Addr.	Register name	Description
0x0218	Row Binning	[4] Row Binning enable
0x0077	Col Binning	[3] Col Binning enable

7.9 Frame Structure

Frame structure is controlled by line length, frame length, window height, window width.

Frame length control:

Frame length is controlled by window height, minimum VB and shutter time.

◆ Frame length depend shutter time.

- Minimum frame length = window height + 28 +VB (VB_min = 0)
- If shutter time < minimum frame length: Actual frame length = minimum frame length
- If shutter time > minimum frame length: Actual frame length = shutter time + 8 (recommended).

Table 19: Frame Length Register

Addr.	Register name	Description
0x0340	Frame length	[7:0] frame length[13:8]
0x0341		[7:0] frame length[7:0]
0x029d	Minimum VB	[7:0] min_vb[7:0]

Line length control:

Line length control for internal set, and not recommended to be modified.

Table 20: Line Length Register

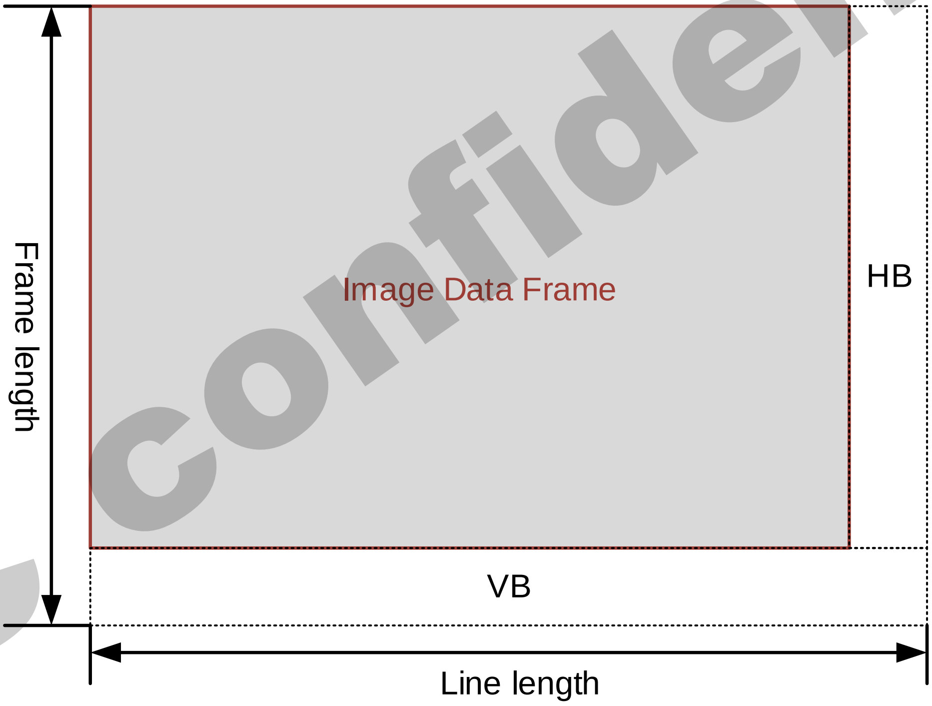
Addr.	Register name	Description
0x0343	Line length	[7:0] Line length[15:8]
0x0342		[7:0] Line length[7:0]

Blank time control:

Line blank time is controlled by line length.

Frame blank time = frame length – out window height

Figure 19: Frame Structure



8. Register List

System Register:

Address	Name	Default	R/W	Description
0x03f0	Sensor_ID_HIGH	0x40	RO	Sensor_ID
0x03f1	Sensor_ID_LOW	0x33	RO	Sensor_ID

Analog & CISCTL:

Address	Name	Default	R/W	Description
0x0202	Exposure[13:8]	0x00	RW	[5:0] Exposure[13:8]
0x0203	Exposure[7:0]	0x10	RW	[7:0] Exposure[7:0]
0x0342	CISCTL_hb[15:8]	0x02	RW	[5:0] CISCTL_hb[15:8]
0x0343	CISCTL_hb[7:0]	0x03	RW	[7:0] CISCTL_hb[7:0]
0x0346	CISCTL_row_start[10:8]	0x00	RW	[2:0] CISCTL_row_start[10:8]
0x0347	CISCTL_row_start[7:0]	0x02	RW	[7:0] CISCTL_row_start[7:0]
0x070c	CISCTL_col_start [10:8]	0x00	RW	[2:0] CISCTL_col_start [10:8]
0x070d	CISCTL_col_start [7:0]	0x00	RW	[7:0] CISCTL_col_start [7:0]
0x034a	CISCTL_win_height[10:8]	0x05	RW	[2:0] CISCTL_win_height[10:8]
0x034b	CISCTL_win_height[7:0]	0x18	RW	[7:0] CISCTL_win_height[7:0]
0x0348	CISCTL_win_width[11:8]	0x09	RW	[3:0] CISCTL_win_width[11:8]
0x0349	CISCTL_win_width[7:0]	0x0c	RW	[7:0] CISCTL_win_width[7:0]
0x0340	Framelength[13:8]	0x06	RW	[5:0] Framelength_high[13:8]
0x0341	Framelength[7:0]	0x42	RW	[7:0] Framelength_low[7:0]
0x029d	min_vb[7:0]	0x10	RW	
0x0213	CISCTL_vs_st	0x18	RW	vs_st
0x0214	CISCTL_vs_et	0x04	RW	vs_et

CSI/PHY1.0

Address	Name	Default	R/W	Description
0x0100	Lane_Ena ULP_Ena Line_sync_mode MIPI_Ena	0x20	RW	[3] Lane_Ena [2] ULP_Ena [1] Line_sync_mode [0] MIPI_Ena
0x0180	DPHY_analog_mode1	0x06	RW	[6] mipi_en [5:4] disable_set [3:0] mipi_diff

0x0181	DPHY_analog_mode2	0x00	RW	[3] dphy_data1_en [2] dphy_data0_en [1] data1delay1s [0] data0delay1s
0x0182	DPHY_analog_mode3	0x00	RW	[3:2] data1lp_drv_10 [1:0] data0lp_drv_10
0x0183	DPHY_analog_mode4	0x05	RW	[3:2] data1ctr [1:0] data0ctr
0x0184	DPHY_analog_mode5	0x05	RW	[3:2] dat1hs_ph [1:0] dat0hs_ph
0x0185	DPHY_analog_mode6	0x00	RW	[0] dphy_clk_en
0x0186	DPHY_analog_mode7	0x53	RW	[7:6] clkctr [5:4] clkhs_ph [3:2] clklp_drv_10 [1] clklane_p2s_sel NA clkp2s_en [0] clkdelay1s
0x0187	DPHY_analog_mode8	0x00	RW	[2] data1lane_clkf_test [1] data0lane_clkf_test [0] clklane_clkf_test
0x0111	LDI_set	0x2b	RW	[7:0] LDI_set [7:6] vc_id [5:4] data type raw10/8
0x010d	LWC_set[15:8]	0x0b	RW	[7:0] LWC_set_1
0x010e	LWC_set[7:0]	0x40	RW	[7:0] LWC_set_2
0x010f	SYNC_set	0xb8	RW	[7:0] SYNC_set
0x0115	DPHY_mode	0x10	RW	[6] mipi para invar when div2 [5] DATA lane gate [4] all_lane_open_mode [3:2] switch_msb_mode [1:0] clklane_mode
0x0116	LP_set	0x29	RW	[7:6] hi-z [5:4] use define
0x0120	T_init_set	0x80	RW	[7:0] T_init_set
0x0121	T_LPX_set	0x10	RW	[7:0] T_LPX_set
0x0122	T_CLK_HS_PREPARE_set	0x05	RW	[7:0] T_CLK_HS_PREPARE_set
0x0123	T_CLK_zero_set	0x20	RW	[7:0] T_CLK_zero_set
0x0124	T_CLK_PRE_set	0x02	RW	[7:0] T_CLK_PRE_set
0x0125	T_CLK_POST_set	0x20	RW	[7:0] T_CLK_POST_set
0x0126	T_CLK_TRAIL_set	0x08	RW	[7:0] T_CLK_TRAIL_set
0x0127	T_HS_exit_set	0x10	RW	[7:0] T_HS_exit_set
0x0128	T_wakeup_set	0xa0	RW	[7:0] T_wakeup_set

0x0129	T_HS_PREPARE_set	0x06	RW	[7:0] T_HS_PREPARE_set
0x012a	T_HS_Zero_set	0x0a	RW	[7:0] T_HS_Zero_set
0x012b	T_HS_TRAIL_set	0x08	RW	[7:0] T_HS_TRAIL_set

OUT

Address	Name	Default	R/W	Description
0x008c	Test image	0x10	RW	[2] input test image
0x0098	out_win_y1[10:8]	0x00	RW	[7:3]NA [2:0] out_win_y1
0x0099	out_win_y1[7:0]	0x00	RW	Out_win_y1
0x009a	out_win_x1[11:8]	0x00	RW	[7:4]NA [3:0]out_win_x1
0x009b	Out_win_x1[7:0]	0x00	RW	out_win_x1
0x0096	Out_win_height[11:8]	0x06	RW	[7:3]NA [3:0] out_win_helght[11:8]
0x0097	Out_win_height[7:0]	0x82	RW	out_win_helght[7:0]
0x0094	Out_win_width[11:8]	0x0b	RW	[7:4]NA [3:0]out_win_width[11:8]
0x0095	Out_win_width[7:0]	0x90	RW	Out_win_width[7:0] must be 8X when raw10
0x009c	Win_mode[2:0]	0x01	RW	[2]hsync_dummy_en [1]amba_mode_en [0]crop_en
0x008e	Out_win_offset	0x05	RW	[7:6]out_offset_y1_bin=1 [5:4]out_offset_y1=2; for auto_mirror [3:2]out_offset_x1_bin=1 [1:0]out_offset_x1=2

OB OFFSET

Address	Name	Default	R/W	Description
0x0038	WB_offset_G1	0x40	RW	WB_offset
0x0039	WB_offset_R1	0x40	RW	WB_offset
0x003a	WB_offset_B1	0x40	RW	WB_offset
0x003b	WB_offset_G2	0x40	RW	WB_offset

Gain

Address	Name	Default	R/W	Description
0x0064	auto_pregain[9:6]	0x01	RW	[3:0] Auto_pregain[9:6]
0x0065	auto_pregain[5:0]	0x00	RW	[7:2] Auto_pregain[5:0]

0x02aa	Analog_PGA_gain[11:8]	0x00	RW	[3:0] analog_gain[11:8]
0x02ab	Analog_PGA_gain[7:0]	0x00	RW	[7:0] Analog_gain[7:0]
0x00a8	Col_gain[13:6]	0x01	RW	[5:0]col_gain[13:6]
0x00a9	Col_gain[5:0]	0x00	RW	[5:0]col_gain[5:0]