GC2607 CSP

1/7.3” FHD CMOS Image Sensor

Datasheet

V0.1

2022-01-20

Ordering Information

◆ **GC2607**

(Color, 150um, back grinding, reconstructed wafer)

GENERATION REVISION HISTORY

REV.	*EFFECTIVEDATE*	*DESCRIPTION OFCHANGES*	*PREPARED BY*
V0.1	*2022-01-20*	*Beta Version*	*AE Dept.*

Galaxycore Incorporation

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Content

1. Sensor Overview

1.1 General Description

GC2607 is a high quality 1080P CMOS image sensor, for security camera products, digital camera products and mobile phone camera applications. GC2607 incorporates a 1920H x 1080V pixel array, on-chip 10-bit ADC, and image signal processor.

The full-scale integration of high-performance and low-power functions makes the GC2607 best fit the design, reduce implementation process, and extend the battery life of Motion Camera, PC cameras, Car DVR, and a wide variety of mobile applications.

It provides RAW10 data formats with MIPI interface. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Standard optical format of 1/7.3 inch
- 1.12μmx1.12μm BSI
- Output formats: Raw Bayer 10bit
- Power supply requirement: AVDD28: 2.7~2.9V(Typ.2.8V)
  DVDD18: 1.1~1.3V(Typ.1.2V)
  IOVDD: 1.7~1.9V(Typ.1.8V)
- PLL support
- Support frame sync
- MIPI (2 lane) interface support
- Horizontal/Vertical mirror
- Image processing module

- OTP support: Module information
- Package: COB/CSP
- HDR Mode

1.3 Application

- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipment

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/7.3inch
Pixel Size	1.12μm×1.12μm
Active pixel array	1920×1080
Shutter type	Electronic rolling shutter
ADC resolution	10 bits ADC
Max Frame rate	60fps@full size 30fps@HDR Mode
Power Supply	AVDD28: 2.8V DVDD: 1.2V IOVDD: 1.8V
Power Consumption	76.474 mW
MAX SNR	TBD
Dark Current	TBD
Sensitivity	TBD
Dynamic range	TBD
Operating temperature:	-30~85℃
Stable Image temperature	0~60℃
Storage temperature	-40~125℃
Optimal lens chief ray angle (CRA)	33.658° (non-linear)
Package type	COB/CSP
Input clock frequency	6~27MHz

2. DC Parameters

2.1 Standby Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	77.7	—	uA
Digital	I_{DVDD}	—	41.9	—	uA
I/O	I_{IOVDD}	—	13.5	—	uA

RST: L, PWND: L
Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

2.2 Power off Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	0	0	uA
Digital	I_{DVDD}	—	0	0	uA
I/O	I_{IOVDD}	—	0	0	uA

Power off, T_j=25℃

2.3 Operation current

Full size (MIPI 2 Lane)

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	17.53	—	mA
Digital	I_{DVDD}	—	18.1	—	mA
I/O	I_{IOVDD}	—	3.15	—	mA

Input clock: 27MHz, Frame rate: 30FPS, RAW 10,

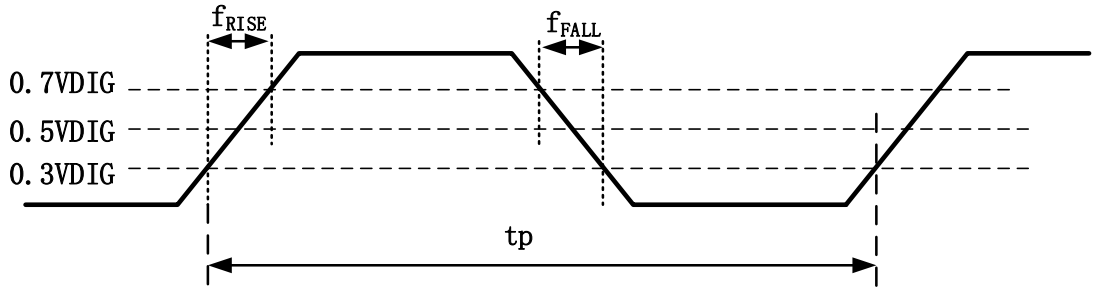
Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

2.4 DC Characteristics

Item	Symbol	Min	Typ	Max	Unit
Power supply	V_{AVDD}	2.7	2.8	2.9	V
	V_{DVDD}	1.1	1.2	1.3	V
	V_{IOVDD}	1.7	1.8	1.9	V
Digital Input(Conditions: AVDD = 2.8V, DVDD =1.2V, IOVDD = 1.8V)					
Input voltage HIGH	V_{IH}	0.7*VIF			V
Input voltage LOW	V_{IL}			0.3*VIF	V
Digital Output(Conditions: AVDD =2.8V, IOVDD = 1.8V, standard Loading 25PF)					
Output voltage HIGH	V_{OH}	0.8*VIF			V
Output voltage LOW	V_{OL}			0.2*VIF	V

3. AC Characteristics

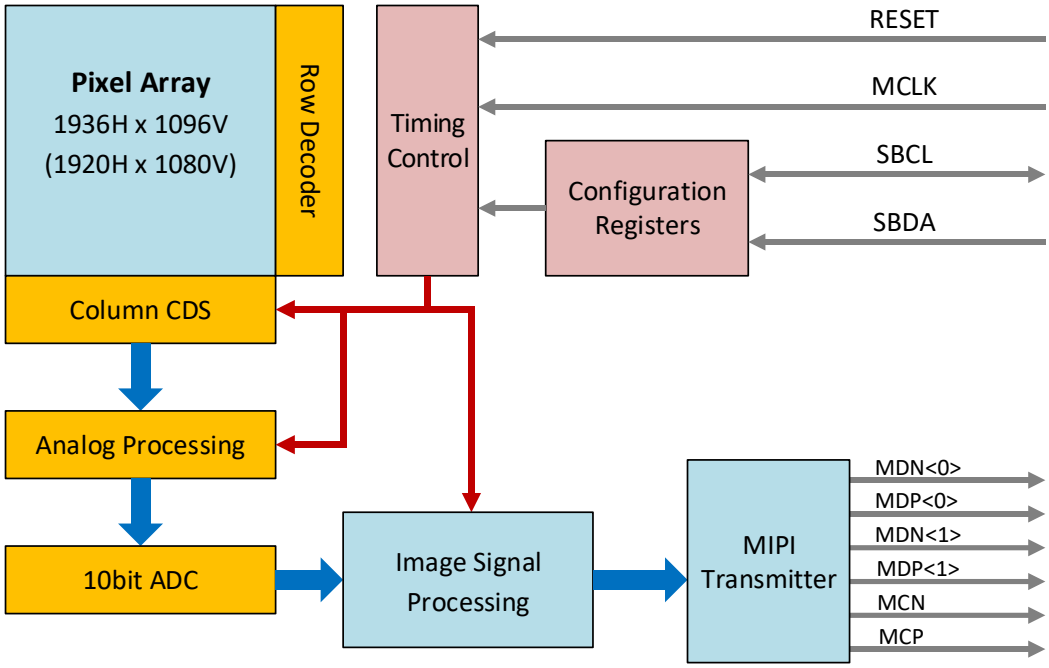
Master clock wave diagram



Input clock square waveform specifications：

Item	Symbol	Min	Typ	Max	unit
Frequency	f_{SCK}	6	24	27	MHz
jitter (period,	T_{jitter}			600	ps
Rise Time	f_{RISE}	1		15	ns
Fall Time	f_{FALL}	1		15	ns
Duty Cycle	f_{DUTY}	40		60	%
Input Leakage	f_{ILEAK}	-10		10	μA

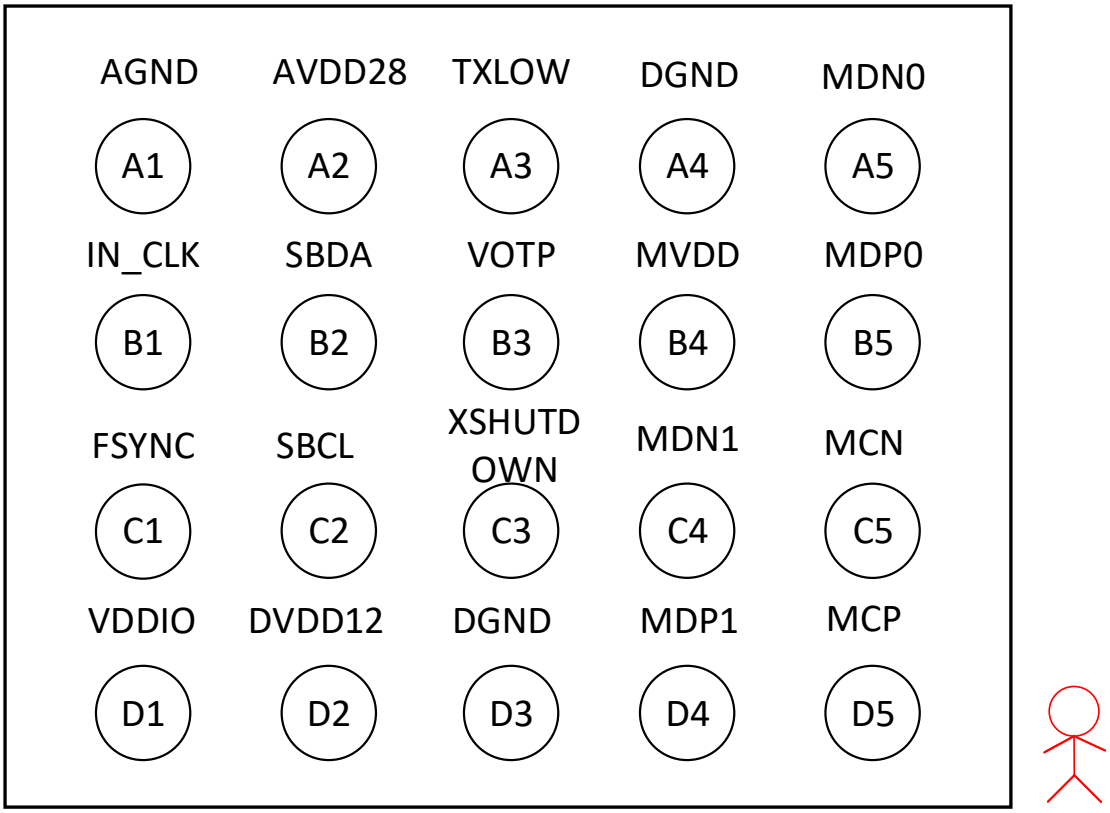
4. Block Diagram



GC2607 has an active image array of 1920x1080 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 10 bits A/D converter. The digital signals are processed in the ISP Block. Users can easily control these functions via two-wire serial interface bus.

5. CSP Package Specifications

5.1 Pin Diagram (CSP)



CSP (Top View)

5.2 Pin Descriptions

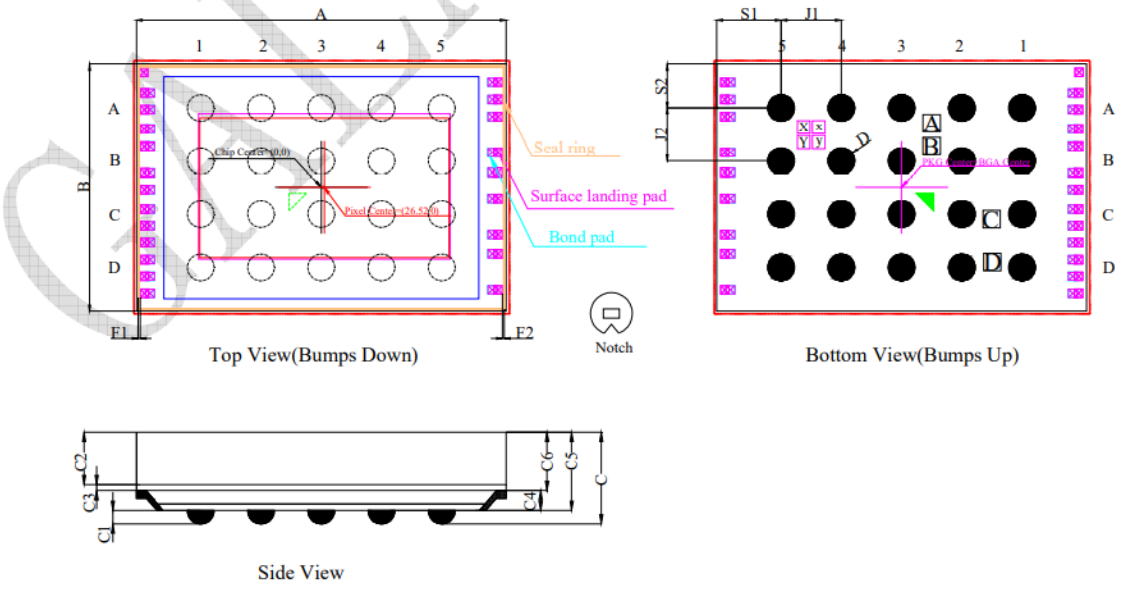
Pin	Name	Pin Type	Description
A1	AGND	Ground	Ground for Analog.
A2	AVDD28	Power	Analog Power: 2.8V
A3	TXLOW	Power	Internal power supply
A4	DGND	Ground	Ground for Digital
A5	MDN0	Output	MIPI data <0> (-)
B1	IN_CLK	Input	Sensor input clock
B2	SBDA	Input	Two-wire serial bus, data.
B3	VOTP	Power	For OTP power supply, external supply of 7V high voltage
B4	MVDD	Power	MIPI Power: 1.1~1.3V
B5	MDP0	Output	MIPI data <0> (+)
C1	FSYNC	I/O	Frame sync control

C2	SBCL	Input	Two-wire serial bus, clock.
C3	XSHUTDOWN	Input	Sensor power down control: (floating forbidden) 0：standby 1：normal work
C4	MDN1	Output	MIPI data <1> (-)
C5	MCN	Output	MIPI clock (-)
D1	VDDIO	Power	I/O Power：1.7~1.9V
D2	DVDD12	Power	DIGITAL Power：1.1~1.3V
D3	DGND	Ground	Ground for Digital.
D4	MDP1	Output	MIPI data <1> (+)
D5	MCP	Output	MIPI clock (+)

5.3 Package Specification

Figure1: Package Mechanical Draw

Mechanical Drawing



Package size table

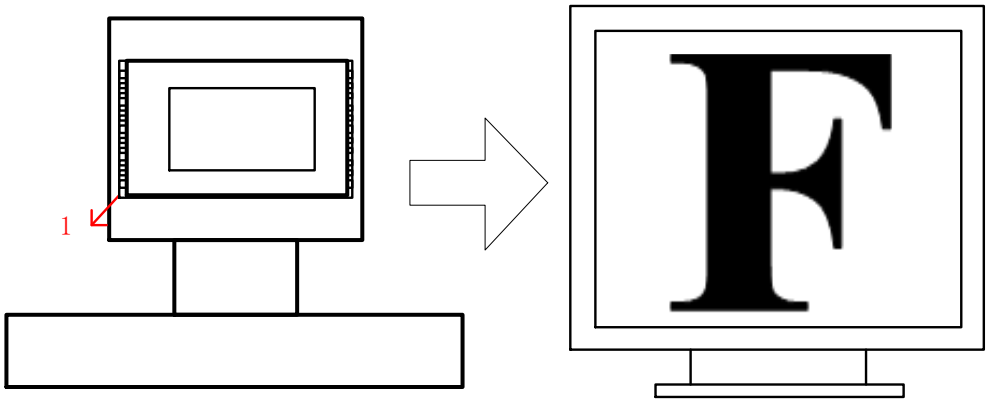
Description	Symbol	Nominal	Min.	Max.
		Millimeters		
Package Body Dimension X	A	3.190	3.165	3.215
Package Body Dimension Y	B	2.130	2.105	2.155

Package Height	C	0.660	0.605	0.715
Ball High	C1	0.130	0.100	0.160
Glass Thickness	C2	0.300	0.290	0.305
CV Thickness	C3	0.041	0.037	0.045
Silicon Thickness	C4	0.150	0.143	0.157
Package Body Thickness	C5	0.530	0.495	0.565
Thickness from top glass surface to wafer	C6	0.345	0.325	0.365
Ball Diameter	D	0.230	0.200	0.260
Total Ball Count	N	20		
Ball Count X axis	N1	5		
Ball Count Y axis	N2	4		
Pins pitch X axis	J1	0.520		
Pins pitch Y axis	J2	0.460		
BGA ball center to package center offset in X-direction	X	0.0000	-0.0250	0.0250
BGA ball center to package center offset in Y-direction	Y	0.0000	-0.0250	0.0250
BGA ball center to chip center offset in X-direction	X1	0.0000	-0.0250	0.0250
BGA ball center to chip center offset in Y-direction	Y1	0.0000	-0.0250	0.0250
Edge to Pin Center Distance along X	S1	0.555	0.525	0.585
Edge to Pin Center Distance along Y	S2	0.375	0.345	0.405

6. Optical Specifications

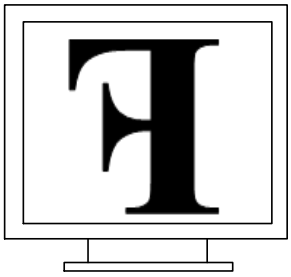
6.1 Readout Position

The GC2607 default status is readout from the lower left corner with pin A1 located in the upper left corner. The image is inverted vertically and horizontally by the lens, so proper image output results when Pin A1 is located in the upper left corner.

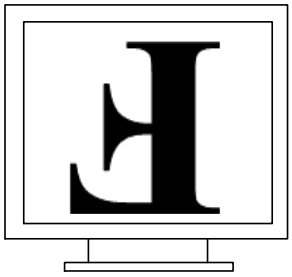


Readout direction can be set by the registers.

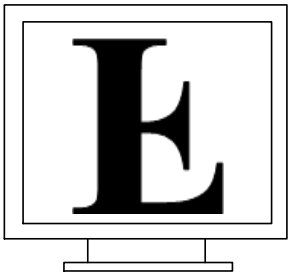
Function	Register Address	Register Value	First Pixel
Normal	0x0101[1:0]	00	Gr
Horizontal mirror	0x0101 [1:0]	01	R
Vertical Flip	0x0101[1:0]	10	B
Horizontal Mirror and Vertical Flip	0x0101 [1:0]	11	Gb



Horizontal Mirror

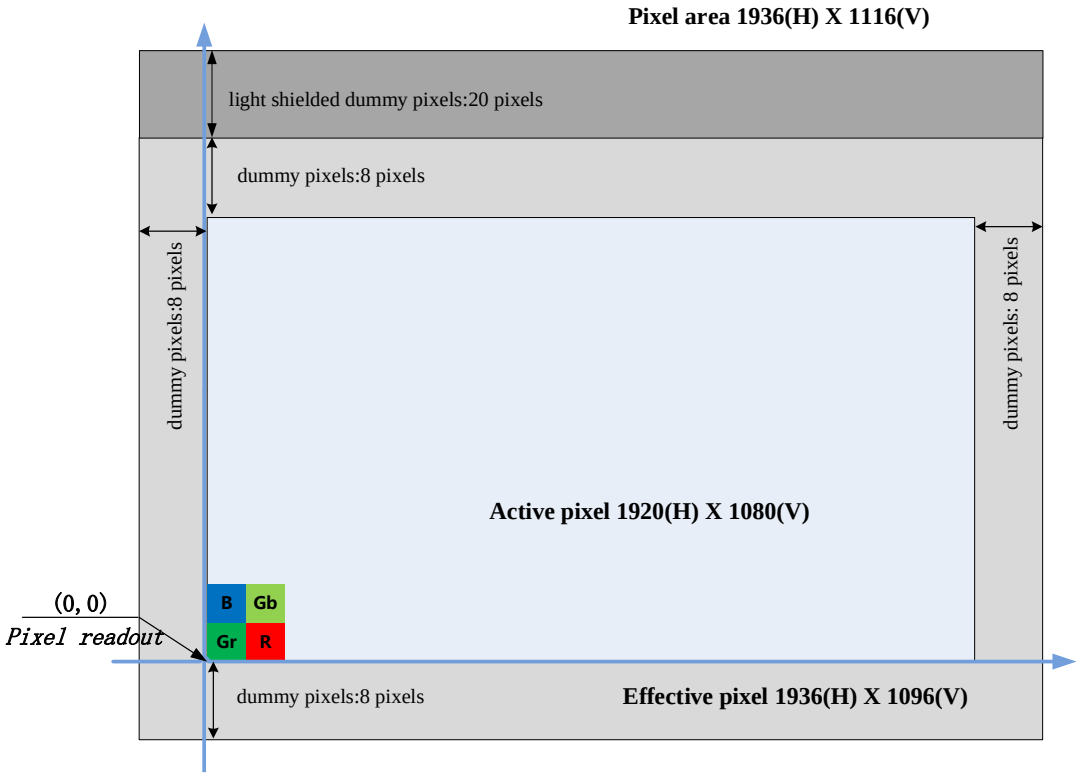


Horizontal Mirror and Vertical Flip



Vertical Flip

6.2 Pixel Array



Pixel array is covered by Bayer pattern color filters. The primary color GR/BG array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 1919. If flip in column, column is read out from 1919 to 0.

If no flip in row, row is read out from 0 to 1079.If flip in row, row is read out from 1079 to 0.

6.3 Lens Chief Ray Angle (CRA)

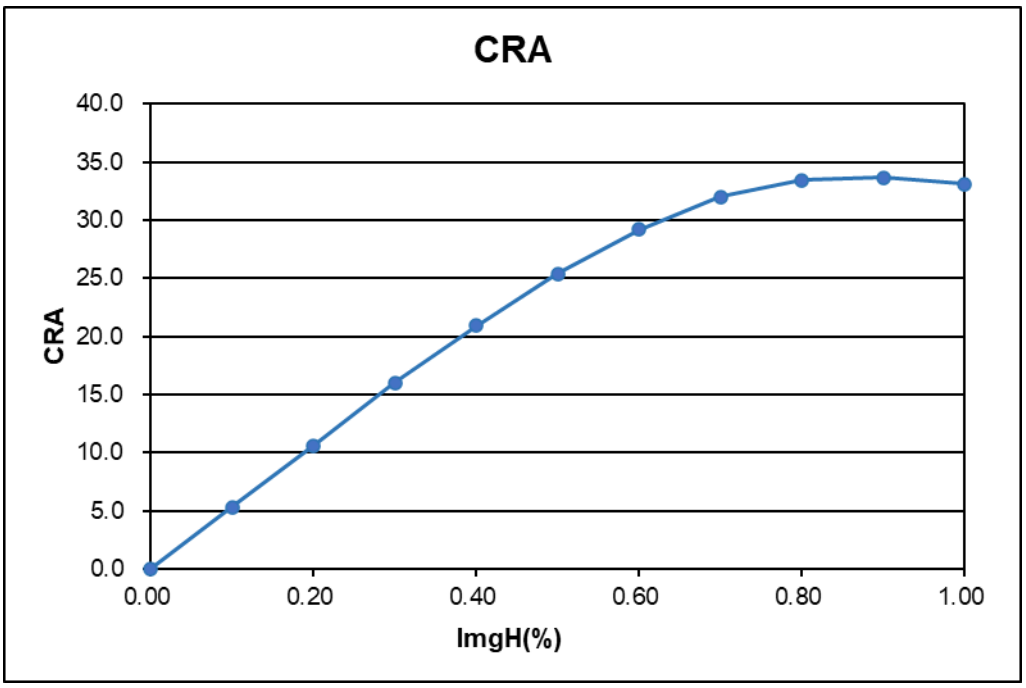


Image Height (%)	Image Height (mm)	CRA
00	0.000	0.000
10	0.123	5.327
20	0.247	10.621
30	0.370	15.988
40	0.493	20.910
50	0.617	25.368
60	0.740	29.198
70	0.864	32.015
80	0.987	33.420
90	1.110	33.658
100	1.234	33.115

7. Two-wire Serial Bus Communication

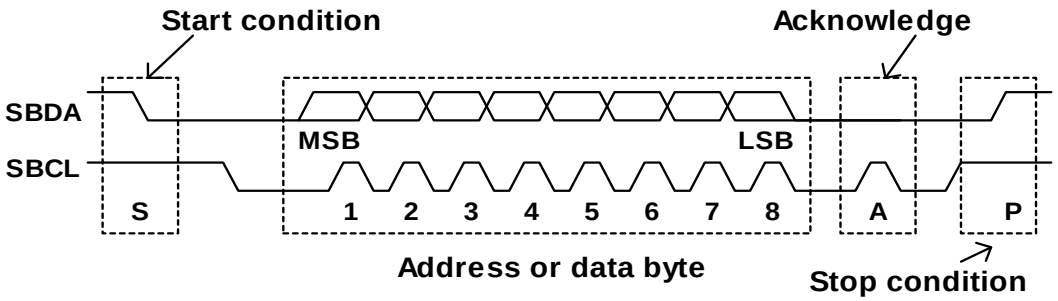
GC2607 Device Address:

ID_SEL	Slave address write mode	Slave address read mode
default	**0x6e**	**0x6f**

7.1 Protocol

The host must perform the role of a communications master and GC2607 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**.



Single Register Writing:

S	6eH	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	6eH	A	Register Address	A	Data(1)	A	……	Data(N)	A	P

Single Register Reading:

S	6eH	A	Register Address	A	S	6fH	A	Data	NA	P

Notes:

From master to slave

From slave to master

S: Start condition

P: Stop condition

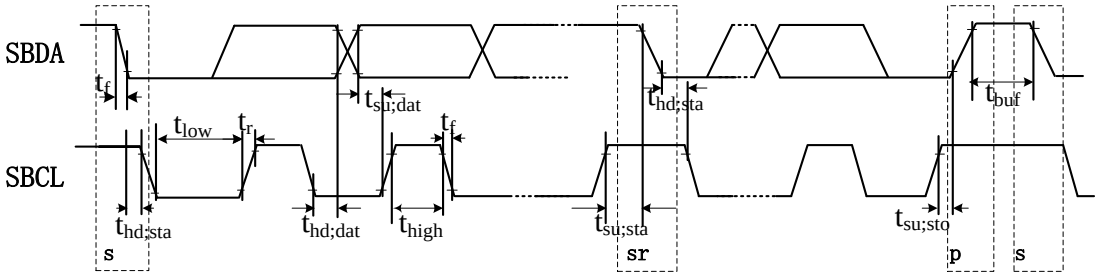
A: Acknowledge bit

NA: No acknowledge

Register Address: Sensor register address

Data: Sensor register value

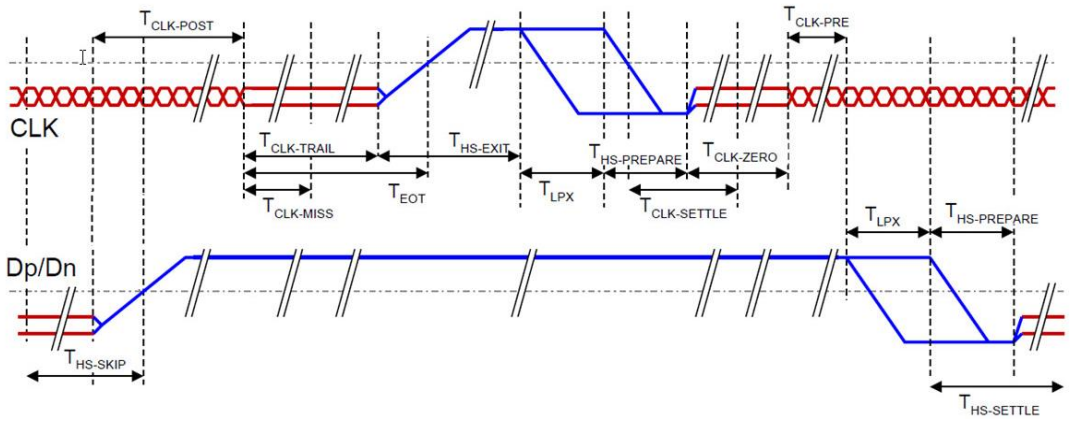
7.2 Serial Bus Timing



Parameter	Symbol	Min.	Typ.	Max.	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between stop and start condition	t_{buf}	1.3	--	--	μs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for a repeated start	$t_{su;sta}$	0.6	--	--	μs
Data hold time	$t_{hd;dat}$	0	--	0.9	μs
Data Set-up time	$t_{su;dat}$	100	--	--	Ns
Rise time of SBCL, SBDA	t_r	--	--	300	Ns
Fall time of SBCL, SBDA	t_f	--	--	300	Ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	--	Pf

8. Applications

8.1 Clock lane low-power



Notice:

- Clock must be reliable during high-speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high-speed clock).

$T_{CLK\_HS\_PREPARE}$: setting by Register 0x0db4

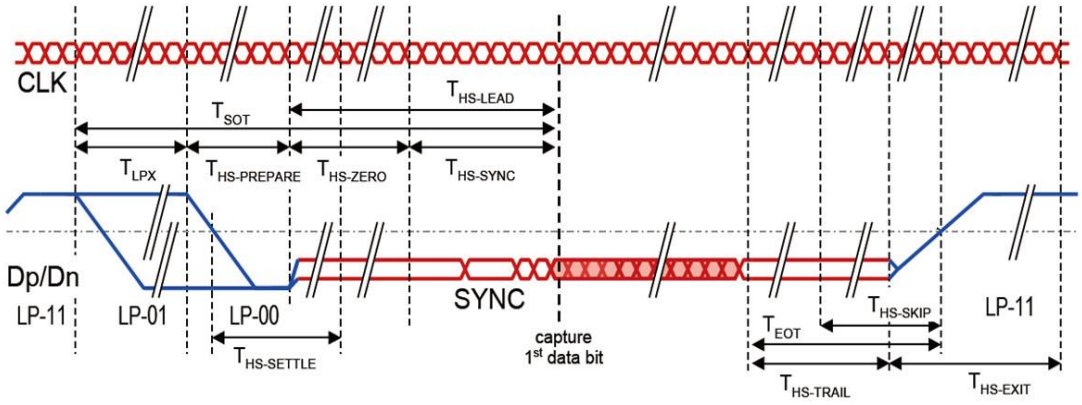
T_{CLK_ZERO}: setting by Register 0x0db5

T_{CLK_PRE}: setting by Register 0x0db6

T_{CLK_POST}: setting by Register 0x0db8

T_{CLK_TRAIL}: setting by Register 0x0db9

8.2 Data Burst



Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

T_{LPX}: setting by Register 0x0d93

$T_{HS\_PREPARE}$: setting by Register 0x0d94

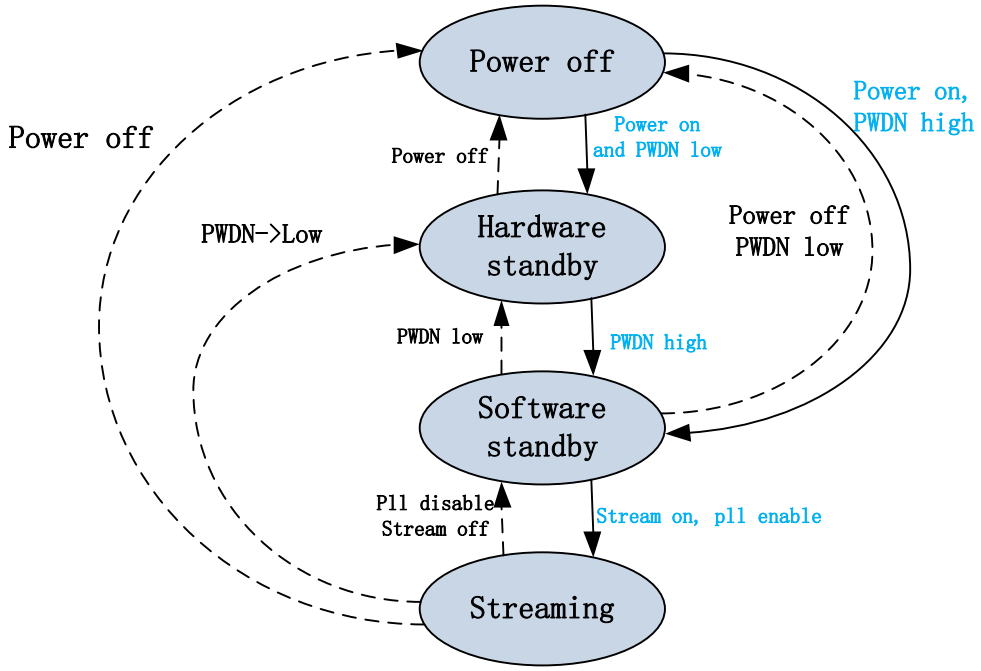
T_{HS_ZERO}: setting by Register 0x0d95

T_{HS_TRAIL}: setting by Register 0x0d99

T_{HS_EXIT}: setting by Register 0x0d9b

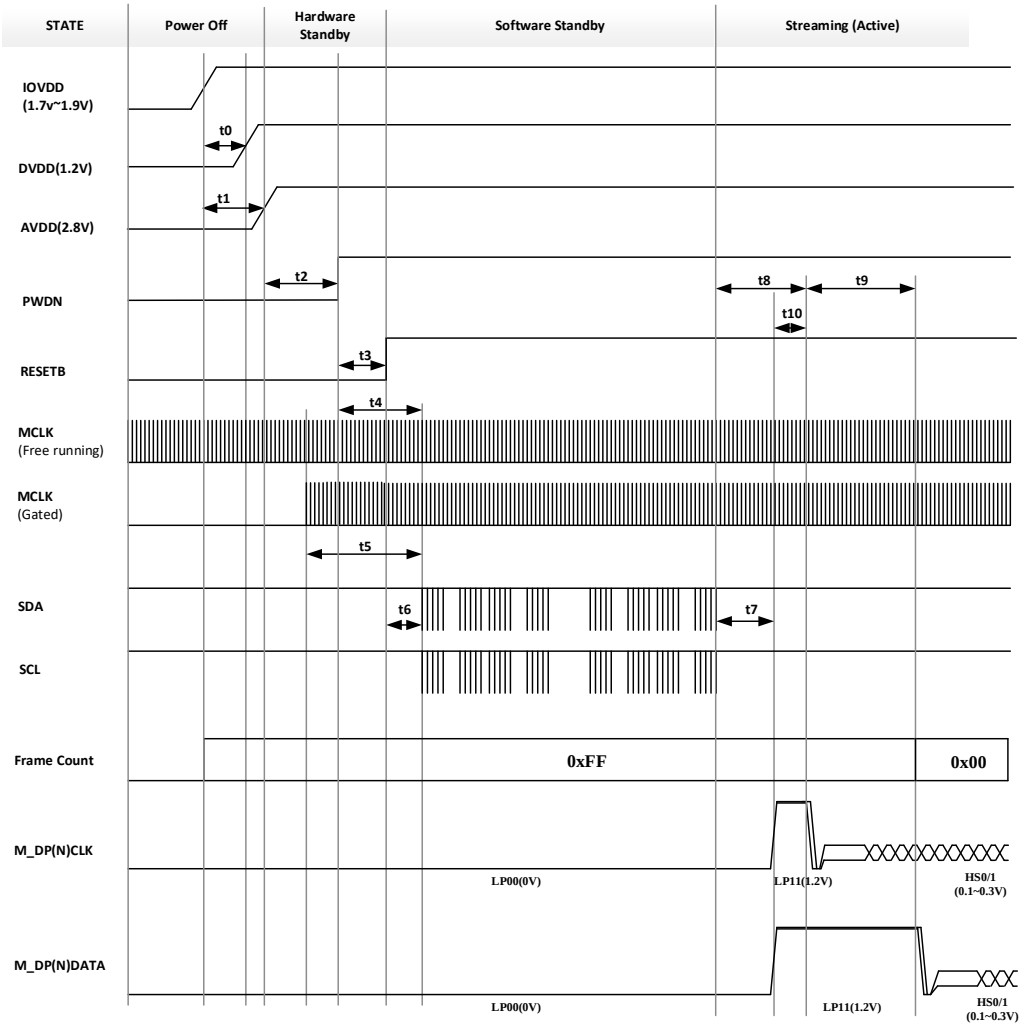
9. Function description

9.1 Operation mode



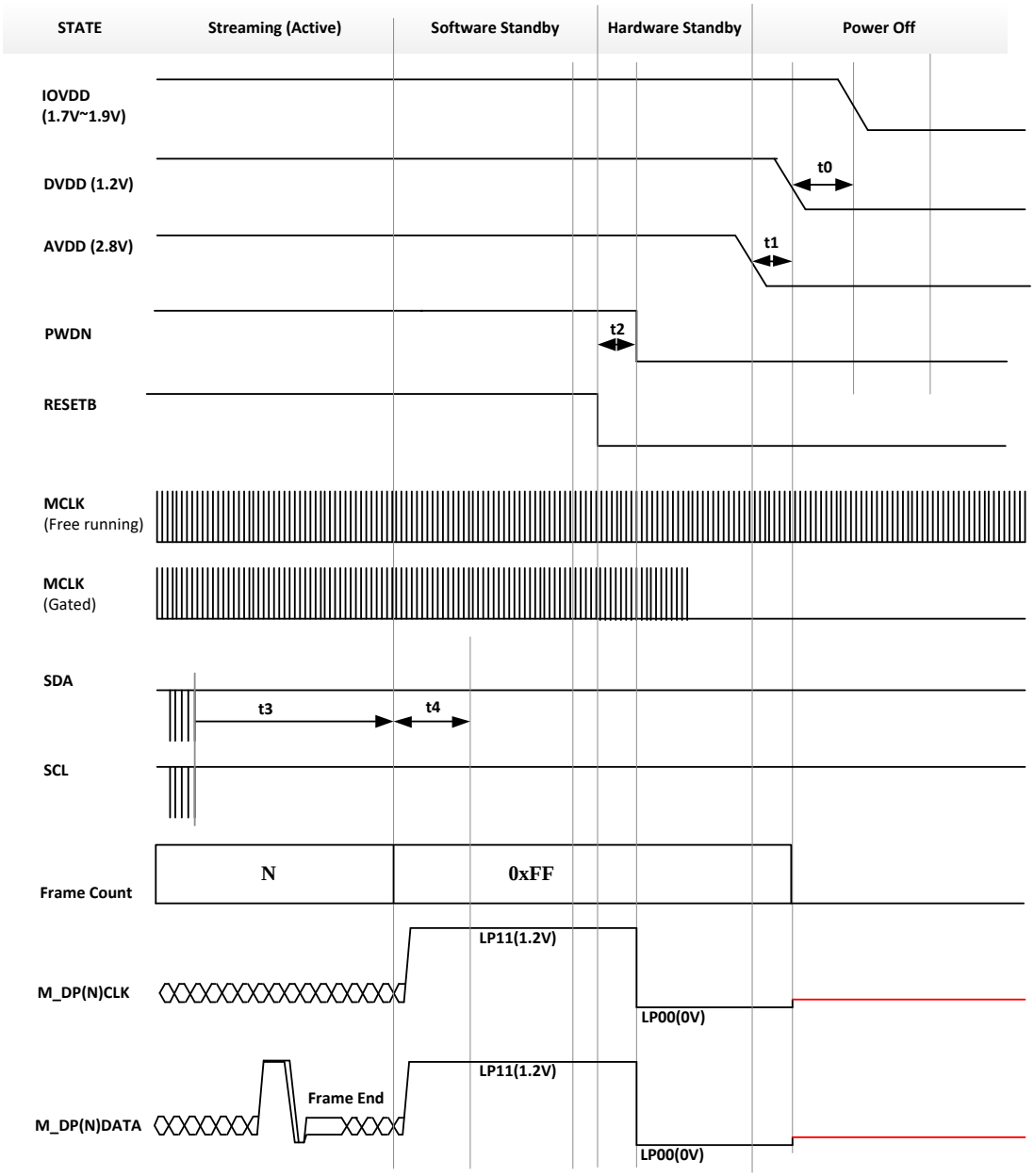
Power state	Description	Activate
Power off	Power supplies are turned off	None
Hardware standby	No communication with sensor, low level on PWDN and RESETB, and stop MCLK	PWDN low
Software standby	Two- wire serial communication with sensor, pll is ready for fast return to streaming mode	Stream mode off PLL disable RESETB high PWDN high
Streaming	Sensor is fully powered and is streaming image data on the MIPI CSI-2 bus	All

9.2 Power on Sequence



Parameter	Description	Min.	Max.	Unit
t0	From IOVDD to DVDD12	TBD	-	μs
t1	From IOVDD to AVDD28	TBD	-	μs
t2	From AVDD28 to PWDN pull high	TBD	-	μs
t3	From PWDN pull high to RESETB pull high	TBD	-	μs
t4	PWDN rising to first I2C transaction	TBD	-	μs
t5	Minimum No. of MCLK cycles prior to the first I2C transaction	TBD	-	MCLK
t6	From RESETB rising to first I2C transaction	TBD	-	μs
t7	PLL start up/lock time	-	TBD	ms
t8	Entering streaming mode – First frame start sequence (fixed part)		TBD	ms
t9	Entering streaming mode – First frame start sequence (variable part)	-		lines
t10	DPHY initialization period (TINIT)	TBD	-	ms

9.3 Power off Sequence



Parameter	Description	Min.	Max.	Unit
t0	From DVDD12 pull down to IOVDD pull down	0	-	μs
t1	From AVDD28 pull down to DVDD12 pull down	0	-	μs
t2	From RESETB pull low to PWDN pull low	0	-	μs
t3	Enter Software Standby CCI command – Device in Software Standby mode	0	-	μs
t4	Minimum number of MCLK cycles after the last CCI transaction or MIPI frame end code.	2000		MCLK

- If the sensor's power cannot be cut off, please keep power supply, then set PWDN pin low. It will make sensor standby

- Register should be reloaded before works.
- If the standby sequence needs to be modified, please contact FAE of *Galaxycore Inc.*

9.4 Black level calibration

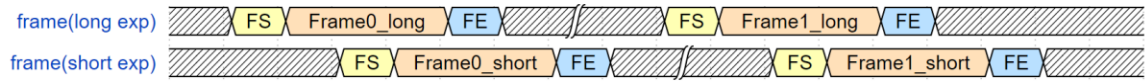
Black level is caused by pixel characteristics and analog channel offset, which makes poor image quality in dark condition and color balance, to reduce these, sensor automatically calibrates the black level every frame with light shield pixel array.

9.5 HDR mode

GC2607 has HDR function. If the function is enabled, by setting 2 different exposure times (always called long and short exposure), user can get 2 frame data in staggered output mode, and can combine two frames into one picture to improve dynamic range and avoid smearing.

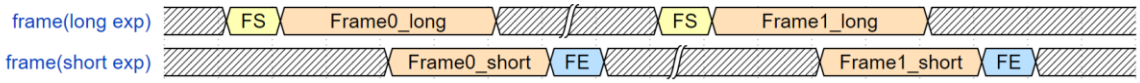
When user choose MIPI protocol as output format, different exposure time line can be distinguished by virtual channel according to MIPI protocol. By default, long exposure line' ID is 00, and short exposure line's ID is 01.

The MIPI output timing as following (virtual channel mode):



Additionally, User can distinguish different exposure time line without virtual channel. In this mode, Short exposure time line has fixed offset lines with Long exposure time line.

The MIPI output timing as following (no virtual channel mode):



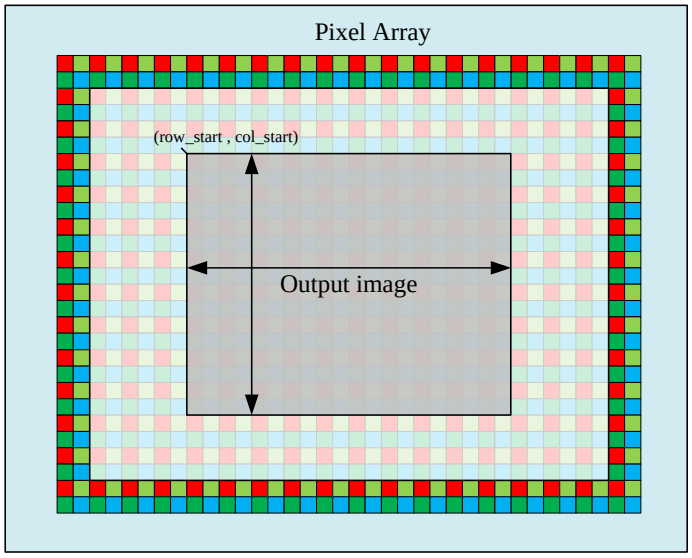
9.6 Integration time

The integration time is controlled by the integration time registers

Addr.	Register name	Description
0x0202	Shutter time	[5:0] shutter time [13:8]
0x0203		[7:0] shutter time [7:0]
0x0340	Frame length	[5:0] frame length [13:8]
0x0341		[7:0] frame length [7:0]

9.7 Windowing

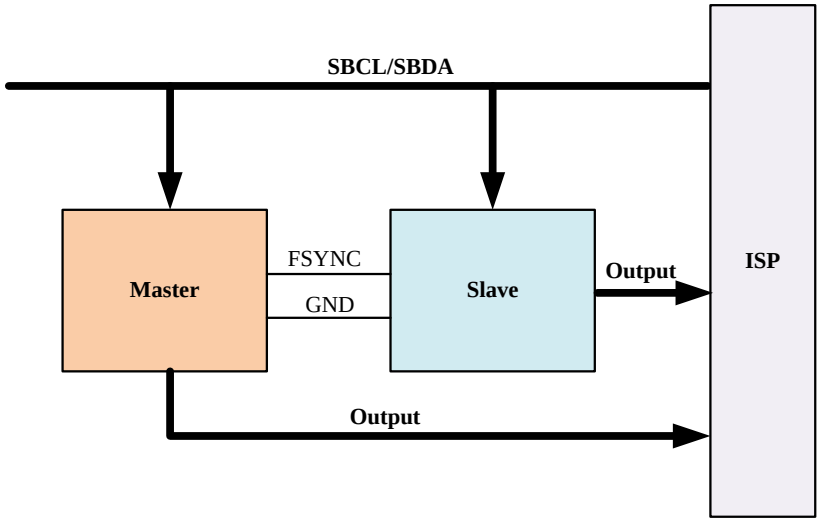
GC2607 has a rectangular pixel array 1920 x 1080, it can be windowed by output size control, the output image windowing can be used to adjust output size, and it will affect field angle.



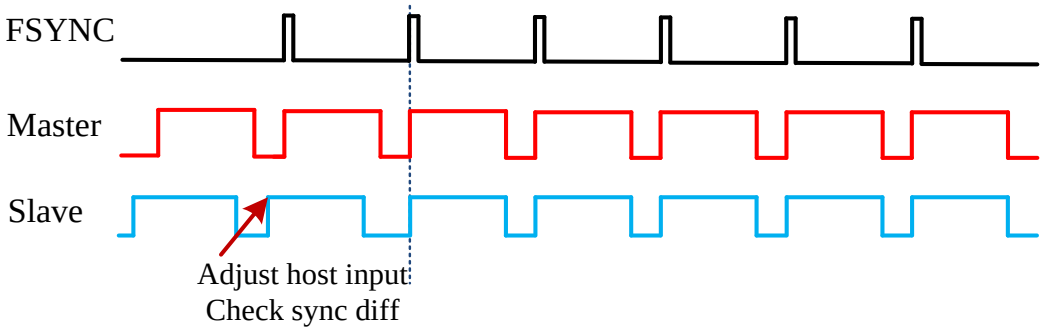
Addr.	Register name	Description
0x0346	Col Start	[3:0] out_win_x1[10:8]
0x0347		[7:0] out_win_x1[7:0]
0x034a	Window height	[2:0] out_win_height[10:8]
0x034b		[7:0] out_win_height[7:0]
0x00c0	Window width	[2:0] out_win_width[10:8]
0x00c1		[7:0] out_win_width[7:1]

9.8 Frame sync mode

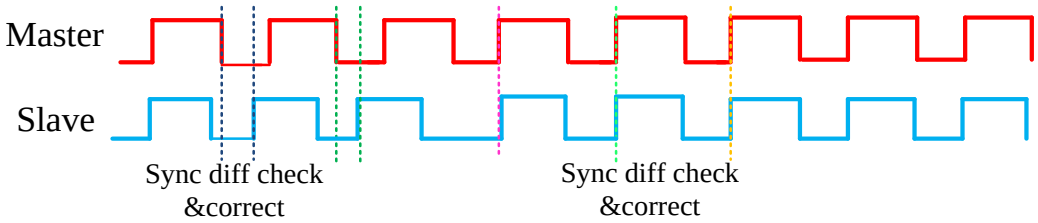
GC2607 can support hardware frame sync for dual camera application. It can be set both master and slave sensor. When use this mode, the two sensor’s FSYNC pin must connect to each other.



Adjust mismatch sync



Dynamic mismatch sync control



Addr.	Register name	Description
0x027f	fsync_mode	[4]fsync_clear_counter [3:0]fsync_mode

0x0282	fsync_mode_new2	
0x0283	fsync_mode_new3	
0x0284	Fsync row time	
0x0285	fsync_mode_new4	
0x0286	fsync_row_diff_th	[5:0] fsync_row_diff_th
0x0287	Debug_mode4	[5:4] fsync_vb_gap
0x0288	fsync_row_diff_big[13:8]	[5:0] fsync_row_diff_big[13:8]
0x0289	fsync_row_diff_big [7:0]	[7:0] fsync_row_diff_big [7:0]
0x028a	fsync_row_diff_big2[13:8]	[5:0] fsync_row_diff_big2[13:8]
0x028b	fsync_row_diff_big2 [7:0]	[7:0] fsync_row_diff_big2[7:0]

9.9 OTP memory

GC2607 sensor has 2K bits embedded OTP (One Time Programmable) memory.

9.10 Frame structure

Frame structure is controlled by HB, frame length, window start, window height, window width and VB.

Frame length control

Frame length are controlled by window height, minimum VB and shutter time.

- Frame length depend shutter time.
  - Minimum frame length = window height + 20 +VB (VB_min = 16)
  - If shutter time < minimum frame length:

    Actual frame length = minimum frame length
  - If shutter time > minimum frame length:

    Actual frame length = shutter time + 16 (recommended).
- Fix frame rate
  - User can fix VB to fix frame rate.

Line length control

Line length = 1200 (not recommended to be modified)

Addr.	Register name	Description
0x0342	Line length	[3:0] Line length[11:8]
0x0343		[7:0] Line length[7:0]

10. Register List

System Register

Address	Name	Width	Default Value	R/W	Description
0x03f0	chip_ID_H	8	0x26	RO	[7:0] Sensor_ID
0x03f1	chip_ID_L	8	0x07	RO	[7:0] Sensor_ID
0x0340	frame_length_h[14:8]	7	0x0c	RW	[15:0]frame_length
0x0341	frame_length_l[7:0]	8	0x60	RW	
0x0342	CISCTL_hb[13:8]	6	0x08	RW	[13:0] CISCTL_hb
0x0343	CISCTL_hb[7:0]	8	0x00	RW	
0x00c0	CISCTL_win_width	4	0x0a	RW	[3:0] CISCTL_win_width[10:8]
0x00c1		8	0x30	RW	[7:1] CISCTL_win_width[7:1] //1304
0x0346	CISCTL_row_start[10:8]	3	0x00	RW	[2:0] CISCTL_row_start[10:8]
0x0347	CISCTL_row_start[7:0]	8	0x02	RW	[7:0] CISCTL_row_start[7:0]
0x034a	CISCTL_win_height	3	0x04	RW	[2:0] CISCTL_win_height[10:8]
0x034b	CISCTL_win_height	8	0x40	RW	[7:0] CISCTL_win_height[7:0]

Analog & CISCTL

Address	Name	Width	Default Value	R/W	Description
0x0202	CISCTL_exp [14:8]	7	0x00	RW	[14:0] tmp_CISCTL_exp_in
0x0203	CISCTL_exp [7:0]	8	0x10	RW	
0x0208	auto_pregain_T1[13:0]	6	0x04	RW	auto_pregain_T1[13:8]
0x0209	buf_CISCTL_capt_hb [7:0]	8	0x00	RW	auto_pregain_T1[7:0]
0x020a	auto_pregain_T2[13:0]	6	0x04	RW	auto_pregain_T2[13:8]
0x020b	buf_CISCTL_capt_vb [7:0]	8	0x00	RW	auto_pregain_T2[7:0]
0x020c	col_gain_T1[11:0]	4	0x00	RW	col_gain_T1[11:8]
0x020d	buf_CISCTL_capt_row_start [7:0]	8	0x40	RW	col_gain_T1[7:0]
0x020e	col_gain_T2[11:0]	4	0x00	RW	col_gain_T2[11:8]
0x020f	buf_CISCTL_capt_col_start [7:1]	8	0x40	RW	col_gain_T2[7:0]

0x02b3	ANALOG_PGA_gain_T1[15:0]	16	0x00	RW	
0x02b4				RW	
0x02b5	ANALOG_PGA_gain_T2[15:0]	16	0x00	RW	
0x02b6				RW	

CSI/PHY1.0

Address	Name	Width	Default Value	R/W	Description
0x0101	Image_Orientation	2	0x00	RW	[1] updown [0] mirror
0x0107	CSI2_mode2	4	0x05	RW	[3] fifo_rst_mode [2]CSI2_mode_update_mode [1] virtual channal [0] mipi_wclk_gate_en
0x0110	mipi_clk_en	1	NA	RO	[0] soc_rclk_enable
0x0112	HDR_T1&T2_VC_ID_set	4	0x00		[3:2] HDR_T1_VC_ID_set [1:0] HDR_T2_VC_ID_set
0x0111	I2C_cm_mipi_rst_n	1	NA	RO	[0] I2C_cm_mipi_rst_n
0x0115	Frame_counter[15：0]	8	0x00	RO	[7:0] frame_counter[15:8]
0x0116	SYNC_set	8	0x00	RO	[7:0] frame_counter[7:0]