GC2053 CSP

1/2.9’’2Mega CMOS Image Sensor

Data Sheet

Rev.1.0

2018-07-31

Ordering Information

◆ **GC2053**

(Colored, 47PIN-CSP)

GENERATION REVISION HISTORY

REV.	*EFFECTIVEDATE*	*DESCRIPTION OF CHANGES*	*PREPARED BY*
V1.0	*2018-07-31*	*Document Release*	*DSC-AE Dept.*

Galaxycore Incorporation

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Content

1. Sensor Overview

1.1 General Description

GC2053 is a high quality 1080P CMOS image sensor, for security camera products, digital camera products and mobile phone camera applications. GC2053 incorporates a 1920H x 1080V pixel array, on-chip 10-bit ADC, and image signal processor.

The full scale integration of high-performance and low-power functions makes the GC2053 best fit the design, reduce implementation process, and extend the battery life of Motion Camera, Car DVR, and a wide variety of mobile applications.

It provides RAW10 and RAW8 data formats with MIPI and DVP interface. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Standard optical format of 1/2.9 inch
- 2.8um*2.8um
- Output formats: Raw Bayer 10bit/8bit
- Power supply requirement: AVDD28: 2.7~3.3V(Typ.2.8V)
  DVDD18: 1.15~1.3V(Typ.1.2V)
  IOVDD: 1.7~3.0V(Typ.1.8V)
- PLL support
- Support frame sync
- DVP /MIPI (2lane) interface support
- Horizontal/Vertical mirror
- Image processing module
- OTP support(1K for customers):Module information/WB
- Package: CSP

1.3 Application

- Security cameras
- Automotive
- Cellular Phone Cameras
- Digital still cameras and camcorders
- Video telephony and conferencing equipment

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/2.9inch
Pixel Size	2.8um x2.8um
Active pixel array	1920 x 1080
Shutter type	Electronic rolling shutter
ADC resolution	10 bit ADC
Max Frame rate	30fps@full size
Power Supply	AVDD28: 2.8V DVDD: 1.2V IOVDD: 1.8V
Power Consumption	TBD
SNR	TBD
Dark Current	TBD
Sensitivity	TBD
Dynamic range	TBD
Operating temperature:	-20~80℃
Stable Image temperature	0~60℃
Optimal lens chief ray angle(CRA)	12 °(linear)
Package type	CSP
Input clock frequency	6~27MHz

s

2. DC Parameters

2.1 Standby Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	TBD	TBD	uA
Digital	I_{DVDD}	—	TBD	TBD	uA
I/O	I_{IOVDD}	—	TBD	TBD	uA

RST: L, PWND: L

Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

2.2 Power off Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	TBD	TBD	uA
Digital	I_{DVDD}	—	TBD	TBD	uA
I/O	I_{IOVDD}	—	TBD	TBD	uA

Power off, T_j=25℃

2.3 Operation current

Full size (DVP)

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	TBD	TBD	mA
Digital	I_{DVDD}	—	TBD	TBD	mA
I/O	I_{IOVDD}	—	TBD	TBD	mA

Input clock: 27MHz, Frame rate: 30FPS, RAW 10,

Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

Full size (MIPI 2 Lane)

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	TBD	TBD	mA
Digital	I_{DVDD}	—	TBD	TBD	mA
I/O	I_{IOVDD}	—	TBD	TBD	mA

Input clock: 27MHz, Frame rate: 30FPS, RAW 10,

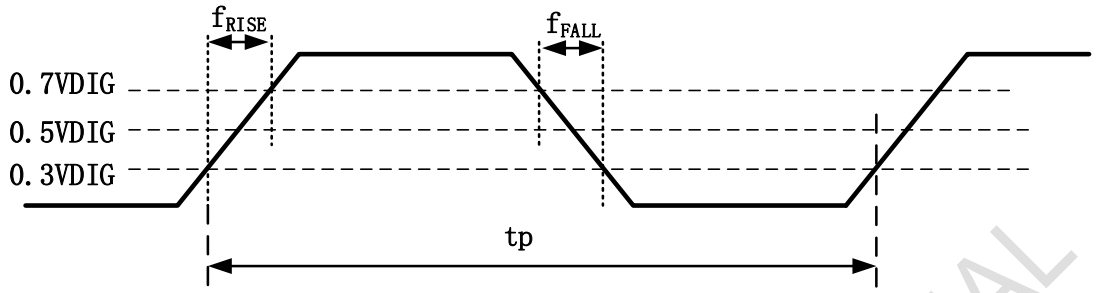
Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

2.4 DC Characteristics

Item	Symbol	Min	Typ	Max	Unit
Power supply	V_{AVDD}	2.7	2.8	3.3	V
	V_{DVDD}	1.15	1.2	1.3	V
	V_{IOVDD}	1.7	1.8	3.3	V
Digital Input(Conditions: AVDD = 2.8V, DVDD =1.2V, IOVDD = 1.8V)					
Input voltage HIGH	V_{IH}	0.7*VIF			V
Input voltage LOW	V_{IL}			0.3*VIF	V
Digital Output(Conditions: AVDD =2.8V, IOVDD = 1.8V, standard Loading 25PF)					
Output voltage HIGH	V_{OH}	0.8*VIF			V
Output voltage LOW	V_{OL}			0.2*VIF	V

3. AC Characteristics

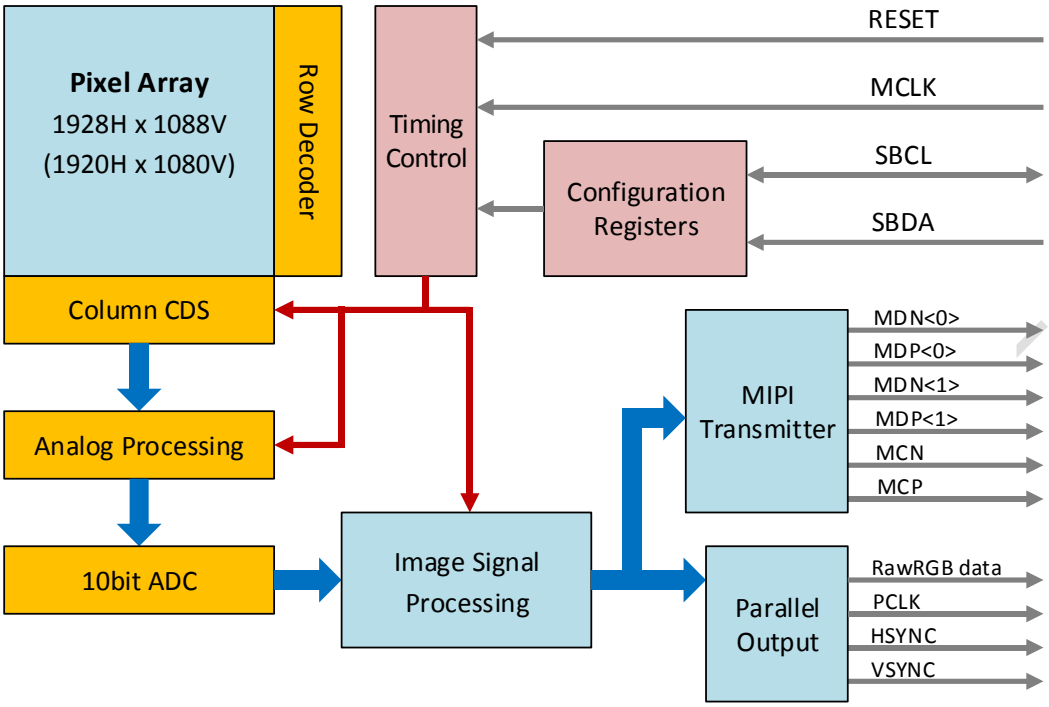
Master clock wave diagram



Input clock square waveform specifications：

Item	Symbol	Min	Typ	Max	unit
Frequency	f_{SCK}	6	24	27	MHz
jitter (period, peak-to-peak)	T_{jitter}			600	ps
Rise Time	f_{RISE}	1		15	ns
Fall Time	f_{FALL}	1		15	ns
Duty Cycle	f_{DUTY}	40		60	%
Input Leakage	f_{ILEAK}	-10		10	μA

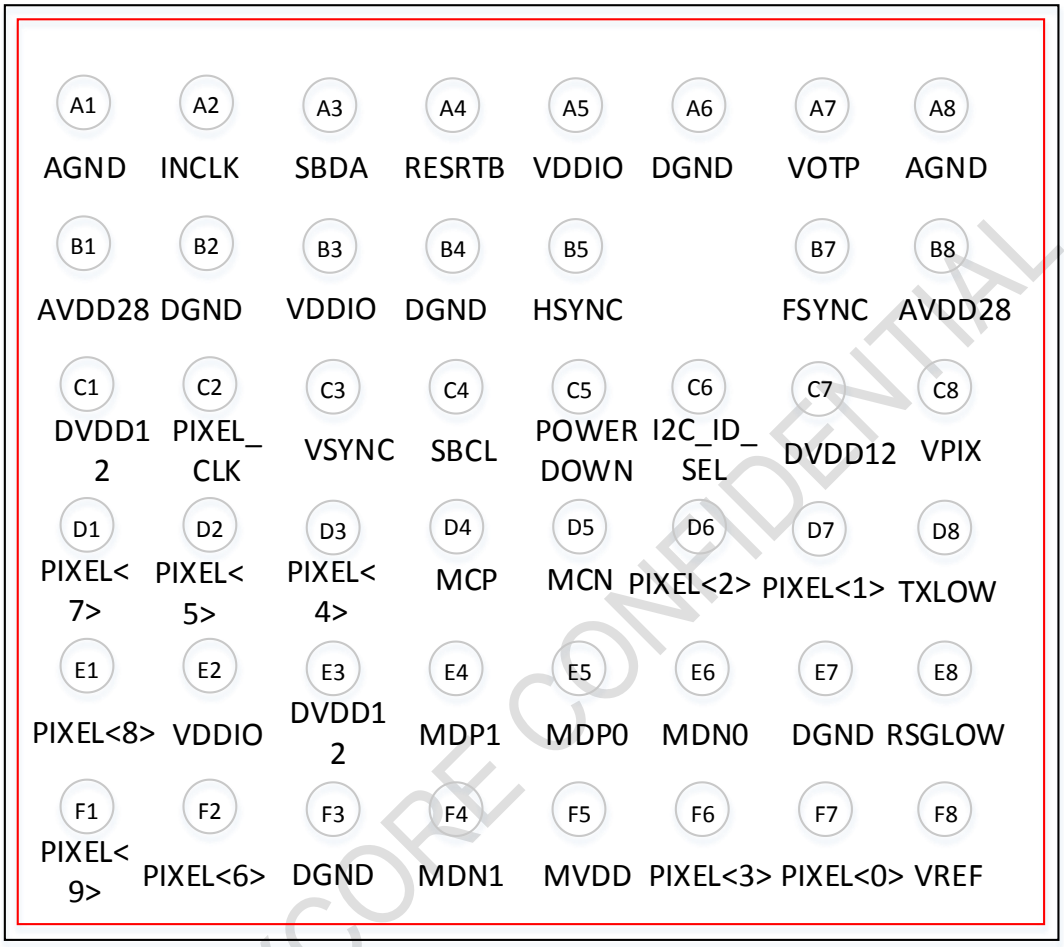
4. Block Diagram



GC2053 has an active image array of 1920x1080 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 10 bit A/D converter. The digital signals are processed in the ISP Block. Users can easily control these functions via two-wire serial interface bus.

5. CSP Package Specifications

5.1 Pin Diagram (CSP)



Top View

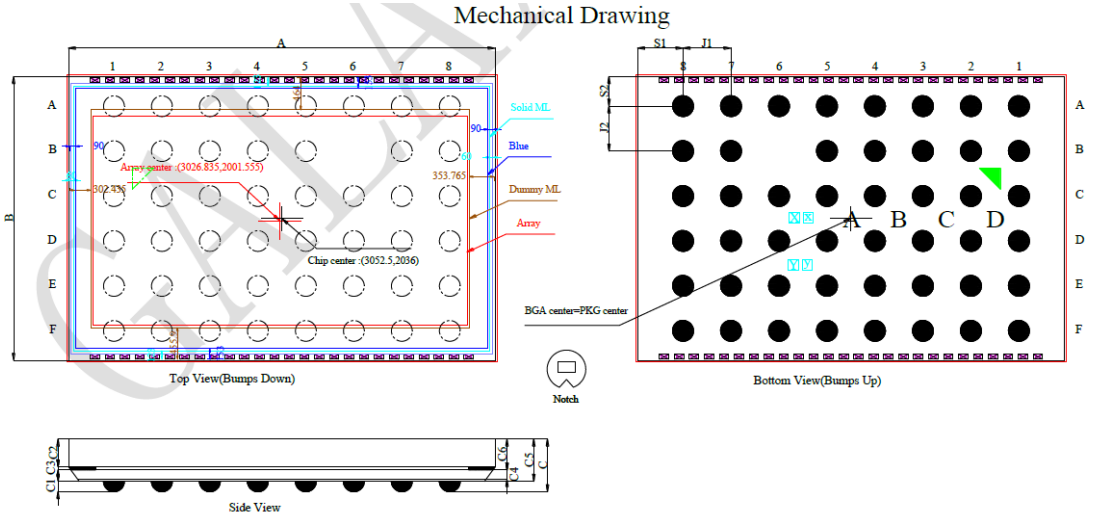
5.2 Pin Descriptions

Pin	Name	Pin Type	Description
A1	AGND	Ground	Ground for analog
A2	INCLK	Input	Sensor input clock
A3	SBDA	I/O	Two-wire serial bus, data
A4	RESETB	Input	Chip reset control: 0: chip reset 1: normal work
A5	VDDIO	POWER	I/O POWER.
A6	DGND	Ground	Ground for digital

A7	VOTP	POWER	For OTP power supply
A8	AGND	Ground	Ground for analog
B1	AVDD28	AVDD28	ANALOG POWER
B2	DGND	Ground	Ground for digital
B3	VDDIO	POWER	I/O POWER
B4	DGND	Ground	Ground for digital
B5	HSYNC	Output	DVP HSYNC
B6	\	\	\
B7	FSYNC	I/O	Frame sync control
B8	AVDD28	POWER	ANALOG POWER
C1	DVDD12	POWER	DIGITAL POWER
C2	PIXEL_CLK	Output	DVP CLK
C3	VSYNC	Output	DVP VSYNC
C4	SBCL	Input	Two-wire serial bus, clock
C5	POWERDOWN	Input	Sensor power down control: 0: standby 1: normal work
C6	I2C_ID_SEL	Input	ID_SEL *0: 0x6e/0x6f (default)* 1: 0x7e/0x7f
C7	DVDD12	POWER	DIGITAL POWER
C8	VPIX	POWER	Internal power supply
D1	PIXEL<7>	Output	DVP07
D2	PIXEL<5>	Output	DVP05
D3	PIXEL<4>	Output	DVP04
D4	MCP	Output	MIPI clock (+)
D5	MCN	Output	MIPI clock (-)
D6	PIXEL<2>	Output	DVP02
D7	PIXEL<1>	Output	DVP01

D8	TXLOW	POWER	Internal power supply
E1	PIXEL<8>	Output	DVP08
E2	VDDIO	POWER	I/O POWER
E3	DVDD12	POWER	DIGITAL POWER
E4	MDP1	Output	MIPI data <1> (+)
E5	MDP0	Output	MIPI data <0> (+)
E6	MDN0	Output	MIPI data <0> (-)
E7	DGND	Ground	Ground for digital
E8	RSGLOW	POWER	Internal power supply
F1	PIXEL<9>	Output	DVP09
F2	PIXEL<6>	Output	DVP06
F3	DGND	Ground	Ground for digital
F4	MDN1	Output	MIPI data <1> (-)
F5	MVDD	Power	DIGITAL POWER
F6	PIXEL<3>	Output	DVP03
F7	PIXEL<0>	Output	DVP00
F8	VREF	POWER	Internal power supply

5.3 Package Specification (unit: mm)



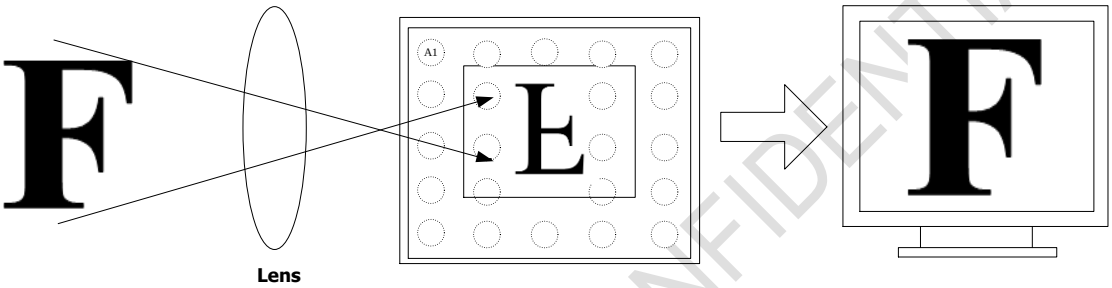
Description	symbol	Nominal	Min	Max
		Millimeters		
Package Body Dimension X	A	6.1350	6.1100	6.1600
Package Body Dimension Y	B	4.1020	4.0770	4.1270
Package Height	C	0.7600	0.7050	0.8150
Ball Height	C1	0.1500	0.1200	0.1800
Glass Thickness	C2	0.4000	0.3900	0.4100
CV Thickness	C3	0.0410	0.0370	0.0450
Silicon Thickness	C4	0.1300	0.1230	0.1370
Package Body Thickness	C5	0.6100	0.5750	0.6450
Thickness from top glass surface to wafer	C6	0.4450	0.4250	0.4650
Ball Diameter	D	0.3000	0.2700	0.3300
Total Ball Count	N	47		
Ball Count X axis	N1	8		
Ball Count Y axis	N2	6		

Pins pitch X axis	J1	0.6900		
Pins pitch Y axis	J2	0.6500		
BGA ball center to package center offset in X-direction	X	0.0000	-0.0250	0.0250
BGA ball center to package center offset in Y-direction	Y	0.000	-0.0250	0.0250
BGA ball center to chip center offset in X-direction	X1	0.000	-0.0250	0.0250
BGA ball center to chip center offset in Y-direction	Y1	0.000	-0.0250	0.0250
Edge to Pin Center Distance along X	S1	0.6525	0.6225	0.6825
Edge to Pin Center Distance along Y	S2	0.4260	0.3960	0.4560

6. Optical Specifications

6.1 Readout Position

The GC2053 default status is readout from the lower left corner with pin A1 located in the upper left corner. The image is inverted vertically and horizontally by the lens, so proper image output results when Pin A1 is located in the upper left corner.

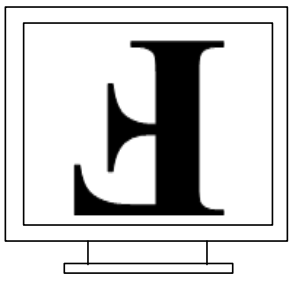


Readout direction can be set by the registers.

Function	Register Address	Register Value	First Pixel
Normal	P0:0x17[1:0]	00	Gr
Horizontal mirror	P0:0x17[1:0]	01	R
Vertical Flip	P0:0x17[1:0]	10	B
Horizontal Mirror and Vertical Flip	P0:0x17[1:0]	11	Gb

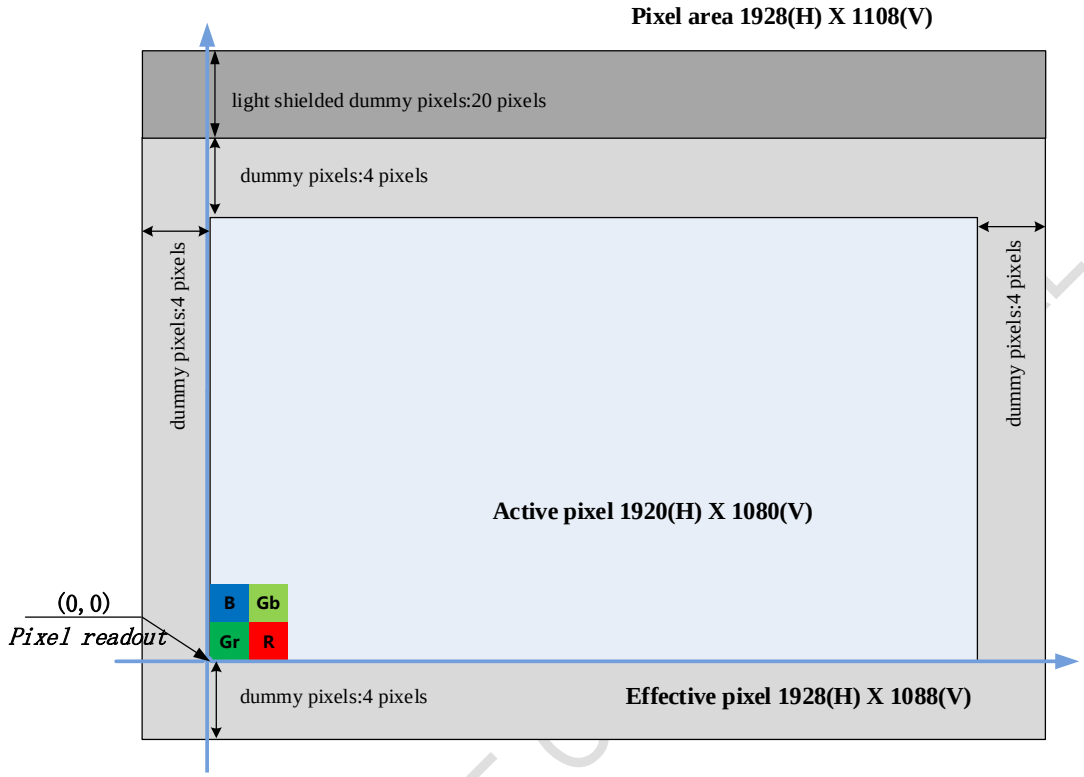
Horizontal Mirror

Vertical Flip



Horizontal Mirror and Vertical Flip

6.2 Pixel Array



Pixel array is covered by Bayer pattern color filters. The primary color GR/BG array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 1919. If flip in column, column is read out from 1919 to 0.

If no flip in row, row is read out from 0 to 1079.If flip in row, row is read out from 1079 to 0.

6.3 Lens Chief Ray Angle (CRA)

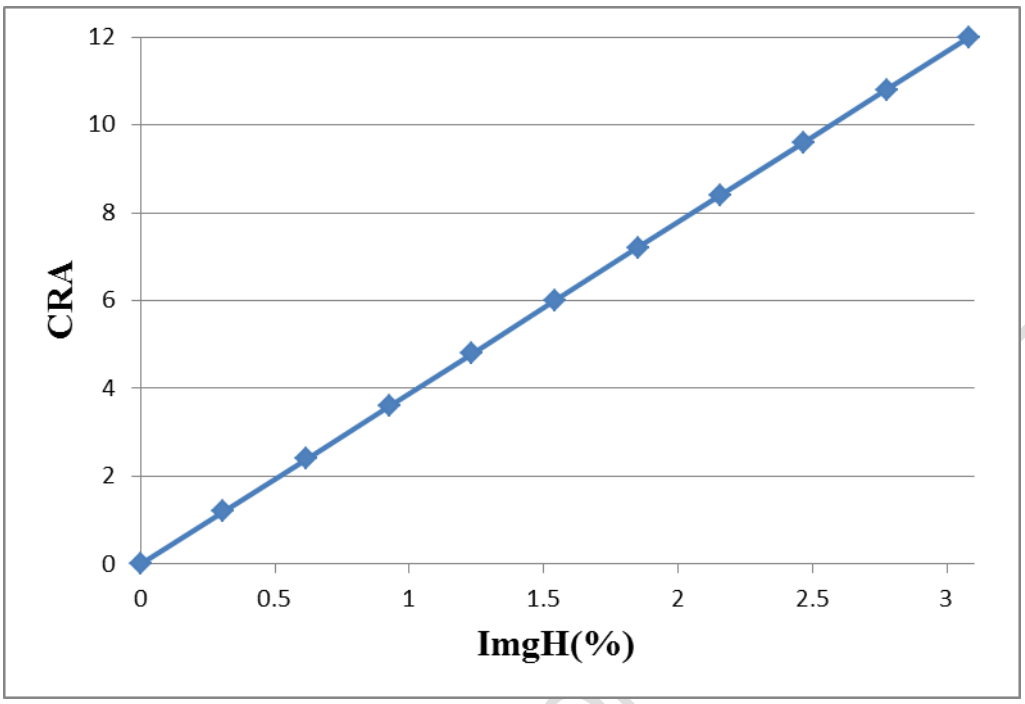
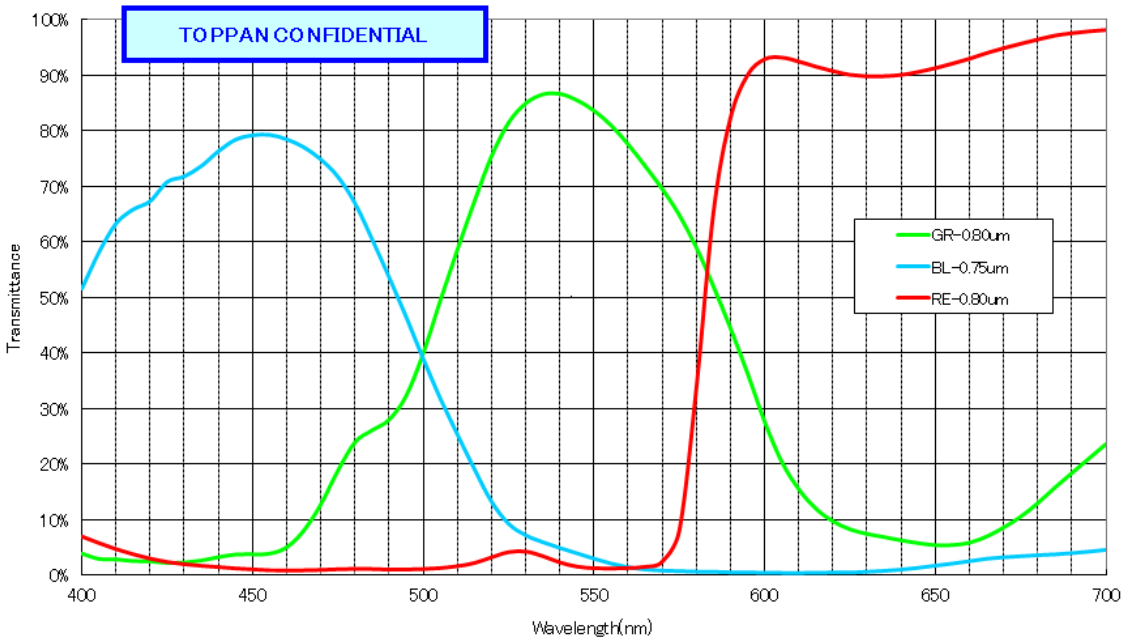


Image Height (%)	Image Height (mm)	CRA (degree)
0	0	0
10	0.3085	1.2
20	0.617	2.4
30	0.9255	3.6
40	1.234	4.8
50	1.5425	6
60	1.851	7.2
70	2.1595	8.4
80	2.468	9.6
90	2.7765	10.8
100	3.085	12

6.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below



7. Two-wire Serial Bus Communication

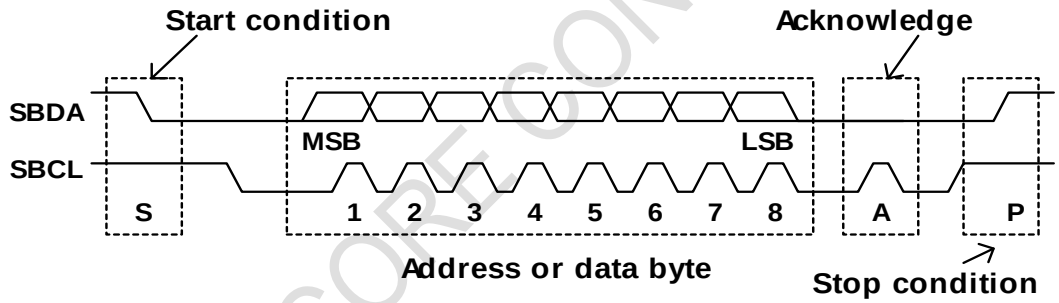
GC2053 Device Address:

ID_SEL	Slave address write mode	Slave address read mode
0(default)	**0x6e**	**0x6f**
1	**0x7e**	**0x7f**

7.1 Protocol

The host must perform the role of a communications master and GC2053 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**.



Single Register Writing:

S	6eH	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	6eH	A	Register Address	A	Data(1)	A	……	Data(N)	A	P

Single Register Reading:

S	6eH	A	Register Address	A	S	6fH	A	Data	NA	P

Notes:

From master to slave

From slave to master

S: Start condition

P: Stop condition

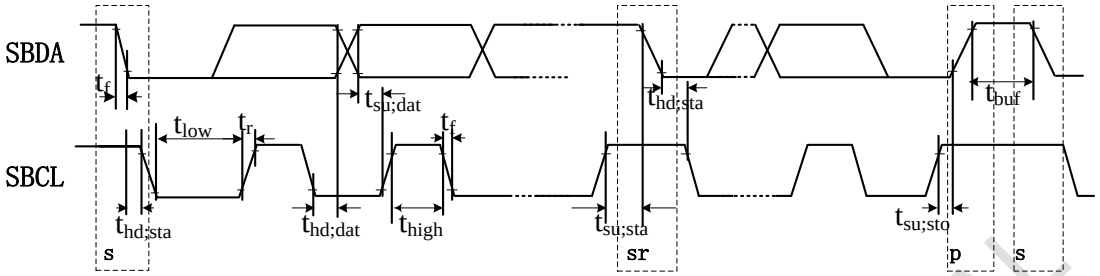
A: Acknowledge bit

NA: No acknowledge

Register Address: Sensor register address

Data: Sensor register value

7.2 Serial Bus Timing

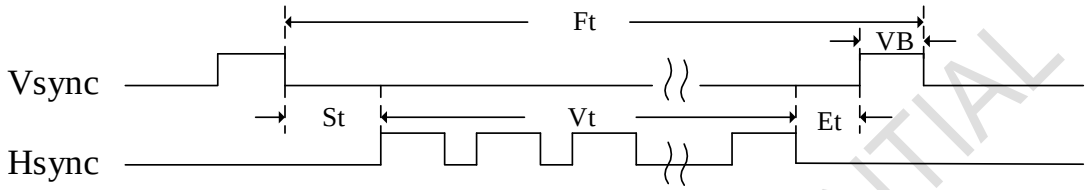


Parameter	Symbol	Min.	Typ.	Max.	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between stop and start condition	t_{buf}	1.3	--	--	μs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for a repeated start	$t_{su;sta}$	0.6	--	--	μs
Data hold time	$t_{hd;dat}$	0	--	0.9	μs
Data Set-up time	$t_{su;dat}$	100	--	--	Ns
Rise time of SBCL, SBDA	t_r	--	--	300	Ns
Fall time of SBCL, SBDA	t_f	--	--	300	Ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	--	Pf

8. Applications

8.1 DVP timing

Suppose Vsync is low active and Hsync is high active, and output format is RAW Bayer 10bit/8bit, then the timing of Vsync and Hsync is bellowing:



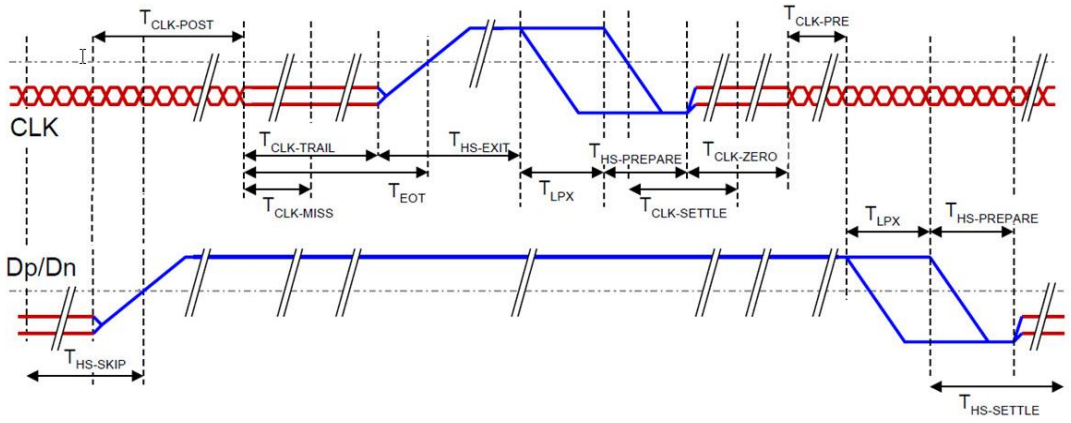
Ft = Vt + 20 + VB；(St + Et = 20)

Ft -> Frame time, one frame time.

Vt -> valid line time. Vt = win_height, win_height is setting by register P0:0x0d and P0:0x0e.

VB->Vblank,setting by register P0:0x07 and P0:0x08

8.2 Clock lane low-power



Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

$T_{CLK\_HS\_PREPARE}$: setting by Register P3: 0x22

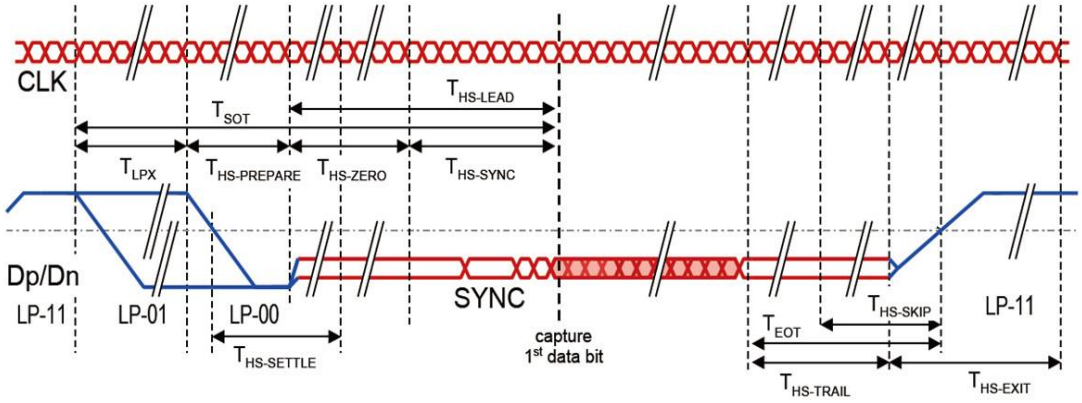
T_{CLK_ZERO}: setting by Register P3: 0x23

T_{CLK_PRE}: setting by Register P3: 0x24

T_{CLK_POST}: setting by Register P3: 0x25

T_{CLK_TRAIL}: setting by Register P3: 0x26

8.3 Data Burst



Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

T_{LPX}: setting by Register P3:0x21

$T_{HS\_PREPARE}$: setting by Register P3: 0x29

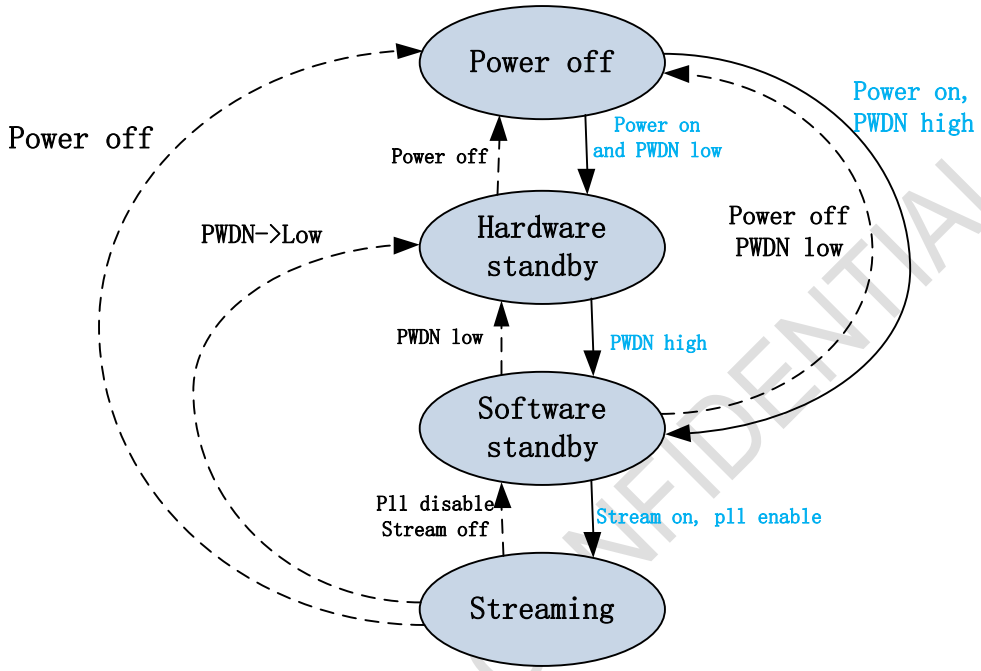
T_{HS_ZERO}: setting by Register P3: 0x2a

T_{HS_TRAIL}: setting by Register P3: 0x2b

T_{HS_EXIT}: setting by Register P3: 0x27

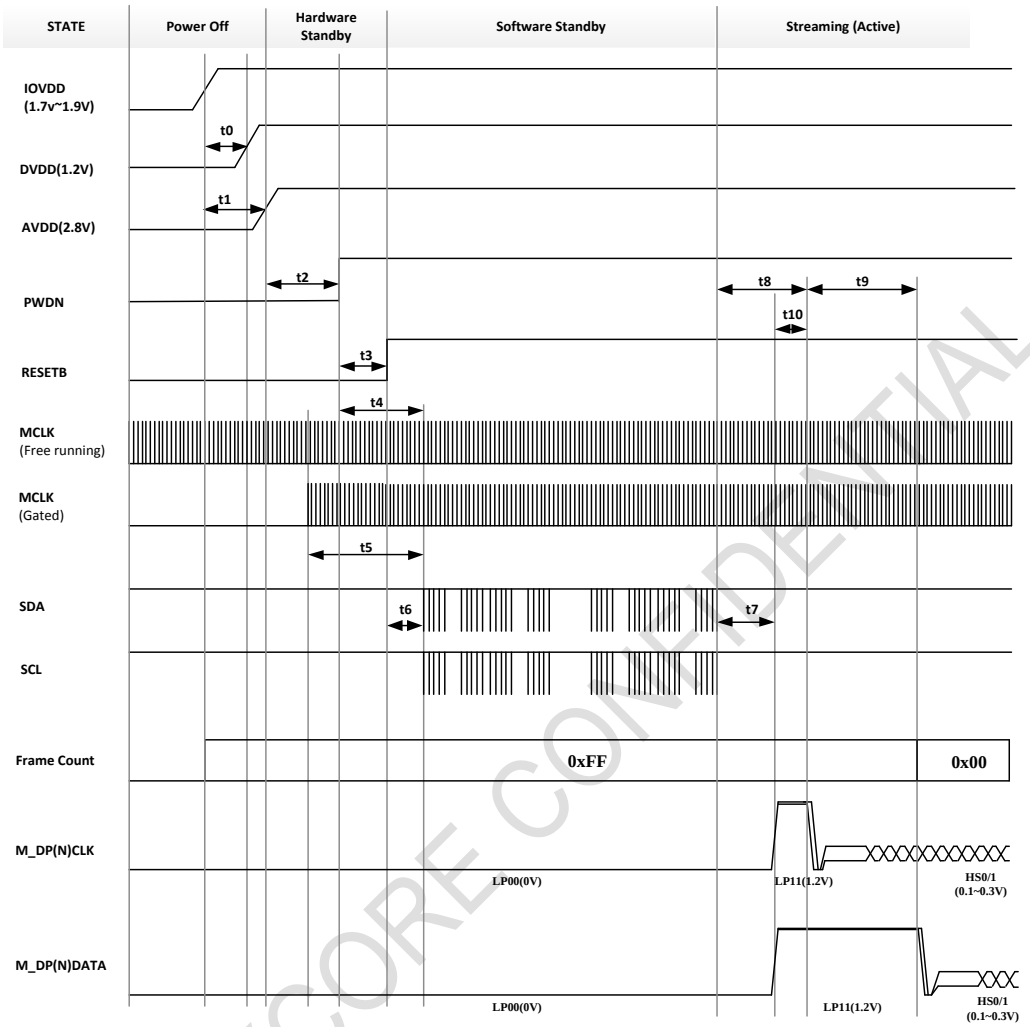
9. Function description

9.1 Operation mode



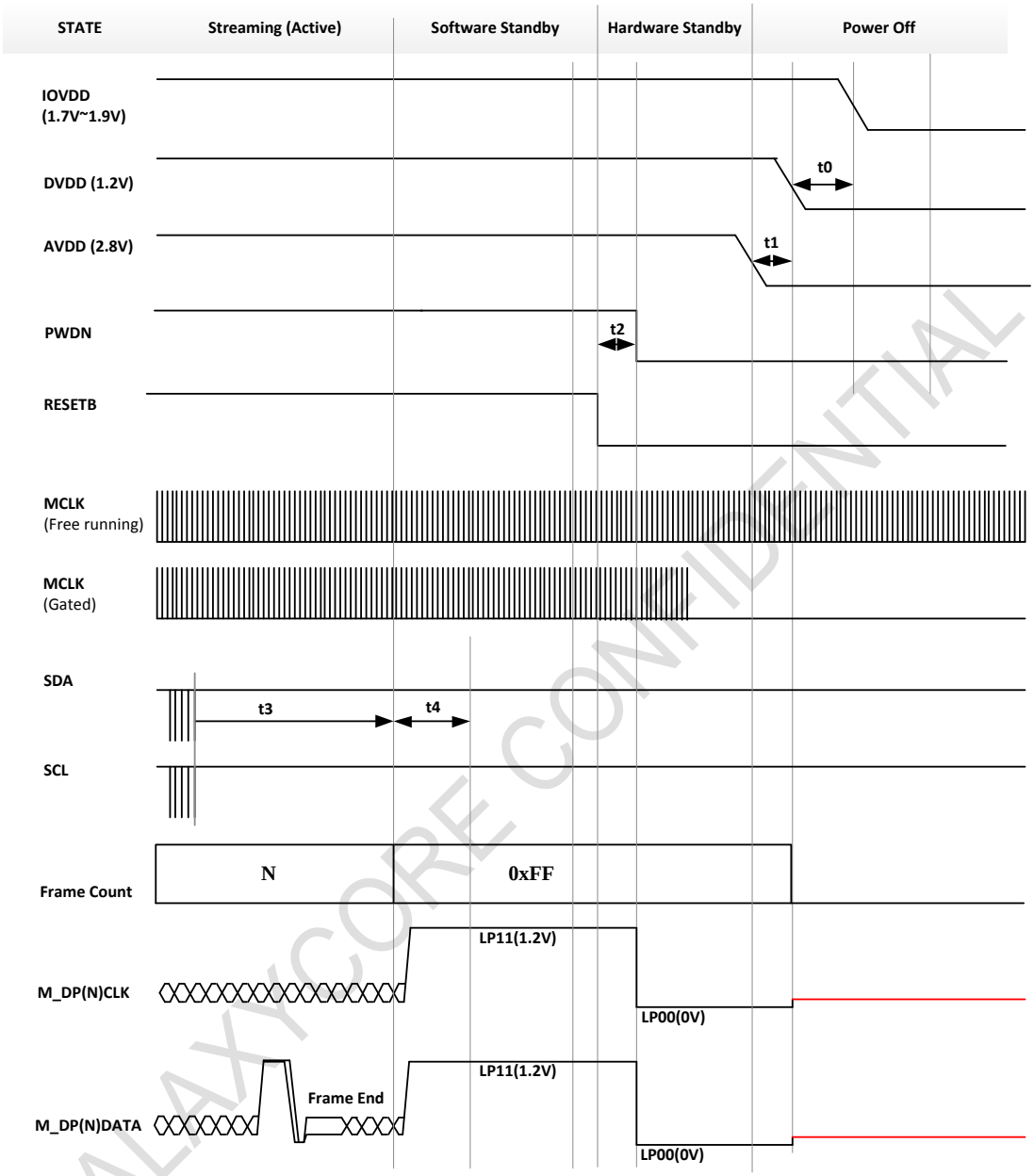
Power state	Description	Activate
Power off	Power supplies are turned off	None
Hardware standby	No communication with sensor, low level on PWDN and RESETB, and stop MCLK	PWDN low
Software standby	Two- wire serial communication with sensor, pll is ready for fast return to streaming mode	Stream mode off PLL disable RESETB high PWDN high
Streaming	Sensor is fully powered and is streaming image data on the MIPI CSI-2 bus	All

9.2 Power on Sequence



Parameter	Description	Min.	Max.	Unit
t0	From IOVDD to DVDD12	50	-	μs
t1	From IOVDD to AVDD28	50	-	μs
t2	From AVDD28 to PWDN pull high	0	-	μs
t3	From PWDN pull high to RESETB pull high	0	-	μs
t4	PWDN rising to first I2C transaction	50	-	μs
t5	Minimum No. of MCLK cycles prior to the first I2C transaction	1200	-	MCLK
t6	From RESETB rising to first I2C transaction	50	-	μs
t7	PLL start up/lock time	-	1	ms
t8	Entering streaming mode – First frame start sequence (fixed part)		10	ms
t9	Entering streaming mode – First frame start sequence (variable part)	-		lines
t10	DPHY initialization period (TINIT)	0.1	-	ms

9.3 Power off Sequence



Parameter	Description	Min.	Max.	Unit
t0	From DVDD12 pull down to IOVDD pull down	0	-	μs
t1	From AVDD28 pull down to DVDD12 pull down	0	-	μs
t2	From RESETB pull low to PWDN pull low	0	-	μs
t3	Enter Software Standby CCI command – Device in Software Standby mode	0	-	μs
t4	Minimum number of MCLK cycles after the last CCI transaction or MIPI frame end code.	2000		MCLK

- If the sensor's power cannot be cut off, please keep power supply, then set PWDN pin low. It will make sensor standby

- Register should be reloaded before works.
- If the standby sequence needs to be modified, please contact FAE of *Galaxycore Inc.*

9.4 Black level calibration

Black level is caused by pixel characteristics and analog channel offset, which makes poor image quality in dark condition and color balance, to reduce these, sensor automatically calibrates the black level every frame with light shield pixel array.

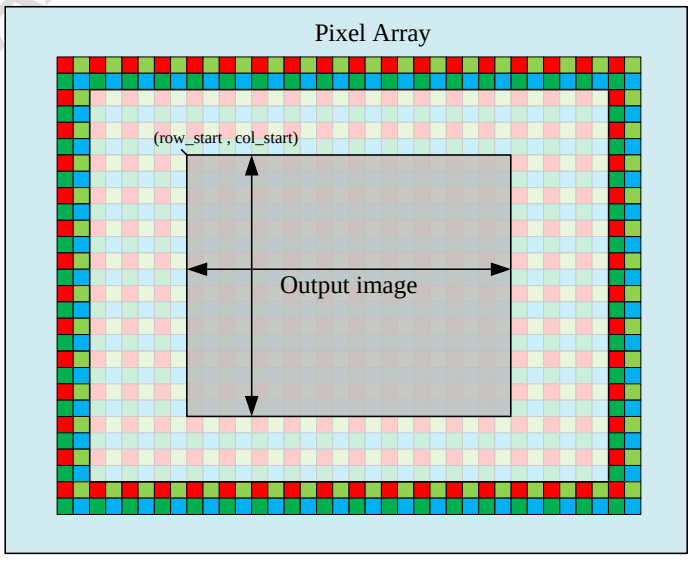
9.5 Integration time

The integration time is controlled by the integration time registers

Addr.	Register name	Description
P0:0x03	Shutter time	[5:0] shutter time[13:8]
P0:0x04		[7:0] shutter time[7:0]
P0:0x41	Frame length	[5:0] frame length[13:8]
P0:0x42		[7:0] frame length[7:0]

9.6 Windowing

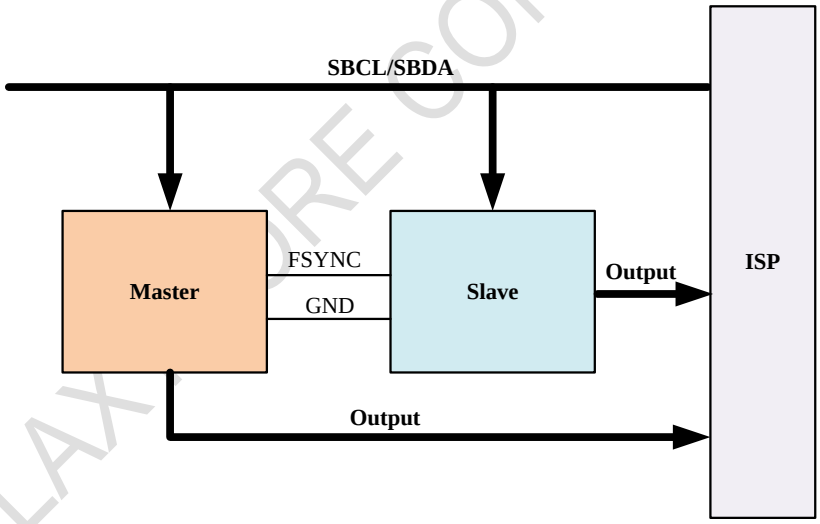
GC2053 has a rectangular pixel array 1920 x 1080, it can be windowed by output size control, the output image windowing can be used to adjust output size, and it will affect field angle.



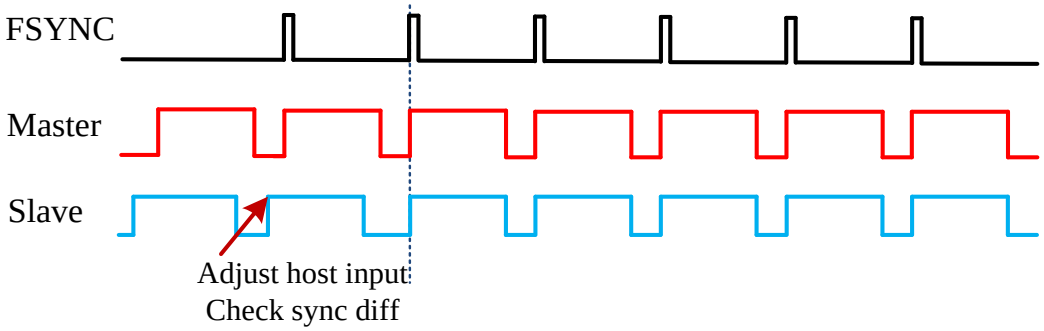
Addr.	Register name	Description
P0:0x0d	win_height	[2:0]win_height[10:8]
P0:0x0e		[7:0]win_height[7:0]
P0:0x0f	win_width	[3:0]win_width[11:8]
P0:0x10		[7:0]win_width[7:0]
P0:0x09	Row start	[2:0]row_start[10:8]
P0:0x0a		[7:0]row_start [7:0]
P0:0x0b	Col start	[2:0]col_start[10:8]
P0:0x0c		[7:0]col_start[7:0]

9.7 Frame sync mode

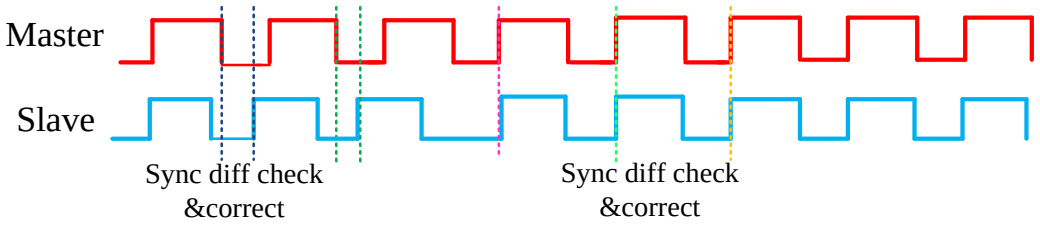
GC2053 can support hardware frame sync for dual camera application. It can be set both master and slave sensor. When use this mode, the two sensor's FSYNC pin must connect to each other.



Adjust mismatch sync



Dynamic mismatch sync control



Addr.	Register name	Description
P0:0x7f	fsync_mode	[4]fsync_clear_counter [3:0]fsync_mode
P0:0x82	fsync_mode_new2	
P0:0x83	fsync_mode_new3	
P0:0x84	Fsync row time	
P0:0x85	fsync_mode_new4	
P0:0x86	fsync_row_diff_th	[5:0] fsync_row_diff_th
P0:0x87	Debug_mode4	[5:4] fsync_vb_gap
P0:0x88	fsync_row_diff_big[13:8]	[5:0] fsync_row_diff_big[13:8]
P0:0x89	fsync_row_diff_big [7:0]	[7:0] fsync_row_diff_big [7:0]
P0:0x8a	fsync_row_diff_big2[13:8]	[5:0] fsync_row_diff_big2[13:8]
P0:0x8b	fsync_row_diff_big2 [7:0]	[7:0] fsync_row_diff_big2[7:0]

9.8 OTP memory

GC2053 sensor has 1K bits embedded OTP(One Time Programmable) memory, 256 bits are for customers , which is for storing camera module calibration date.

9.9 Frame structure

Frame structure is controlled by HB, frame length, window start, window height, window width and VB.

Frame length control

Frame length are controlled by window height, minimum VB and shutter time.

- Frame length depend shutter time.

- Minimum frame length = window height + 20 +VB (VB_min = 16)

- If shutter time < minimum frame length:

Actual frame length = minimum frame length

- If shutter time > minimum frame length:

  Actual frame length = shutter time + 16 (recommended).

- Fix frame rate

- User can fix VB to fix frame rate.

Line length control

Line length = 1200 (not recommended to be modified)

Addr.	Register name	Description
P0:0x05	Line length	[3:0] Line length[11:8] X2
P0:0x06		[7:0] Line length[7:0] X2

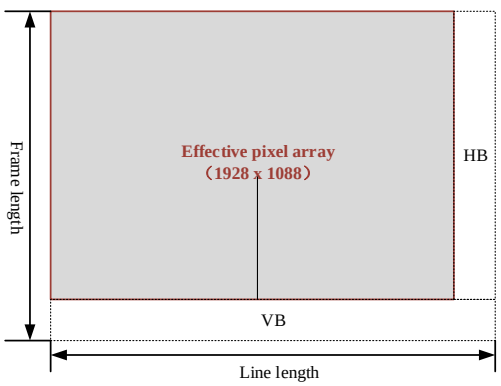
Output window array control

Addr.	Register name	Description
P1:0x91	Out_window_y1	[2:0] Out_window_y1[10:8]
P1:0x92		[7:0] Out_window_y1[7:0]
P1:0x93	Out_window_x1	[3:0] Out_window_x1[11:8]
P1:0x94		[7:0] Out_window_x1[7:0]
P1:0x95	Out window height	[2:0] Out window height[10:8]
P1:0x96		[7:0] Out window height[7:0]
P1:0x97	Out window width	[3:0] Out window width[11:8]
P1:0x98		[7:0] Out window width[7:0]

Blank time control

1. line blank time is controlled by HB
2. frame blank time

   - frame blank time = frame length lines – window height – 20



10. Register List

System Register

Address	Name	Width	Default Value	R/W	Description
0xf0	CHIP_ID_high	8	0x20	RO	[7:0]CHIP ID high
0xf1	CHIP_ID_low	8	0x53	RO	[7:0]CHIP ID low
0xf2	OTP_clk_gate OTP_mode_temp I2C_open_ena pwd_dn	5	0x00	RW	[7] OTP_clk_gate [6:4] OTP_mode_temp [1] I2C_open_ena [0]pwd_dn
0xf3	Spad_vb_hiz_mode Spad_buf_mode Sdata_pad_io Ssync_pad_io	8	0x0f	RW	[7] OTP_finish [6] OTP_busy [5] Spad_vb_hiz_mode [4] Spad_buf_mode [3] Sdata_pad_io [2:0] Ssync_pad_io
0xf4	reduce_power_mode PLL_mode3	8	0x36	RW	[7] reduce_power_mode [6:4]PLL_ldo_set [3:0]spi_clk_div
0xf5	Cp_clk_mode	8	0x80	RW	[7]soc_mclk_enable [6] pll_ldo_en [5:4]cp_clk_del [3:0]cp_clk_div
0xf6	Wpllclk_div Refmp_div	8	0x15	RW	[7:3]wpllclk_div 10000:div5 01000:div4 00100:div3 00010:div2.5 00001:div2 [2:0]refmp_div
0xf7	PLL_mode1	8	0x00	RW	[7]refdiv2d5_en [6]refdiv1d5_en [5:4]scaler_mode(dvpmode) [3]refmp_enb [2]freq div2 [1]div2en [0]pll_en
0xf8	PLL_mode2	8	0x4b	RW	[7:0]pllmp_div
0xf9	Rpllclk_div Pllmp_prediv Analog_pwc	8	0x83	RW	[7:3]rpllclk_div 10000:div5 01000:div4

					00100:div3 00010:div2.5 00001:div2 [2:1]pllmp_prediv [0]analog_pwc
0xfa	clk_div_mode	8	0x00	RW	[7]div2 enable [6]div2 frame [5]divmp_enp 0:en 1:off [4]NA [3]spi_clk-en [2]div2_mode [1]div2 [0]div1
0xfb	i2c_device_id	8	0x6e	RO	[7:1] i2c_device_id [0] NA
0xfc	cm_mode	8	0x00	RW	[7] regf clk enable [6] sys_rclk_sel [5] sys_wclk_sel [4:3]spi_sel_mode 00:spi_sel_rpll 01:spi_sel_wpll 10:spi_sel_serial_clk [2] serail_clk enable [1] re_lock_pll [0] not_use_pll
0xfd	Mclk_sel REGF_BUF_mode	6	0x00	RW	[7]mclk_sel [6]hold function [5]regf_buf_clk_en [4]cen_mode [3]buf_en [2]page_select_mode [1:0]sel_flag//[1]sel_buf2,[0]sel_buf1
0xfe	Page_select	3	0x00	RW	[2:0]page select

Analog & CISCTL

Address	Name	Width	Default Value	R/W	Description
P0:0x03	CISCTL_buf_exp_in [13:8]	6	0x00	RW	[7:6] NA [5:0] CISCTL_cur_exp_out[13:8]
P0:0x04	CISCTL_buf_exp_in [7:0]	8	0x10	RW	[7:0] CISCTL_cur_exp_out[7:0]
P0:0x05	buf_CISCTL_capt_hb[11:8]	4	0x04	RW	CISCTL_hb
P0:0x06	buf_CISCTL_capt_hb [7:0]	8	0x48	RW	
P0:0x07	buf_CISCTL_capt_vb [13:8]	6	0x00	RW	CISCTL_vb
P0:0x08	buf_CISCTL_capt_vb [7:0]	8	0x20	RW	if current exposure < (Vb + window Height) , frame rate will be (Vb + window Height); otherwise frame rate will be determined by exposure
P0:0x09	buf_CISCTL_capt_row_start[10:8]	3	0x00	RW	[7:4] reserved
P0:0x0a	buf_CISCTL_capt_row_start [7:0]	8	0x00	RW	[3:0]Row Start[11:8] Row Start[7:0]
P0:0x0b	buf_CISCTL_capt_col_start [10:8]	3	0x00	RW	[3:0] colstart[10:8]
P0:0x0c	buf_CISCTL_capt_col_start [7:1]	8	0x00	RW	[7:1] colstart[7:1] [0] NA
P0:0x0d	buf_CISCTL_capt_win_height[10:8]	3	0x04	RW	[7:3] NA
P0:0x0e	buf_CISCTL_capt_win_height [7:0]	8	0x48	RW	[2:0] Window height[10:8] Window height[7:0]
P0:0x0f	buf_CISCTL_capt_win_width [10:8]	3	0x07	RW	[7:3] NA [2:0] Window width[11:8]
P0:0x10	buf_CISCTL_capt_win_width [7:0]	8	0x90	RW	[7:0]window width[7:0]
P0:0x13	CISCTL_vs_st	8	0x10	RW	vs_st
P0:0x14	CISCTL_vs_et	8	0x04	RW	vs_et
P0:0x7f	fsync_clear_counter fsync_mode	5	0x08		[4]fsync_clear_counter [3:0]fsync_mode
P0:0x80	Fsync_mode_global	8	0x00		[7]fsync_vb_gap_lasts [6]strobe_output [5]fsync_out_polarity [4]fsync_in_polarity [3]gpio_mode [2]gpio_value [1]vsync_out_mode [0]fsync_every_frame_slave

P0:0x81	Fsync_mode_new	8	0x13		
P0:0x82	Fsync_mode_new2	8	0x00		
P0:0x83	Fsync_mode_new3	8	0x04		
P0:0x84	Fsync_rowtime	8	0x00		
P0:0x85	Fsync_mode_new4	8	0x01		[7]fsync_vb_gap_mode_tmp [6]fsync_vb_first_mode_tmp [5]fsync_row_diff_mode [4]fsync_vb_mode
P0:0x86	Fsync_row_diff_th	8	0x02		
P0:0x87	Debug_mode4	8	0x58		[7] exp_change_retime [5:4] fsync_vb_gap [1:0] fsync_vb_old
P0:0x88	Fsync_row_diff_big[13:8]	6	0x00		[13:8] fsync_row_diff_big
P0:0x89	Fsync_row_diff_big[7:0]	8	0x04		[7:0] fsync_row_diff_big
P0:0x8a	Fsync_row_diff_big2[13:8]	6	0x00		[5:0] Fsync_row_diff_big2
P0:0x8b	Fsync_row_diff_big2[7:0]	8	0x10		

CSI/PHY1.0

Address	Name	Width	Default Value	R/W	Description
P3:0x01	DPHY_analog_mode1	8	0x20	RW	
P3:0x02	DPHY_analog_mode2	8	0x16	RW	
P3:0x03	DPHY_analog_mode3	8	0xca	RW	
P3:0x04	FIFO_prog_full_level[7:0]	8	0x08	RW	[7:0]FIFO_prog_full_level[7:0]
P3:0x05	FIFO_prog_full_level[11:8]	4	0x00	RW	[3:0] FIFO_prog_full_level[11:8]
P3:0x06	FIFO_mode	8	0x00	RW	
P3:0x11	LDI_set	8	0x2b	RW	
P3:0x12	LWC_set[7:0]	8	0x60	RW	
P3:0x13	LWC_set[15:8]	8	0x09	RW	
P3:0x14	SYNC_set	8	0xb8	RW	SYNC_set
P3:0x15	DPHY_mode	8	0x10	RW	
P3:0x16	LP_set	8	0x29	RW	
P3:0x1b	fifo2_prog_full_level	5	0x08	RW	[4:0]fifo2_prog_full_level
P3:0x1c	fifo2_push_prog_full_level	5	0x08	RW	[4:0]fifo2_push_prog_full_level
P3:0x1d	sram_test_mode	4	0x02	RW	[3]RF1_not_split [2]RF1 cen [1]RF1 gate [0]NA sram test
P3:0x20	T_init_set	8	0x80	RW	
P3:0x21	T_LPX_set	8	0x10	RW	
P3:0x22	T_CLK_HS_PREPARE_set	8	0x05	RW	

P3:0x23	T_CLK_zero_set	8	0x20	RW	
P3:0x24	T_CLK_PRE_set	8	0x02	RW	
P3:0x25	T_CLK_POST_set	8	0x20	RW	
P3:0x26	T_CLK_TRAIL_set	8	0x08	RW	
P3:0x27	T_HS_exit_set	8	0x10	RW	
P3:0x28	T_wakeup_set	8	0xa0	RW	
P3:0x29	T_HS_PREPARE_set	8	0x06	RW	
P3:0x2a	T_HS_Zero_set	8	0x0a	RW	
P3:0x2b	T_HS_TRAIL_set	8	0x08	RW	
P3:0x30	MIPI_test	2	0x00	RW	[1:0]MIPI_Test
P3:0x35	OUT_pad_test_data	8	0x00		
P3:0x36	clklp_drv	2	0x00		[1:0]clklp_drv
P3:0x37	lp_drv	4	0x00		[3:2] data1lp_drv [1:0] data0lp_drv
P3:0x38	prbs_mode	8	0x20		
P3:0x39	prbs_LDI	8	0x3d		
P3:0x4a	prbs_seed[7:0]	8	0x9a		
P3:0x4b	prbs_seed[15:8]	8	0x78		
P3:0x4c	MIPI_TSEL	2	0x01		[1:0] MIPI_TSEL
P3:0xaa	o_vsync_pola o_hsync_pola pad_test_valid pad_test_value	8	0x00		[7] o_vsync_pola [6] o_hsync_pola [5:3] pad_test_valid [2:0]pad_test_value

OUT

Address	Name	Width	Default Value	R/W	Description
P1:0x90	Win_mode	1	0x01		
P1:0x91	out_win_y1[10:8]	11	0x00		[7:3]NA [2:0] out_win_y1
P1:0x92	out_win_y1[7:0]	11	0x00		Out_win_y1
P1:0x93	Out_win_x1[11:8]	12	0x00		[7:4]NA [3:0]out_win_x1
P1:0x94	Out_win_x1[7:0]	12	0x00		
P1:0x95	Out_win_height[10:8]	11	0x04		[7:3]NA [2:0] out_win_helght[10:8]
P1:0x96	Out_win_height[7:0]	11	0x38		out_win_helght[7:0]
P1:0x97	Out_win_width[11:8]	12	0x07		[7:4]NA [3:0]out_win_width[11:8]
P1:0x98	Out_win_width[7:0]	12	0x38		Out_win_width[7:0]

					must be 8X when raw10
P1:0x99	Out_win_offset	4	0x05		[7:4]NA [3:0] Out_win_offset for auto_updown[3:2] out_offset_y1=2 for auto_mirror[1:0] out_offset_x1=2

BLK

Address	Name	Width	Default Value	R/W	Description
P1:0x40	BLK_mode1	8	0x23	RW	[7] not smooth [6:4] blk_smooth_speed [3]blk_dd_map [2]dark_sel_map [1]dark_current_en [0]offset_en
P4:0x0c	Ndark_offset_G1[14:8]				
P4:0x09	Ndark_offset_R1[7:0]				
P4:0x0d	Ndark_offset_R1[14:8]				
P4:0x0a	Ndark_offset_B2[7:0]				
P4:0x0e	Ndark_offset_B2[14:8]				
P4:0x0b	Ndark_offset_G2[7:0]				
P4:0x0f	Ndark_offset_G2[14:8]				
P4:0x14	Ndark_ratio_G1	8			1.7
P4:0x15	Ndark_ratio_R1	8			1.7
P4:0x16	Ndark_ratio_B2	8			1.7
P4:0x13	Ndark_ratio_G2	8			1.7

GLOBAL/PRE/POSTGAIN

Address	Name	Width	Default Value	R/W	Description
P0:0xb1	auto_pregain_sync[9:6]	4	0x01	RW	[7:4] NA [3:0] Auto_pregain[9:6] 4.6 精度
P0:0xb2	auto_pregain[5:0]	8	0x00	RW	[7:2] Auto_pregain[5:0] [1:0]NA
P0:0xb3	Analog_PGA_gain[7:0]	8	0x00	RW	
P0:0xb4	Analog_PGA_gain[9:8]	2	0x00	RW	[7:2]NA [1:0] nanlog_pga_gain [9:8]
P0:0xb8	Col_gain[11:6]	8	0x00	RW	[7:6]NA [5:0]col_gain[11:6]
P0:0xb9	Col_gain[5:0]	8	0x00	RW	[7:6]NA [5:0]col_gain[5:0]

DARK OFFSET

Address	Name	Width	Default Value	R/W	Description
P1:0x60	WB_offset	8	0x00	RW	WB_offset