GC1084 CSP

1/4.5’’HD CMOS Image Sensor

Datasheet

V0.0

2021-12-17

Ordering Information

◆ **GC1084-C31YA**

(Colored, 31PIN-csp)

GENERATION REVISION HISTORY

REV.	*EFFECTIVE DATE*	*DESCRIPTION OF CHANGES*	*PREPARED BY*
V0.0	*2021-12-17*	*Document Release*	*AE Dept.*

Galaxycore Incorporation

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Content

1. Sensor Overview

1.1 General Description

GC1084 is a high quality 720P CMOS image sensor, for mobile phone camera applications and digital camera products. GC1084 incorporates a 1280H x 720V pixel array, on-chip 10-bit ADC, and image signal processor.

The full scale integration of high-performance and low-power functions makes the GC1084 best fit the design, reduce implementation process, and extend the battery life of Motion Camera, Car DVR, and a wide variety of mobile applications.

It provides RAW10 and RAW8 data formats with DVP and MIPI interface. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Standard optical format of 1/4.5 inch
- 2.72um*2.72um
- Output formats: Raw Bayer 10bit/8bit
- Power supply requirement: AVDD28: 2.7~2.9V(Typ.2.8V)
  DVDD: 1.7~1.9V(Typ.1.8V)
  IOVDD: 1.7~1.9V(Typ.1.8V)
- PLL support
- DVP@30fps，MIPI@30fps
- Windowing support
- DVP /MIPI (1lane) interface support
- Horizontal/Vertical mirror
- Image processing module
- Package: CSP/PLCC
- Binning 2x2

1.3 Application

- Motion camera
- Car DVR
- Monitoring
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipment
- Security systems
- Industrial and environmental systems

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/4.5inch
Pixel Size	2.72um x2.72um
Active pixel array	1280 x 720
ADC resolution	10 bit ADC
Max Frame rate	30fps@36MHz
Power Supply	AVDD28: 2.7~2.9V(Typ.2.8V) DVDD: 1.7~1.9(Typ.1.8V) IOVDD: 1.7~1.9V(Typ.1.8V)
Power Consumption	98mW @30fps,720p
SNR	38.5dB
Dark Current	TBD
Sensitivity	TBD
Dynamic range	83dB
Operating temperature:	-30~80℃
Stable Image temperature	0~60℃
Optimal lens chief ray angle(CRA)	12°(linear)
Package type	CSP
Input clock frequency	6~27MHz

2. DC Parameters

2.1 Standby Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	10	—	uA
Digital	I_{DVDD}	—	20	—	uA
I/O	I_{IOVDD}	—	20	—	uA

INCK: 27MHz, XSHUTDOWN:H

Typ. Analog: 2.8V, Digital: 1.8V, I/O:1.8V, Tj=25℃

2.2 Power off Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	0	0	uA
Digital	I_{DVDD}	—	0	0	uA
I/O	I_{IOVDD}	—	0	0	uA

Power off, T_j=25℃

2.3 Operation current

Full size Operation Current (Parallel mode)

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	18	—	mA
Digital	I_{DVDD}	—	17	—	mA
I/O	I_{IOVDD}	—	5	—	mA

Frame rate: 30FPS, RAW 10, Input clock: 27MHz

DCLK: 36MHz

Typ. Analog: 2.8V, Digital: 1.8V, I/O:1.8V, T_j=25℃

Full size Operation Current (MIPI mode @312Mbps / Lane)

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	18	—	mA
Digital	I_{DVDD}	—	25	—	mA
I/O	I_{IOVDD}	—	1	—	mA

Frame rate: 30FPS, RAW 10, Input clock: 24MHz

DCLK: 78MHz

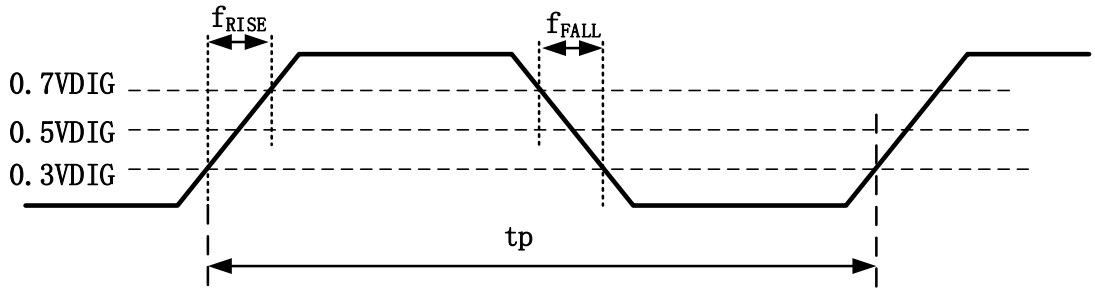
Typ. Analog: 3.3V, Digital: 1.5V, I/O:1.8V, T_j=25℃

2.4 DC Characteristics

Item	Symbol	Min	Typ	Max	Unit
Power supply	**V_{AVDD}**	2.7	2.8	2.9	V
	V_{DVDD}	1.7	1.8	1.9	V
	V_{IOVDD}	1.7	1.8	1.9	V
Digital Input(Conditions: AVDD = 2.8V, DVDD = 1.8V, IOVDD = 1.8V)					
Input voltage HIGH	**V_{IH}**	0.7*VIF			V
Input voltage LOW	**V_{IL}**			0.3*VIF	V
Digital Output(Conditions: AVDD = 2.8V, IOVDD = 1.8V, standard Loading 25PF)					
Output voltage HIGH	**V_{OH}**	0.8*VIF			V
Output voltage LOW	**V_{OL}**			0.2*VIF	V

3. AC Characteristics

Master clock wave diagram

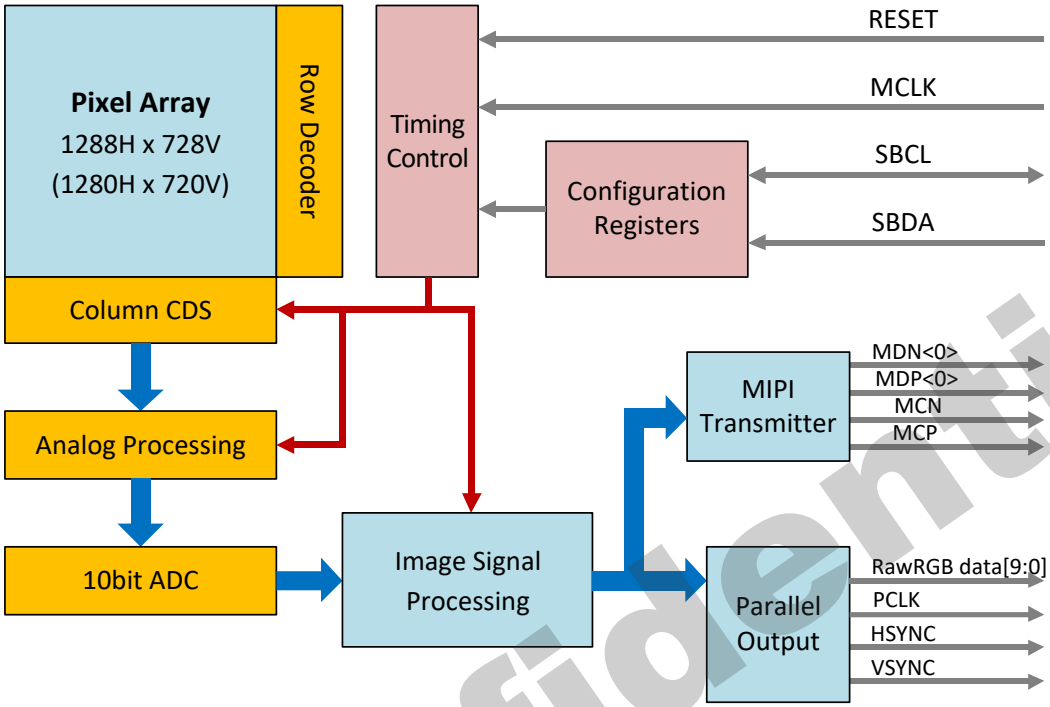


Input clock square waveform specifications：

Item	Symbol	Min	Typ	Max	unit
Frequency	f_{SCK}	6	27	36	MHz
jitter (period, peak-to-peak)	T_{jitter}			600	ps
Rise Time	f_{RISE}	1		15	ns
Fall Time	f_{FALL}	1		15	ns
Duty Cycle	f_{DUTY}	40		60	%
Input Leakage	f_{ILEAK}	-10		10	μA

4. Block Diagram

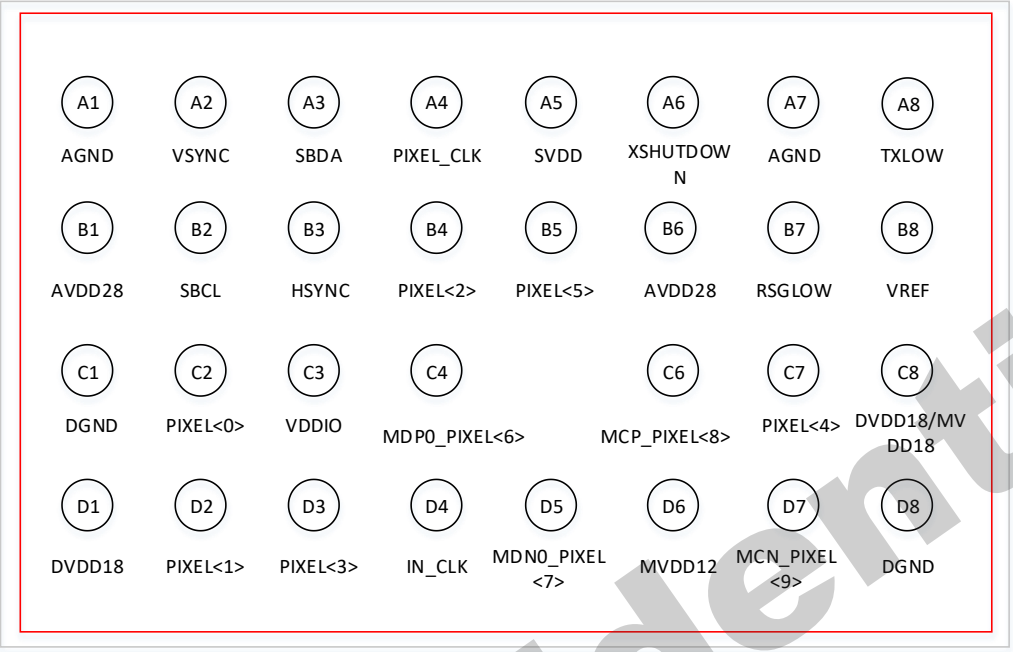
4.1 Block Diagram



GC1084 has an active image array of 1280x720 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 10 bit A/D converter. The digital signals are processed in the ISP Block. Users can easily control these functions via two-wire serial interface bus.

5. CSP Package Specifications

5.1 Pin Diagram (CSP)



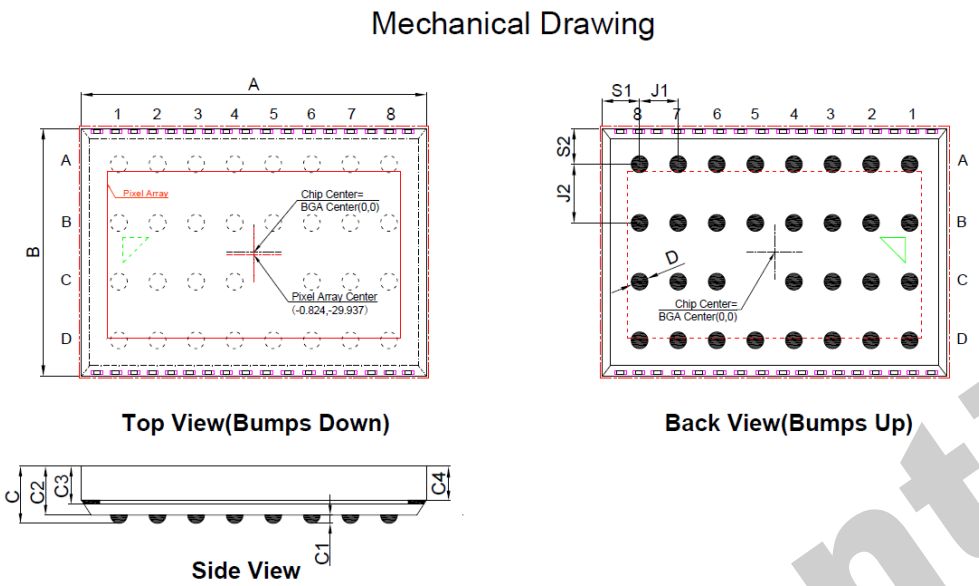
Top View

5.2 Pin Descriptions

Pin	Name	Pin Type	Description
A1	AGND	Ground	Ground for analog
A2	VSYNC	Output	Vertical reference output
A3	SBDA	Input	Two-wire serial bus, data
A4	PCLK	Output	Pixel clock output
A5	SVDD	Power	Digital power supply pin: 1.8V, please connect capacitor to digital ground.
A6	XSHUTDOWN	Input	Chip reset control: 0: chip reset 1: normal work
A7	AGND	Ground	Ground for analog
A8	TXLOW	Power	Internal power supply, please connect capacitor to analog ground.
B1	AVDD28	Power	Main power supply pin: 2.8V, Please connect capacitors to analog ground
B2	SBCL	Input	Two-wire serial bus, clock
B3	HSYNC	Output	Horizontal sync output

B4	PIXEL<2>	Output	Raw RGB Parallel data output bit[2]
B5	PIXEL<5>	Output	Raw RGB Parallel data output bit[5]
B6	AVDD28	Power	Main power supply pin: 2.8V, Please connect capacitors to analog ground
B7	RSGLOW	Power	Internal power supply, please connect capacitor to analog ground.
B8	VREF	Power	Internal power supply, please connect capacitor to analog ground.
C1	DGND	Ground	Ground for digital
C2	PIXEL<0>	Output	Raw RGB Parallel data output bit[0]
C3	VDDIO	Power	Power supply for I/O circuits: 1.8V, Please connect capacitor to digital ground.
C4	MDP0/PIXEL<6>	Output	MIPI: MIPI data<0> (+) DVP: Raw RGB Parallel data output bit[6]
C5	/	/	/
C6	MCP/PIXEL<8>	Output	MIPI: MIPI clock (+) DVP: Raw RGB Parallel data output bit[8]
C7	PIXEL<4>	Output	Raw RGB Parallel data output bit[4]
C8	MVDD18	Power	Digital power supply pin: 1.8V, please connect capacitor to digital ground.
D1	DVDD18	Power	Digital power supply pin: 1.8V, please connect capacitor to digital ground.
D2	PIXEL<1>	Output	Raw RGB Parallel data output bit[1]
D3	PIXEL<3>	Output	Raw RGB Parallel data output bit[3]
D4	IN_CLK	Input	Sensor input clock
D5	MDN0/PIXEL<7>	Output	MIPI: MIPI: MIPI data<0> (-) DVP: Raw RGB Parallel data output bit[7]
D6	MVDD12	Power	Internal power supply, please connect capacitor to digital ground.
D7	MCN/PIXEL<9>	Output	MIPI: MIPI: MIPI clock (-) DVP: Raw RGB Parallel data output bit[9]
D8	DGND	Ground	Ground for digital

5.3 Package Specification (unit: um)

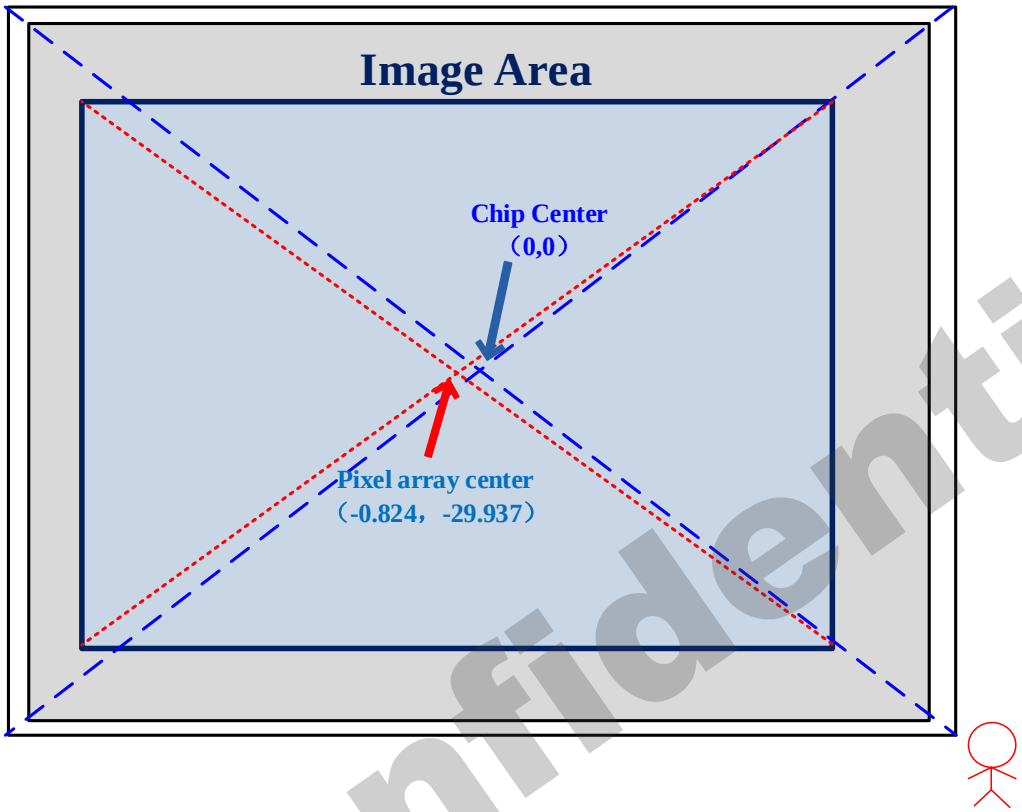


Description	symbol	Nominal	Min	Max
		Millimeters		
Package Body Dimension X	A	4.1100	4.0850	4.1350
Package Body Dimension Y	B	2.9540	2.9290	2.9790
Package Height	C	0.7100	0.6550	0.7650
Ball Height	C1	0.1000	0.0700	0.1300
Package Body Thickness	C2	0.6100	0.5750	0.6450
Thickness from top glass surface to wafer	C3	0.4450	0.4300	0.4600
Glass Thickness	C4	0.4000	0.3900	0.4100
Ball Diameter	D	0.2000	0.1700	0.2300
Total Ball Count	N	31		
Ball Count X axis	N1	8		
Ball Count Y axis	N2	4		

Pins pitch X axis	J1	0.4600	0.4500	0.4700
Pins pitch Y axis	J2	0.7000	0.6900	0.7100
BGA ball center to package center offset in X-direction	X	0.0000	-0.0250	0.0250
BGA ball center to package center offset in Y-direction	Y	0.0000	-0.0250	0.0250
BGA ball center to chip center offset in X-direction	X1	0.0000	-0.0250	0.0250
BGA ball center to chip center offset in Y-direction	Y1	0.0000	-0.0250	0.0250
Edge to Ball Center Distance along X	S1	0.45500	0.4250	0.4850
Edge to Ball Center Distance along Y	S2	0.42700	0.3970	0.4570

6. Optical Specifications

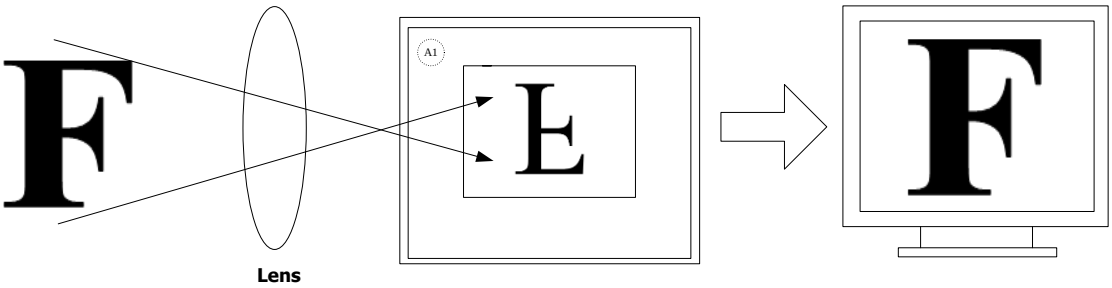
6.1 Optical Center (unit: μm)



Top View

6.2 Readout Position

The GC1084 default status is readout from the lower left corner with pin A1 located in the upper left corner. The proper image output as follow when Pin A1 is located in the upper left corner as the lens inverts image vertically and horizontally.



In addition, this system supports up/down and/or right/left inversion, and is

capable of following outputs. When using the inversion function, the pixel array reads from the sensor changes, but this is processed adaptively within the ISP, so there is no need for users to be aware of it. However, care must be taken in RAW output mode, as the sensor data is output as is.

Readout direction can be set by the registers.

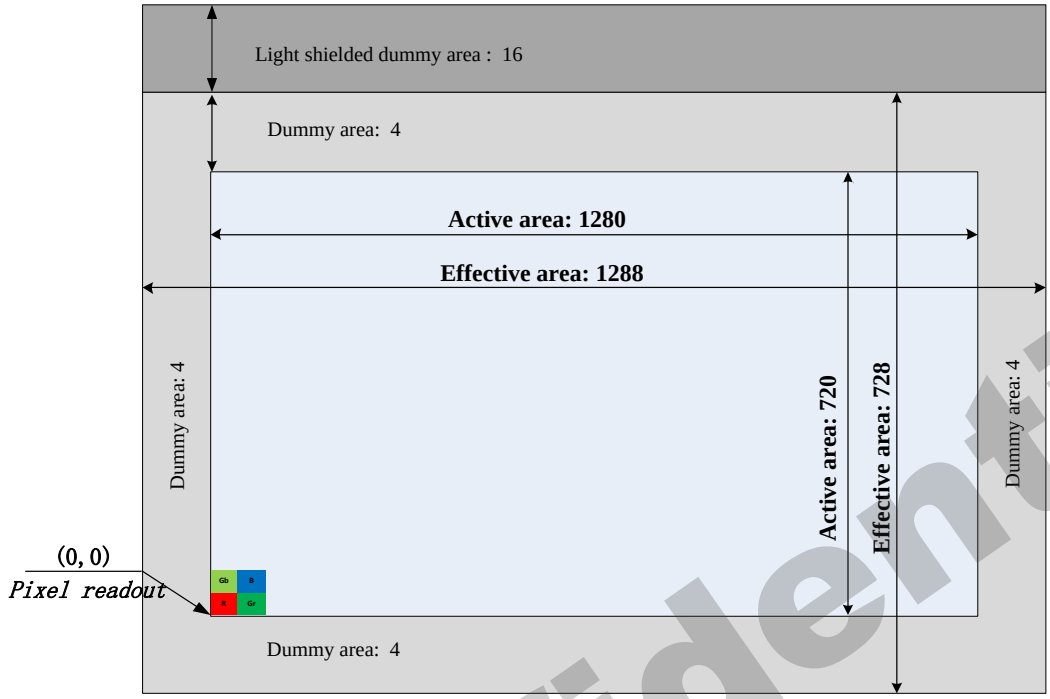
Function	Register Address	Register Value	First Pixel
Normal	0x0015[1:0]&0x0d15[1:0]	00/00	R
Horizontal mirror	0x0015[1:0]&0x0d15[1:0]	01/01	Gr
Vertical Flip	0x0015[1:0]&0x0d15[1:0]	10/10	Gb
Horizontal Mirror and Vertical Flip	0x0015[1:0]&0x0d15[1:0]	11/11	B

Horizontal Mirror

Vertical Flip

Horizontal Mirror and Vertical Flip

6.3 Pixel Array



Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 1279. If flip in column, column is read out from 1279 to 0.

If no flip in row, row is read out from 0 to 719.If flip in row, row is read out from 719 to 0.

6.4 Lens Chief Ray Angle (CRA)

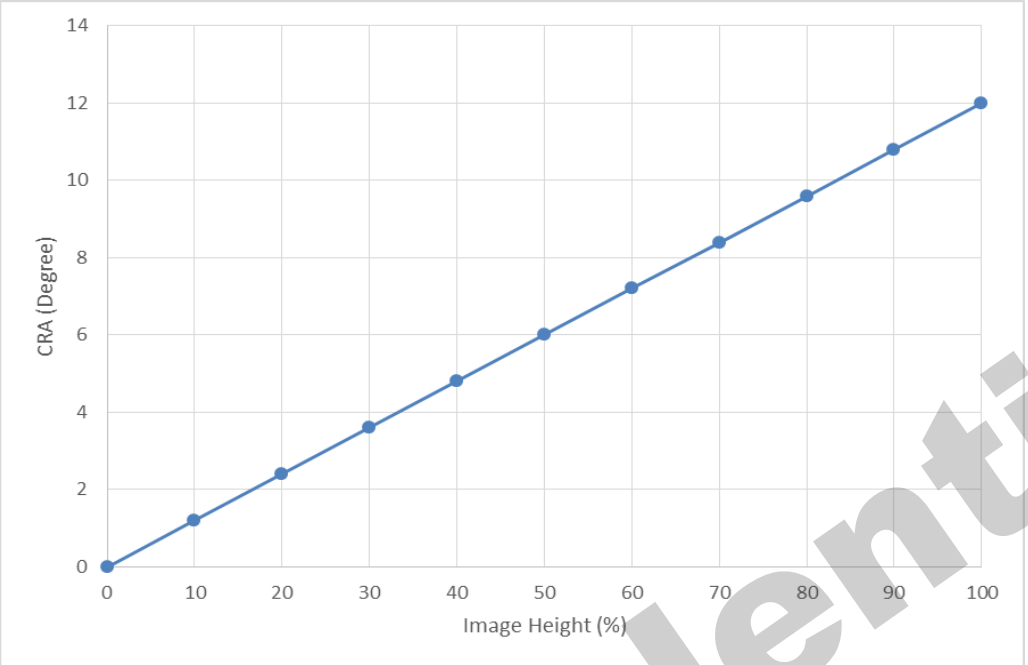
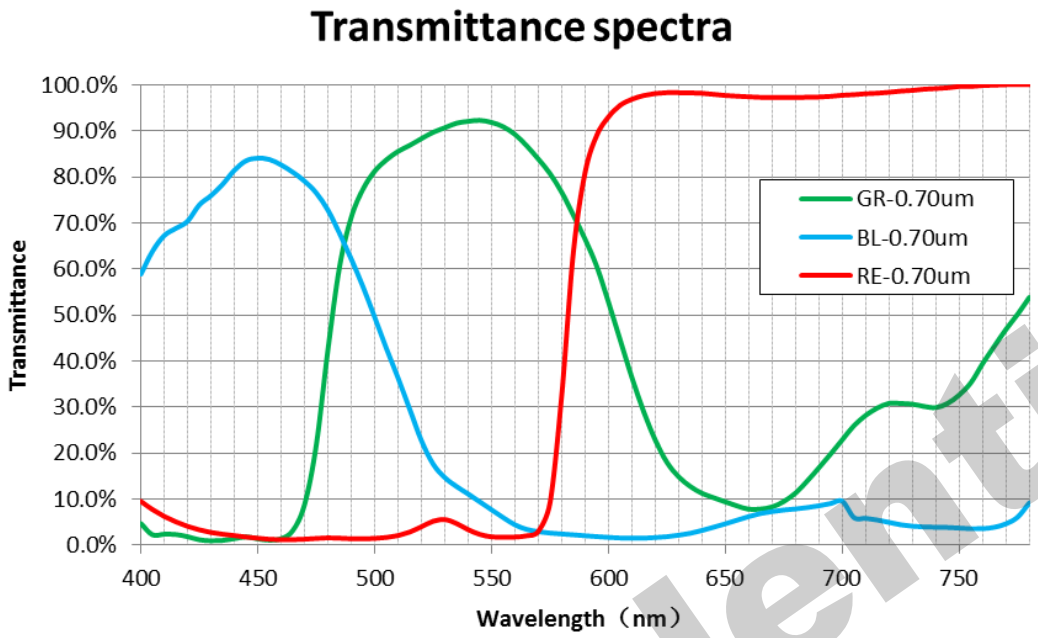


Image Height (%)	Image Height (mm)	CRA (degree)
0	0	0
10	0.2197	1.2
20	0.4394	2.4
30	0.6591	3.6
40	0.8788	4.8
50	1.0985	6
60	1.3182	7.2
70	1.5379	8.4
80	1.7576	9.6
90	1.9773	10.8
100	2.197	12

6.5 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below



7. Two-wire Serial Bus Communication

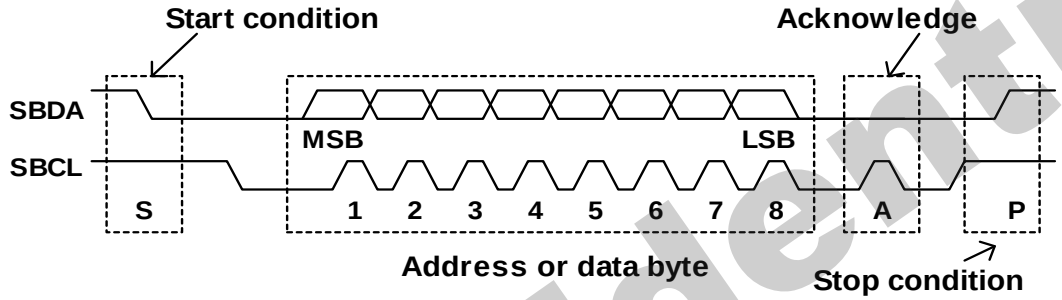
GC1084 Device Address:

Serial bus write address = 0x6e Serial bus read address = 0x6f

7.1 Protocol

The host must perform the role of a communications master and GC1084 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**.



Single Register Writing:

S	6eH	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	6eH	A	Register Address	A	Data(1)	A	……	Data(N)	A	P

Single Register Reading:

S	6eH	A	Register Address	A	S	6fH	A	Data	NA	P

Notes:

From master to slave From slave to master

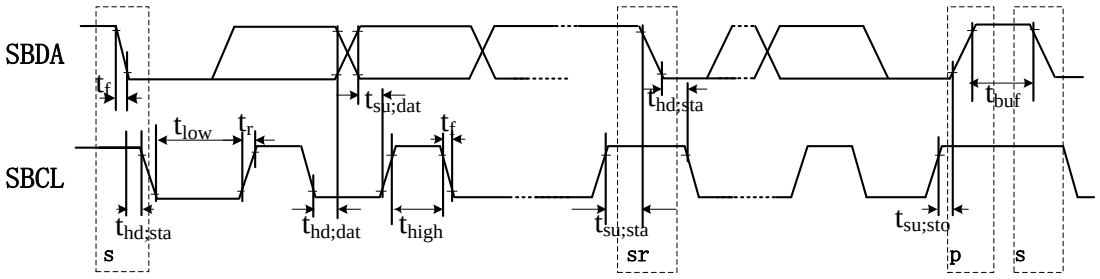
S: Start condition **P:** Stop condition

A: Acknowledge bit **NA:** No acknowledge

Register Address: Sensor register address

Data: Sensor register value

7.2 Serial Bus Timing

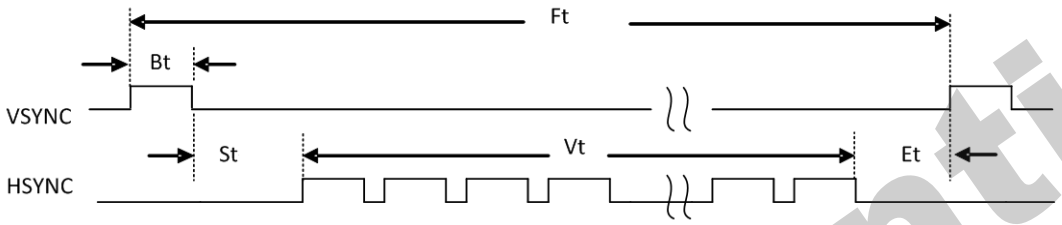


Parameter	Symbol	Min.	Typ.	Max.	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between stop and start condition	t_{buf}	1.3	--	--	μs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for a repeated start	$t_{su;sta}$	0.6	--	--	μs
Data hold time	$t_{hd;dat}$	0	--	0.9	μs
Data Set-up time	$t_{su;dat}$	100	--	--	Ns
Rise time of SBCL, SBDA	t_r	--	--	300	Ns
Fall time of SBCL, SBDA	t_f	--	--	300	Ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	--	Pf

8. Applications

8.1 DVP timing

Suppose Vsync is low active and Hsync is high active, and output format is RAW Bayer 10bit/8bit, then the timing of Vsync and Hsync is bellowing (take capture mode for example, preview mode is the same):



Ft =VB+ Vt +16 (dark line) (unit is row_time)

VB+16 = Bt + St + Et, Vblank/Dummy line, setting by register 0x0d07 and 0x0d08.

Ft -> Frame time, one frame time.

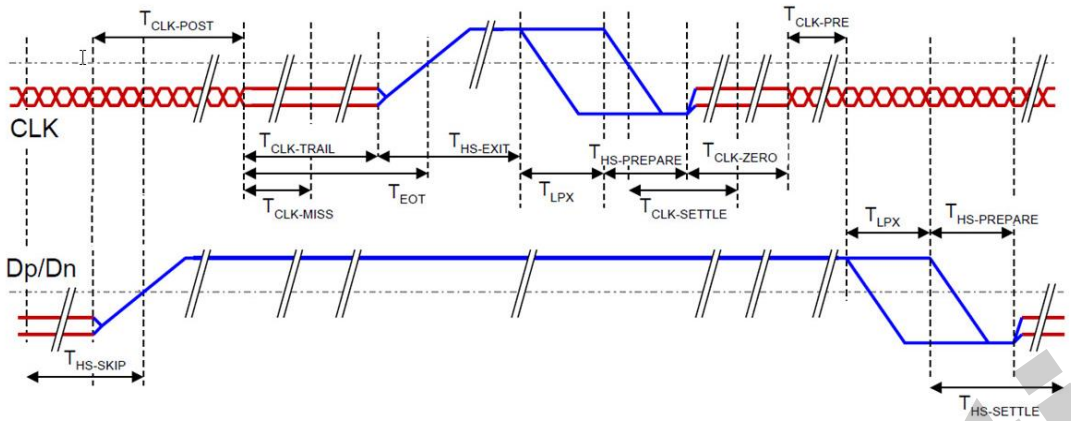
Bt -> Blank time, Vsync no active time.

St -> Start time, setting by register 0x0d13.

Et –> End time, setting by register 0x0d14.

Vt -> valid line time. Vt = win_height, win_height is setting by register 0x0d0d and0x0d0e.

8.2 Clock lane low-power



Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

$T_{CLK\_HS\_PREPARE}$: setting by Register : 0x0222

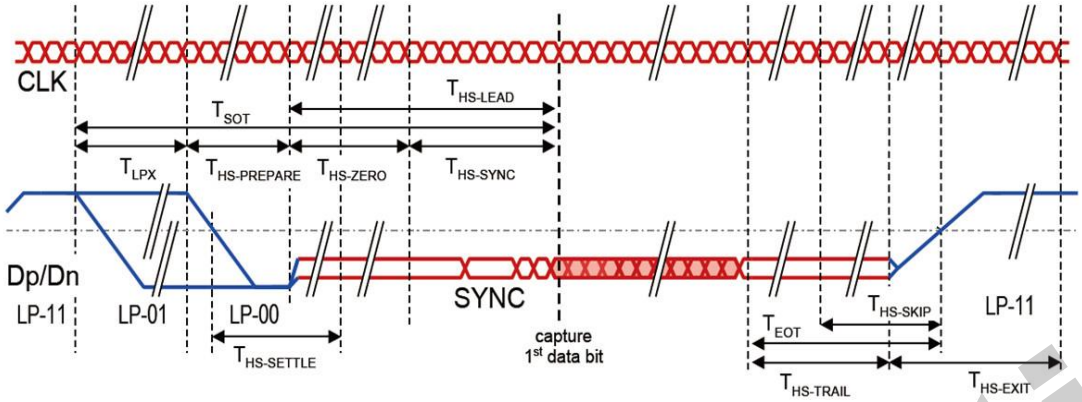
T_{CLK_ZERO}: setting by Register : 0x0223

T_{CLK_PRE}: setting by Register : 0x0224

T_{CLK_POST}: setting by Register : 0x0225

T_{CLK_TRAIL}: setting by Register : 0x0226

8.3 Data Burst



Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

T_{LPX}: setting by Register : 0x0221

$T_{HS\_PREPARE}$: setting by Register : 0x0229

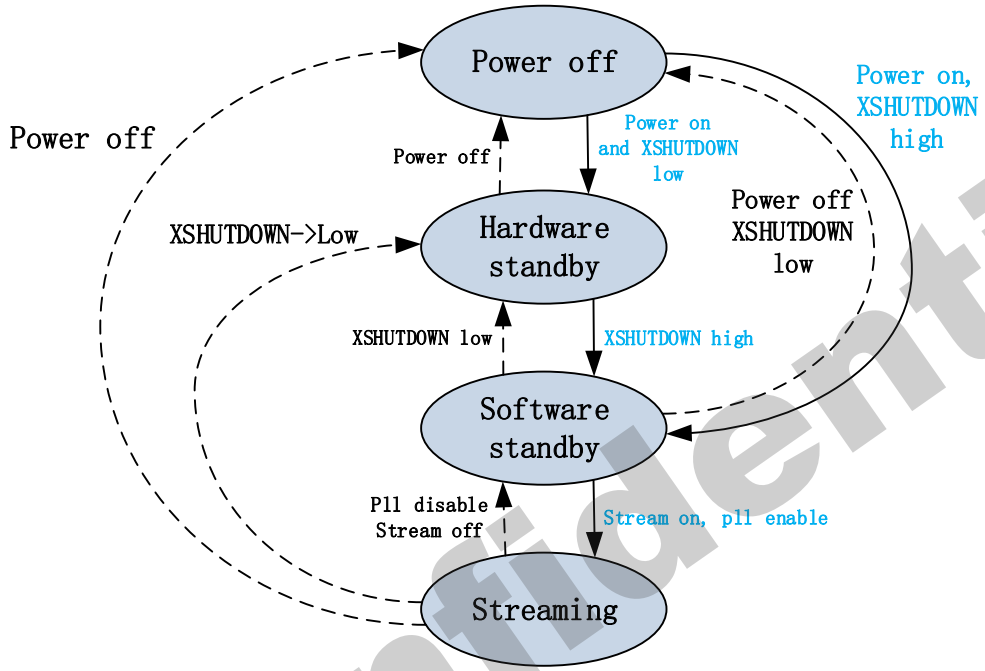
T_{HS_ZERO}: setting by Register : 0x022a

T_{HS_TRAIL}: setting by Register : 0x022b

T_{HS_EXIT}: setting by Register : 0x0227

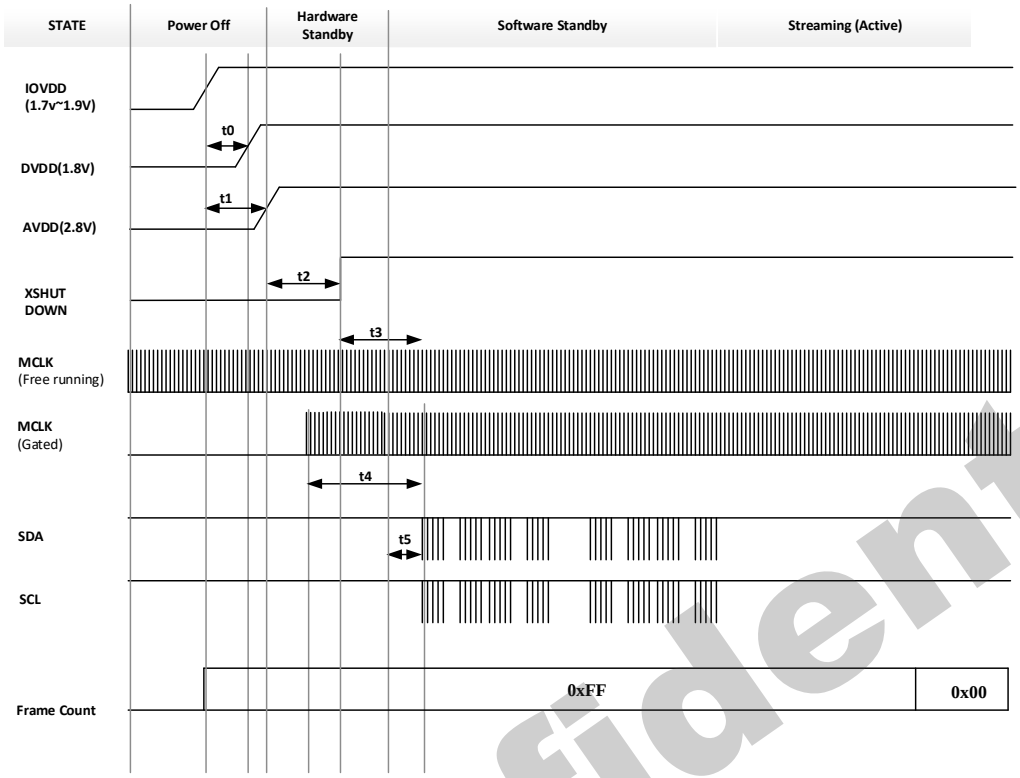
9. Power On/Off Sequence

9.1 Operation mode



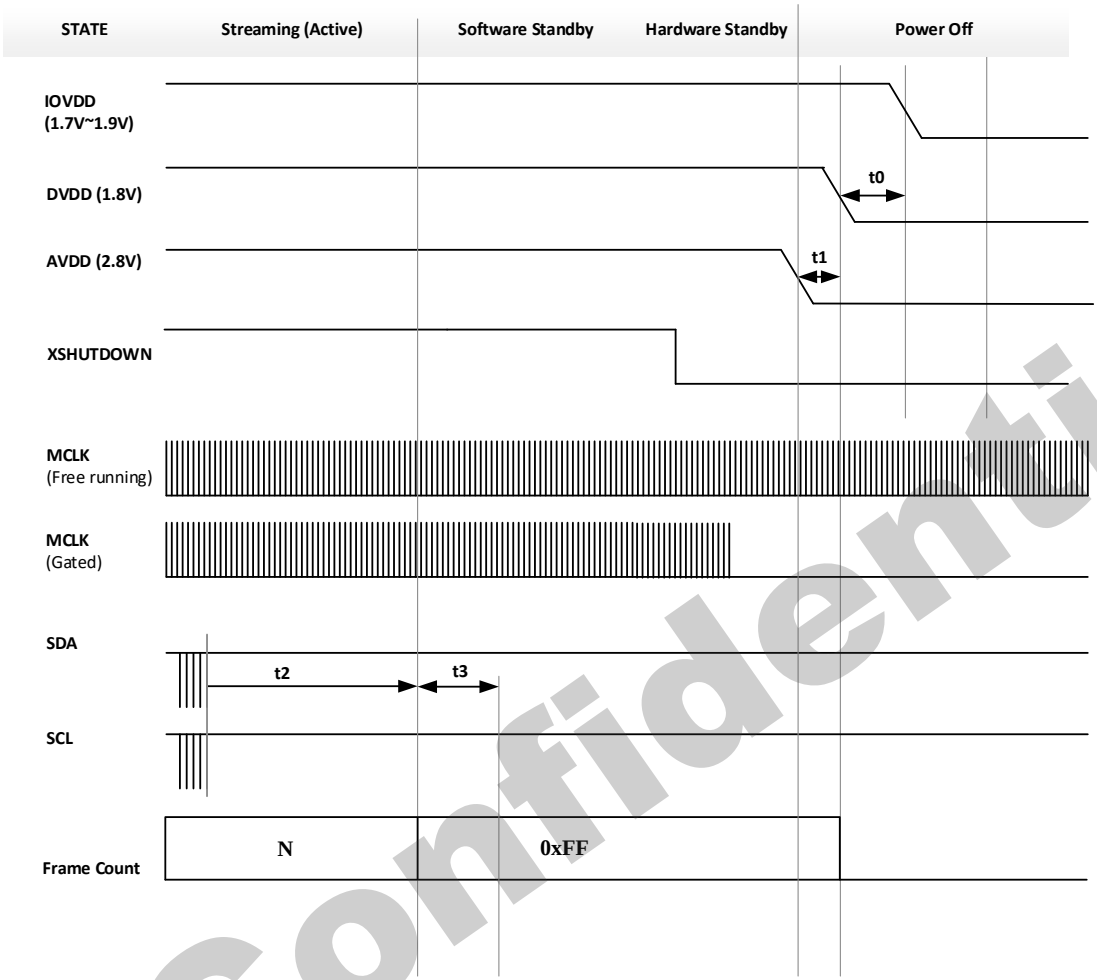
Power state	Description	Activate
Power off	Power supplies are turned off	None
Hardware standby	No communication with sensor, low level on XSHUTDOWN, and stop MCLK	XSHUTDOWN high
Software standby	Two- wire serial communication with sensor, pll is ready for fast return to streaming mode	Stream mode off PLL disable XSHUTDOWN high
Streaming	Sensor is fully powered and is streaming image data on the MIPI CSI-2 bus	All

9.2 Power on Sequence



Parameter	Description	Min.	Max.	Unit
t0	From IOVDD to DVDD18	50	-	μs
t1	From IOVDD to AVDD28	50	-	μs
t2	From AVDD28 to XSHUTDOWN pull high	0	-	μs
t3	XSHUTDOWN rising to first I2C transaction	50	-	μs
t4	Minimum No. of MCLK cycles prior to the first I2C transaction	1200	-	MCLK
t5	From XSHUTDOWN rising to first I2C transaction	50	-	μs

9.3 Power off Sequence



Parameter	Description	Min.	Max.	Unit
t0	From DVDD12 pull down to IOVDD pull down	0	-	μs
t1	From AVDD28 pull down to DVDD12 pull down	0	-	μs
t2	Enter Software Standby CCI command – Device in Software Standby mode	0	-	μs
t3	Minimum number of MCLK cycles after the last CCI transaction or MIPI frame end code.	2000		MCLK

- If the sensor's power cannot be cut off, please keep power supply, then set PWDN pin low. It will make sensor standby
- Register should be reloaded before works.
- If the standby sequence needs to be modified, please contact FAE of *Galaxycore Inc.*

9.4 Black level calibration

Black level is caused by pixel characteristics and analog channel offset, which makes poor image quality in dark condition and color balance, to reduce these, sensor automatically calibrates the black level every frame with light shield pixel array.

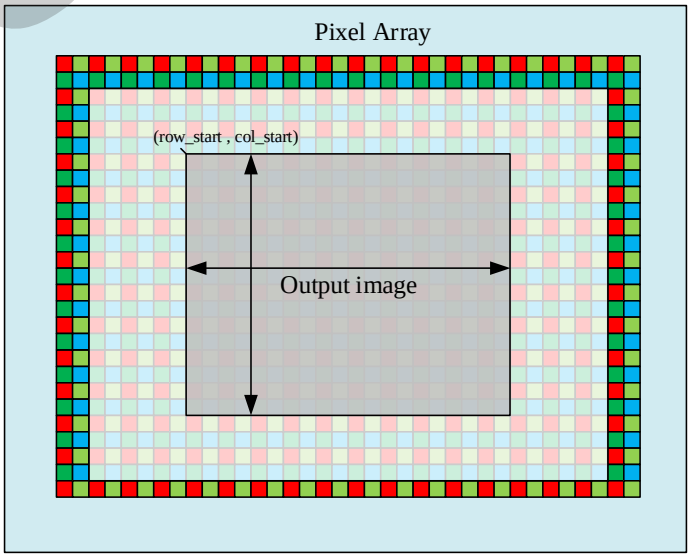
9.5 Integration time

The integration time is controlled by the integration time registers

Addr.	Register name	Description
0x0d03	Shutter time	[5:0] shutter time[13:8]
0x0d04		[7:0] shutter time[7:0]
0x0d41	Frame length	[5:0] frame length[13:8]
0x0d42		[7:0] frame length[7:0]

9.6 Windowing

GC1084 has a rectangular pixel array 1280 x 720, it can be windowed by output size control, the output image windowing can be used to adjust output size, and it will affect field angle.



Addr.	Register name	Description
0x0d0d	win_height	[1:0]win_height[9:8]
0x0d0e		[7:0]win_height[7:0]
0x000f	win_width	[2:0]win_width[10:8]
0x0010		[7:0]win_width[7:0]
0x0d09	Row start	[1:0]row_start[9:8]
0x0d0a		[7:0]row_start [7:0]
0x000b	Col start	[2:0]col_start[10:8]
0x000c		[7:0]col_start[7:0]

9.7 Frame structure

Frame structure is controlled by HB, frame length, window start, window height, window width and VB.

Frame length control

Frame length are controlled by window height, minimum VB and shutter time.

- Frame length depend shutter time.
- Minimum frame length = window height + 16 +VB (VB_min = 16)
- If shutter time < minimum frame length:

  Actual frame length = minimum frame length
- If shutter time > minimum frame length:

  Actual frame length = shutter time + 16 (recommended).

- Fix frame rate
- User can fix VB to fix frame rate.

Line length control

Line length = 1200 (not recommended to be modified)

Addr.	Register name	Description	
0x0d05	Line length	[3:0] Line length[11:8]	X2
0x0d06		[7:0] Line length[7:0]	X2

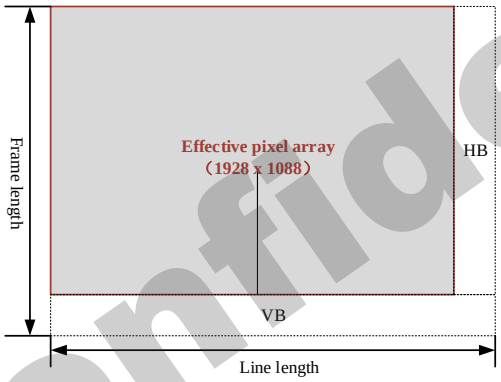
Output window array control

Addr.	Register name	Description

0x0191	Out_window_y1	[2:0] Out_window_y1[10:8]
0x0192		[7:0] Out_window_y1[7:0]
0x0193	Out_window_x1	[3:0] Out_window_x1[11:8]
0x0194		[7:0] Out_window_x1[7:0]
0x0195	Out window height	[2:0] Out window height[10:8]
0x0196		[7:0] Out window height[7:0]
0x0197	Out window width	[3:0] Out window width[11:8]
0x0198		[7:0] Out window width[7:0]

Blank time control

1. line blank time is controlled by HB
2. frame blank time
   - frame blank time = frame length lines – window height – 16



10. Register List

System Register

Address	Name	Width	Default Value	R/W	Description
0x03f0	Sensor_ID_HIGH	8	0x10	RO	Sensor_ID
0x03f1	Sensor_ID_LOW	8	0x84	RO	Sensor_ID
0x03fe	Page select	8	0x00	RW	[7] soft_rst [6]cm_rst [5]mipi_rst [4]cisctl_rst [3]spi_rst

Analog & CISCTL

Address	Name	Width	Default Value	R/W	Description
0x0d03	Exposure time[13:8]	6	0x00	RW	[5:0] exposure time[13:8]
0x0d04	Exposure time[7:0]	8	0x10	RW	[7:0] exposure time[7:0]
0x0d05	CISCTL_HB[13:8]	6	0x04	RW	[5:0]CISCTL_HB[13:8]
0x0d06	CISCTL_HB[7:0]	8	0x80	RW	[7:0]CISCTL_HB[7:0]
0x0d07	CISCTL_vb[13:8]	6	0x00	RW	[5:0] CISCTL_vb[13:8]
0x0d08	CISCTL_vb[7:0]	8	0x20	RW	[7:0] CISCTL_vb[7:0]
0x0d09	CISCTL_row_start[10:8]	2	0x00	RW	[2:0]CISCTL_capt_row_start[10:8]
0x0d0a	CISCTL_row_start[7:0]	8	0x02	RW	[7:0]CISCTL_capt_row_start[7:0]
0x000b	CISCTL_col_start [10:8]	3	0x00	RW	[2:0]CISCTL_capt_col_start[10:8]
0x000c	CISCTL_col_start [7:0]	8	0x00	RW	[7:0]CISCTL_capt_col_start[7:0]
0x0d0d	CISCTL_win_height[10:8]	3	0x02	RW	[2:0]CISCTL_capt_win_height[10:8]
0x0d0e	CISCTL_win_height [7:0]	8	0xd0	RW	[7:0]CISCTL_capt_win_height[7:0]
0x000f	CISCTL_win_width [10:8]	3	0x05	RW	[2:0]CISCTL_capt_win_width[10:8]
0x0010	CISCTL_win_width [7:0]	8	0x0c	RW	[7:0]CISCTL_capt_win_width[7:0]

0x0d41	buf_frame_length_high[13:8]	6	0x04	RW	[5:0] frame_length_high[13:8]
0x0d42	buf_frame_length_low[7:0]	8	0xe0	RW	[7:0] frame_length_low[7:0]

CSI/PHY1.0

Address	Name	Width	Default Value	R/W	Description
0x0201	DPHY_analog_mode1	8	0x20	RW	[7] disable_set[1] [6:5] clkctr [4] NA [3] disable_set[0] [2] phy-lane1_en [1] phy_lane0_en [0] phy_clk_en;
0x0202	DPHY_analog_mode2	8	0x16	RW	[7:6]data1ctr [5:4] data0ctr [3:0]mipi_diff
0x0203	DPHY_analog_mode3	8	0xca	RW	[7] clklane_p2s_sel [6:5] data0hs_ph [4] data0delay1s [3] clkdelay1s [2] mipi_en [1:0] clkhs_ph
0x0204	fifo_prog_full_level[7:0]	8	0x08	RW	[7:0] fifo_prog_full_level1
0x0206	fifo_mode	8	0x00	RW	[7] NA [6] RF2 32X32 cen [5] mipi write gate mode [4]fifo_rst_mode [3]bit10_swicth [2]NA [1] write fifo gate mode [0] read fifo gate mode
0x0208	lpldo_mode	6	0x1d	RW	[5] lpldo_refsel [4] lpldo_en [3:1] lpldo_r [0] lpldo_loaden

0x0211	LDI_set	8	0x2b	RW	[7:0] LDI_set [7:6] vc_id [5:4]data type raw10/8
0x0212	LWC_set[15:8]	8	0x06	RW	[7:0] LWC_set_1
0x0213	LWC_set[7:0]	8	0x40	RW	[7:0] LWC_set_2
0x0214	SYNC_set	8	0xb8	RW	[7:0] SYNC_set
0x0215	DPHY_mode	8	0x10	RW	[7]NA [6]mipi para invar when div2 [5]DATA lane gate [4]all_lane_open_mode [3:2]switch_msb_mode [1:0] clklane_mode
0x0216	LP_set	8	0x29	RW	[7:6] hi-z [5:4]use define
0x021b	fifo2_prog_full_level	5	0x08	RW	[7:5]reserved [4:0] fifo2_prog_full_level
0x021c	fifo2_push_prog_full_level	5	0x08	RW	[7:5]reserved [4:0] fifo2_push_prog_full_level
0x021d	sram_test_mode	4	0x02	RW	[3:0]sram_test_mode
0x0220	T_init_set	8	0x80	RW	[7:0] T_init_set more than 100 us
0x0221	T_LPX_set	8	0x10	RW	[7:0] T_LPX_set more than 50ns
0x0222	T_CLK_HS_PREPARE_set	8	0x05	RW	[7:0] T_CLK_HS_PREPARE_set 38ns ~95nsLP00
0x0223	T_CLK_zero_set	8	0x20	RW	[7:0] T_CLK_zero_set more than 300ns
0x0224	T_CLK_PRE_set	8	0x02	RW	[7:0] T_CLK_PRE_set more than 8UI
0x0225	T_CLK_POST_set	8	0x20	RW	[7:0] T_CLK_POST_set 60ns +52UI
0x0226	T_CLK_TRAIL_set	8	0x08	RW	[7:0] T_CLK_TRAIL_set 60ns
0x0227	T_HS_exit_set	8	0x10	RW	[7:0] T_HS_exit_set more than 100ns
0x0228	T_wakeup_set	8	0xa0	RW	[7:0] T_wakeup_set 1 ms
0x0229	T_HS_PREPARE_set	8	0x06	RW	[7:0] T_HS_PREPARE_set 45+4UI ~85+5UI
0x022a	T_HS_Zero_set	8	0x0a	RW	[7:0] T_HS_Zero_set 140ns
0x022b	T_HS_TRAIL_set	8	0x08	RW	[7:0] T_HS_TRAIL_set /60ns
0x0230	MIPI_Test	2	0x00	RW	[1:0] MIPI_Test
0x0235	OUT_pad_test_data	8	0x00	RW	[7:0] OUT_pad_test_data
0x0236	clklp_drv	2	0x00	RW	[1:0] clklp_drv
0x0237	lp_drv	4	0x00	RW	[3:2] data1lp_drv [1:0] data0lp_drv

0x0238	prbs_mode	8	0x20	RW	[7]NA [6]prbs11 [5]prbs_9 [4]clane prbs en [3]dlane3 prbs en [2]dlane2 prbs en [1]dlane1 prbs en [0]dlane0 prbs en
0x0239	prbs_LDI	8	0x3d	RW	[7:0] prbs_LDI
0x023a	CSI2_update_mode	1	0x00	RE	
0x023e	CSI2_mode	8	0x48	RW	[7] lane_ena [6] DVPBUF_ena [5] ULPEna [4] MIPI_ena [3]mipi_set_auto_enable [2]RAW8_mode [1] line_sync_mode [0] double_lane_en
0x023f	fifo_error_valid	4	0x00	R	[3] fifo1_error_valid [2] fifo1_full_valid [1] fifo_pop_error_valid [0] fifo_push_error_valid
0x0240	mbist_done				
0x024a	prbs_seed[8]	1	0x00	RW	[8] prbs_seed
0x024b	prbs_seed[7:0]	8	0xff	RW	[7:0] prbs_seed
0x024c	MIPI_TSEL	2	0x01	RW	[1:0] MIPI_TSEL
0x0250	frame_counter[15:8]	8		RE	
0x0251	frame_counter[7:0]	8		RE	
0x0252	frame_clr	1	0x00	RE	
0x0290	dvp_out_mode	6	0x00	RW	[5] OUT_gate_mode [4] hsync_delay_half_pclk [3] data_delay_half_pclk [2] vsync_polarity [1] hsync_polarity [0] pclk_out_polarity
0x0291	pad_test_valid[11:8]	4	0x00	RW	
0x0292	pad_test_valid[7:0]	8	0x00	RW	
0x0293	pad_test_data[11:8]	4	0x00	RW	
0x0294	pad_test_data[7:0]	8	0x00	RW	

OUT

Address	Name	Width	Default Value	R/W	Description
0x018c	Color bar	8	0x10	RW	[2]input test image
0x0191	out_win_y1[10:8]	3	0x00	RW	out_win_y1[10:8]
0x0192	out_win_y1[7:0]	8	0x00	RW	out_win_y1[7:0]
0x0193	out_win_x1[11:8]	4	0x00	RW	out_win_x1[11:8]
0x0194	out_win_x1[7:0]	8	0x00	RW	out_win_x1[7:0]
0x0195	out_win_height[10:8]	3	0x02	RW	out_win_height[10:8]
0x0196	out_win_height[7:0]	8	0xd0	RW	out_win_height[7:0]
0x0197	out_win_width[11:8]	4	0x05	RW	out_win_width[11:8] must be 8X when raw10
0x0198	out_win_width[7:0]	8	0x00	RW	out_win_width[7:0]
0x0199	out_win_offset[3:0]	4	0x05	RW	out_win_offset[3:0] for auto_updown[3:2] out_offset_y1=2 ; for auto_mirror[1:0]out_offset_x1=2

GLOBAL/PRE/Channel GAIN

Address	Name	Width	Default Value	R/W	Description
0x007a	global_gain	8	0x40	RW	
0x00b1	buf_auto_pregain[9:6]	4	0x01	RW	[3:0]auto_pregain[9:6]
0x00b2	buf_auto_pregain [5:0]	6	0x00	RW	[7:2]buf_auto_pregain [5:0] 4.6 精度
0x00b8	buf_col_gain[11:6]	6	0x01	RW	[5:0] buf_col_gain[11:6]
0x00b9	buf_col_gain [5:0]	6	0x00	RW	[5:0] buf_col_gain[5:0] 6.6 精度
0x00d0	buf_ANALOG_PGA_gain[7:0]	8	0x00	RW	[13:5] isel [2:0] rsel_dac
0x00d1	buf_ANALOG_PGA_gain[15:8]	8	0x00	RW	
0x0dc1	again	1	0x00	RW	[0] Again
0x0418	channel_gain_L_G1	8	0x00	RW	channel_gain_L_G1
0x0419	channel_gain_L_ R1	8	0x00	RW	channel_gain_L_ R1
0x041a	channel_gain_L_B1	8	0x00	RW	channel_gain_L_B1
0x041b	channel_gain_L_G2	8	0x00	RW	channel_gain_L_G2
0x041c	channel_gain_H_G1	8	0x04	RW	channel_gain_H_G1
0x041d	channel_gain_H_R1	8	0x04	RW	channel_gain_H_R1

0x041e	channel_gain_H_B1	8	0x04	RW	channel_gain_H_B1
0x041f	channel_gain_H_G2	8	0x04	RW	channel_gain_H_G2

DARK OFFSET

Address	Name	Width	Default Value	R/W	Description
0x0170	WB_Gr_offset[7:0]	8	0x40	RW	
0x0171	WB_R_offset [7:0]	8	0x40	RW	
0x0172	WB_B_offset [7:0]	8	0x40	RW	
0x0173	WB_Gb_offset [7:0]	8	0x40	RW	