GC1029 CSP

1/9’’ 1Mega CMOS Image Sensor

Datasheet

V0.0

2022-07-21

Ordering Information

◆ **GC1029**

(Colored, 19PIN-CSP)

GENERATION REVISION HISTORY

Version.	Effective Date	Description of Changes	Prepared by
V0.0	2022-07-21	Initial Release	DSC-AE Dept.

Galaxycore Incorporation

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Content

Figure Content

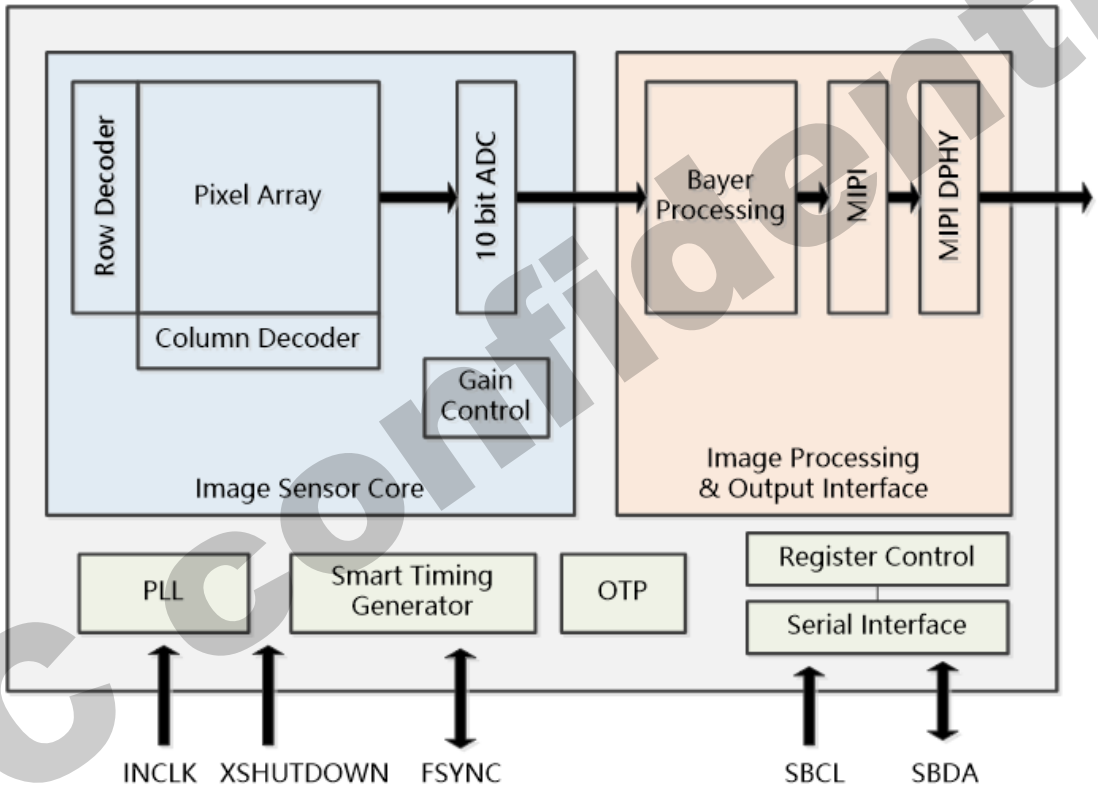
Table content

1. Sensor Overview

1.1 General Description

GC1029 is a high quality 1Mega CMOS image sensor, for notebook camera digital camera and mobile phone camera applications. GC1029 incorporates a 1280H x 720V active pixel array, on-chip 10-bit ADC, and image signal processor. It is programmable through a simple two-wire serial interface and has very low power consumption. It provides RAW10 and RAW8 data formats with MIPI interface.

Figure 1: Block Diagram



1.2 Features

- Optical size: 1/9 inch
- Pixel size: 1.4μm x 1.4μm BSI
- Active image size: 1280 x 720
- Color Filter: RGB Bayer
- Output formats: Raw Bayer 10bit / 8bit
- Power supply requirement: AVDD28: 2.7~2.9V (Typ. 2.8V)
  DVDD: 1.1~1.3V (Typ. 1.2V)
  IOVDD: 1.7~1.9V (Typ. 1.8V)
- Power Consumption: TBD
- Max Frame rate: 60fps@Full Size
- PLL support
- Frame sync support (master/slave)
- Windowing support
- Mirror and Flip support
- Binning Mode support
- OTP support
- Analog Gain: 16X(Max)
- Sensitivity: TBD
- Dynamic range: TBD
- MAX SNR: TBD
- Dark Current: TBD
- Micro lens chief ray angle (CRA): 32.1°(non-linear)
- Operation Temperature: -30~85℃
- Stable Image temperature: -20~60℃
- Storage temperature: -40~125℃
- Package: CSP

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

Description	Symbol	Rating	Unit	Note
Analogue absolute max	V_{AVDD_MAX}	-0.3~3.9	V	Refer to GND
Digital absolute voltages	V_{DVDD_MAX}	-0.3~1.8	V	
IO absolute max	V_{IOVDD_MAX}	-0.3~3.6	V	
Digital input voltages	V_{IF_MAX}	-0.3~V_{IOVDD}+0.3	V	

Note: Digital input voltage: XCLK, SBCL, SBDA, XSHUTDOWN, FSYNC

2.2 Operation Conditions

Table 2: Operation Conditions

Description	Symbol	Min.	Typical	Max.	Unit
Analog power supply	V_{AVDD}	2.7	2.8	2.9	V
Digital power supply	V_{DVDD}	1.1	1.2	1.3	V
IO power supply	V_{IOVDD}	1.7	1.8	1.9	V
Digital input voltages	V_{IF}	0		IOVDD	V
Test temperature	T_{TEST}	21	25	27	℃

Note: 1. Digital input voltage: XCLK, SBCL, SBDA, XSHUTDOWN, FSYNC.
2. Test temperature: image quality test condition.

2.3 DC Characteristics

Table 3: DC Characteristics

Characteristics	Symbol	Min.	Typical	max	Unit
Input voltage HIGH	V_{IH}	0.7 x V_{IF}	-	-	V
Input voltage Low	V_{IL}	-	-	0.3 x V_{IF}	V
Output voltage HIGH	V_{OH}	0.7 x V_{IOVDD}	-	-	V
Output voltage LOW	V_{OL}	-	-	0.3 x V_{IOVDD}	V

Note: Input voltage apply to XCLK, SBCL, SBDA, XSHUTDOWN, FSYNC.

2.4 AC Characteristics

Figure 2: AC Characteristics

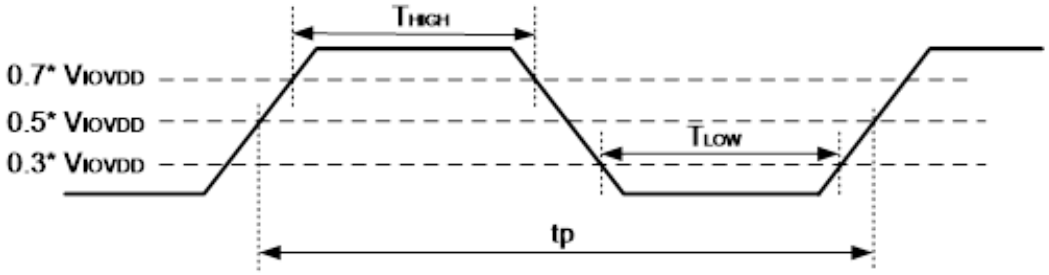


Table 4: AC Characteristics

Item	Symbol	Min.	Typ.	max	unit
Frequency	f_{SCK}	6	24	36	MHz
jitter (period, peak-to-peak)	T_{jitter}			600	ps
High level width	T_{HIGH}	0.4tp		0.6tp	ns
Low level width	T_{LOW}	0.4tp		0.6tp	ns
Duty Cycle	f_{DUTY}	40		60	%

2.5 Power Consumption

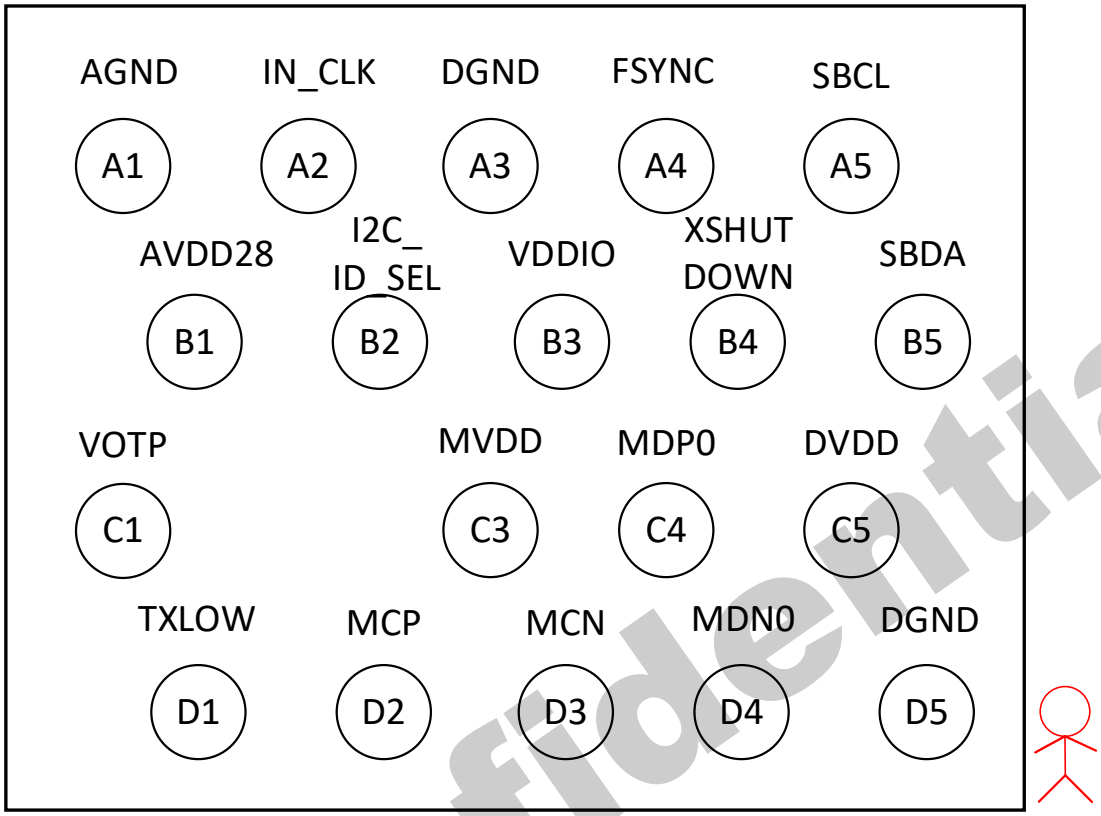
Table 5: Power Consumption

Item	Symbol	Min	Typ	Max	Unit
Full size @30fps MIPI 2lane	I_{AVDD}	-	TBD	-	mA
	I_{DVDD}		TBD		mA
	I_{IOVDD}	-	TBD	-	mA
Full size @60fps MIPI 2lane	I_{AVDD}	-	TBD	-	mA
	I_{DVDD}		TBD		mA
	I_{IOVDD}	-	TBD	-	mA
Standby current	I_{AVDD}	-	TBD	-	μA
	I_{DVDD}		TBD		μA
	I_{IOVDD}	-	TBD	-	μA
Power off current	I_{total}	-	-	TBD	μA

Note: 1. All operate current are measured at 24MHz XCLK.
2. Standby current is measured at XSHUTDOWN = L, XCLK=24MHz.
3. We recommend that power should be turned off, when lower power consumption is required.

3. CSP Package Specifications

Figure 3: CSP Pin Top View



3.1 Pin Descriptions

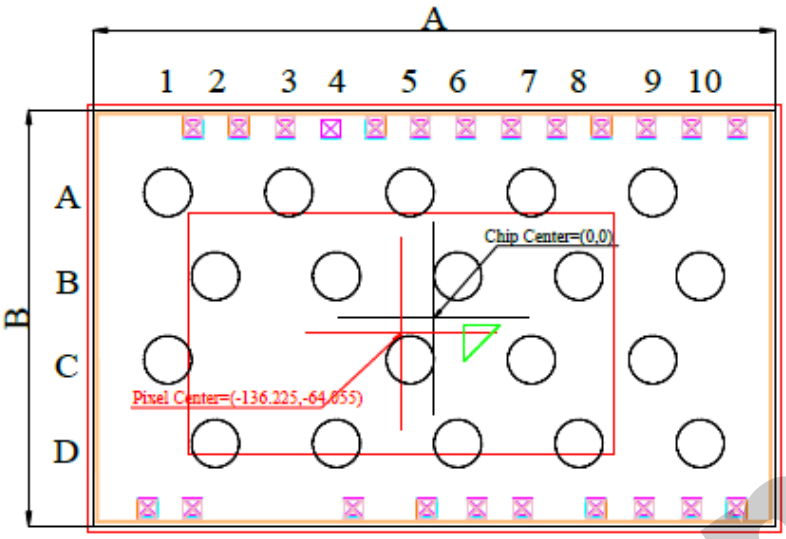
Table 6: Pin Descriptions

Pin	Name	Type	A/D	Description
A1	AGND	Ground	A	Ground for analog
A2	IN_CLK	Input	D	Sensor input clock
A3	DGND	Ground	D	Ground for digital
A4	FSYNC	I/O	D	Frame sync control
A5	SBCL	Input	D	Two-wire serial bus, clock.
B1	AVDD28	Power	A	Analog power supply: 2.8V
B2	I2C_ID_SEL	Input	D	ID_SEL (floating forbidden). 0:0x6e, 1:0x20
B3	VDDIO	Power	D	I/O Power supply: 1.8V
B4	XSHUTDOWN	Input	D	Sensor power down control: (Floating forbidden) 0: reset & standby; 1: normal work
B5	SBDA	I/O	D	Two-wire serial bus, data.
C1	VOTP	Power	D	OTP power supply: 6.5V (floating available)
C2	/	/	/	/

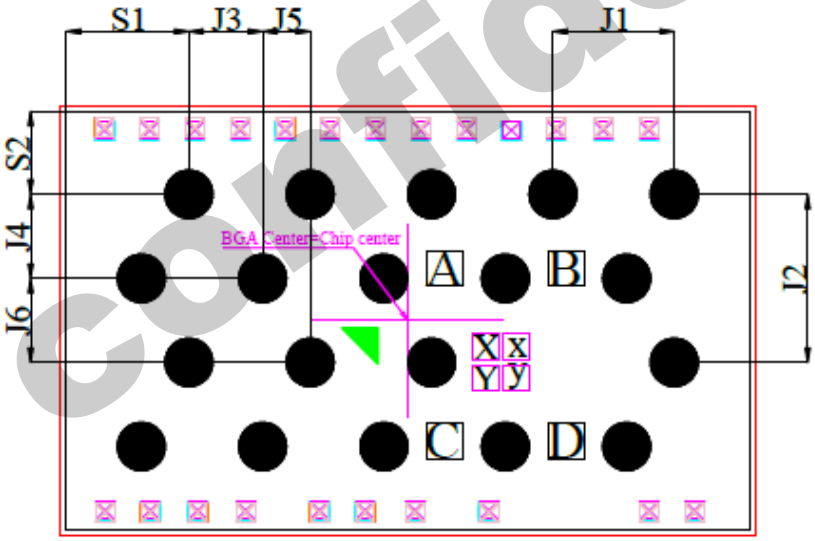
Pin	Name	Type	A/D	Description
C3	MVDD	Power	D	Digital power supply: 1.2V
C4	MDP0	Output	D	MIPI data <0> (+)
C5	DVDD	Power	D	Digital power supply: 1.2V
D1	TXLOW	Power	A	Internal power supply.
D2	MCP	Output	D	MIPI clock (+)
D3	MCN	Output	D	MIPI clock (-)
D4	MDN0	Output	D	MIPI data<0> (-)
D5	DGND	Ground	D	Ground for digital

3.2 Package Specification

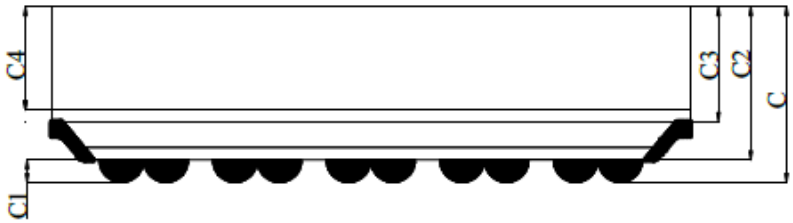
Figure 4: Mechanical Drawing View(μ m)



Top View(Bumps Down)



Back View(Bumps Up)



Side View

Table 7: Package Specifications

Description	symbol	Nominal	Min	Max
		Millimeters		
Package Body Dimension X	A	2.869	2.844	2.894
Package Body Dimension Y	B	1.741	1.716	1.766
Package Height	C	0.710	0.655	0.765
Ball Height	C1	0.110	0.080	0.140
Package Body Thickness	C2	0.600	0.565	0.635
Thickness from top glass surface to wafer	C3	0.445	0.425	0.465
Glass Thickness	C4	0.400	0.390	0.405
Ball Diameter	D	0.200	0.170	0.230
Total Ball Count	N	19		
Ball Count X axis	N1	5		
Ball Count Y axis	N2	4		
Pins pitch X axis	J1	0.510		
Pins pitch Y axis	J2	0.700		
Pins pitch X axis	J3	0.310		
Pins pitch Y axis	J4	0.350		
Pins pitch X axis	J5	0.200		
Pins pitch Y axis	J6	0.350		
BGA ball center to package center offset in X-direction	X	0.0000	-0.0250	0.0250
BGA ball center to package center offset in Y-direction	Y	0.0000	-0.0250	0.0250
BGA ball center to chip center offset in X-direction	X1	0.0000	-0.0250	0.0250
BGA ball center to chip center offset in Y-direction	Y1	0.0000	-0.0250	0.0250
Edge to Pin Center Distance along X1	S1	0.5145	0.4850	0.5450
Edge to Pin Center Distance along Y1	S2	0.3455	0.3160	0.3760

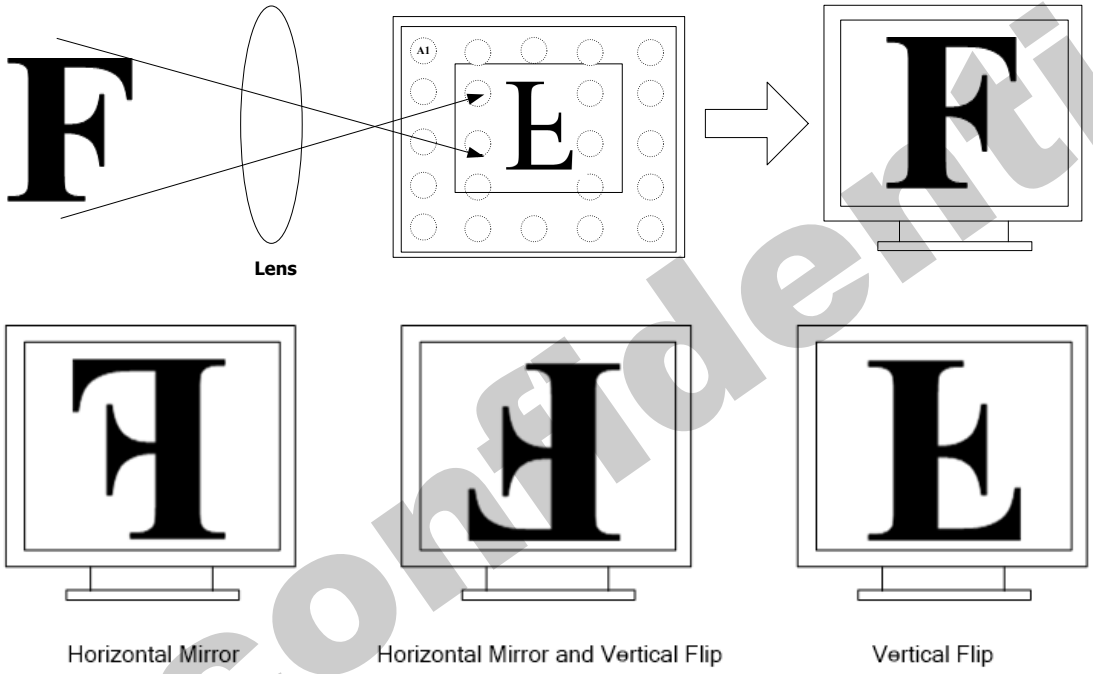
Note: The package center, optical center, and BGA center of the chip are not coincident. If setting the package center as the origin (0, 0), the BGA center coordinate is (0, 0), the optical center coordinate is (-136.225, -64.055), with μm unit

4. Optical Specifications

4.1 Readout Position

GC1029 default status is readout from the lower left corner with pin A1 located in the upper left corner. The image is inverted vertically and horizontally by the lens, so proper image output results when Pin A1 is located in the upper left corner.

Figure 5: Readout Position



Readout direction can be set by the registers.

Table 8: Mirror and Flip Information

Function	Register Address	Register Value	First Pixel
Normal	0x0015[1:0]	00	Gr
Horizontal mirror	0x0015[1:0]	01	R
Vertical Flip	0x0015[1:0]	10	B
Horizontal Mirror and Vertical Flip	0x0015[1:0]	11	Gb

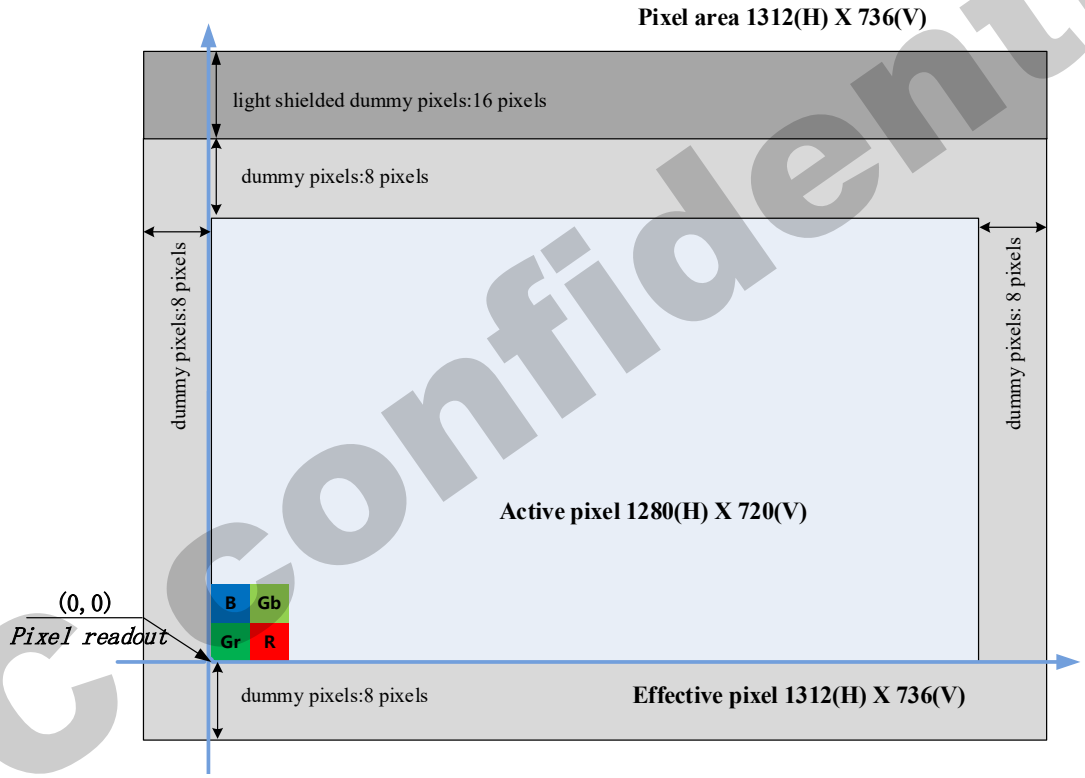
4.2 Pixel Array

Pixel array is covered by Bayer pattern color filters. The primary color GR/BG array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 1279. If flip in column, column is read out from 1279 to 0.

If no flip in row, row is read out from 0 to 719.If flip in row, row is read out from 719 to 0.

Figure 6: Pixel Array



4.3 Lens Chief Ray Angle (CRA)

Figure 7 CRA Information

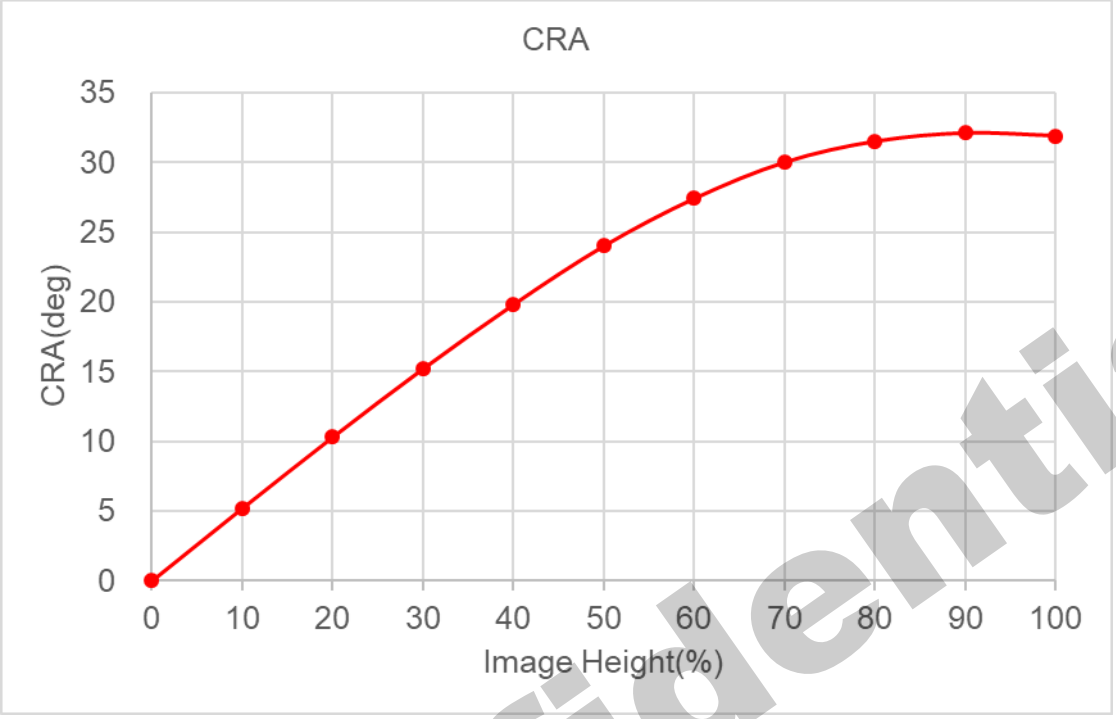


Table 9: CRA Information

Image Heigh (%)	Image Height (mm)	CRA (degree)
00	0.000	0.000
10	0.103	5.200
20	0.206	10.300
30	0.308	15.200
40	0.411	19.800
50	0.514	24.000
60	0.617	27.400
70	0.720	30.000
80	0.822	31.500
90	0.925	32.100
100	1.028	31.900

4.4 QE Spectral Characteristics

The optical spectrum of QE is below:

Figure 8 QE curve

TBD

5. Two-wire Serial Bus Communication

GC1029 Device Address:

Table 10: Device ID

ID_SEL	Slave address write mode	Slave address read mode
0(default)	0x6e	0x6f
1	0x20	0x21

NOTE: When IDSEL0/IDSEL1 is "High", it means connect to IOVDD. When IDSEL0/IDSEL1 is "Low", you should connect it to DGND.

5.1 Protocol

The host must perform the role of a communications master and GC1029 acts as either a slave receiver or transmitter. The master must do:

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**

Figure 9: Write operate (2 bytes address –1byte data format)

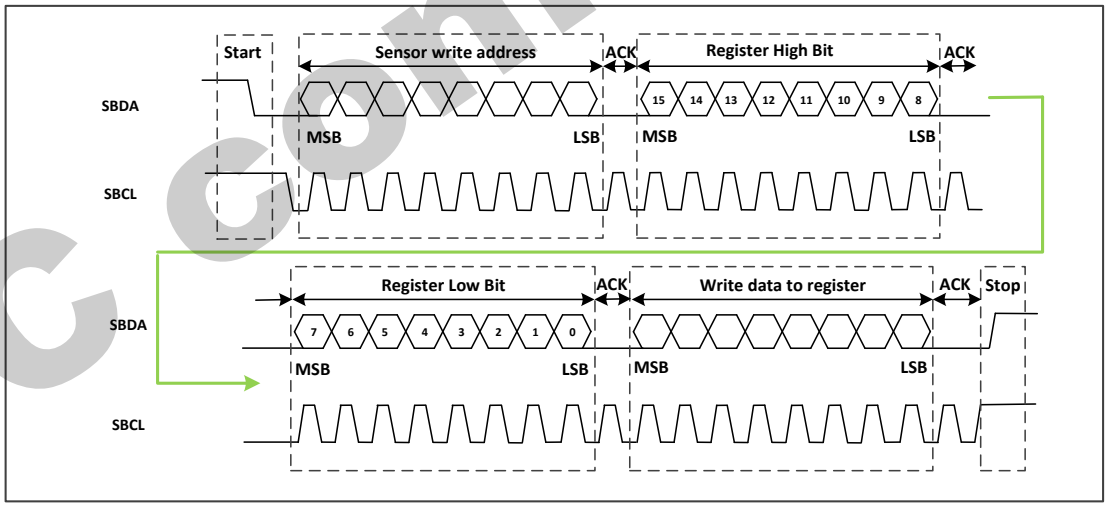
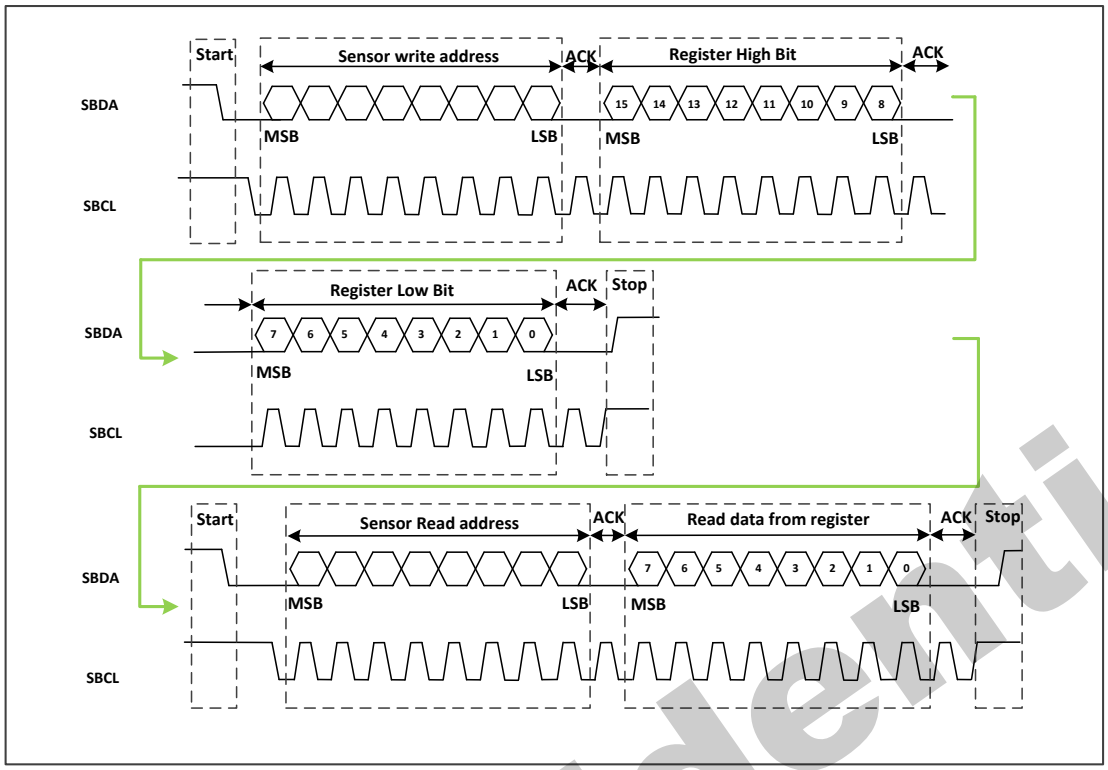


Figure 10: Read Operate (2 bytes address –1byte data format)



5.2 Serial Bus Timing

Figure 11: Serial Bus Timing

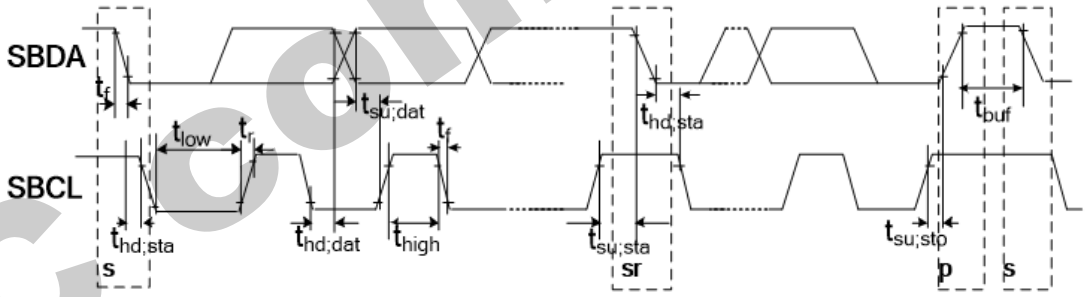


Table 11: Serial Bus Timing

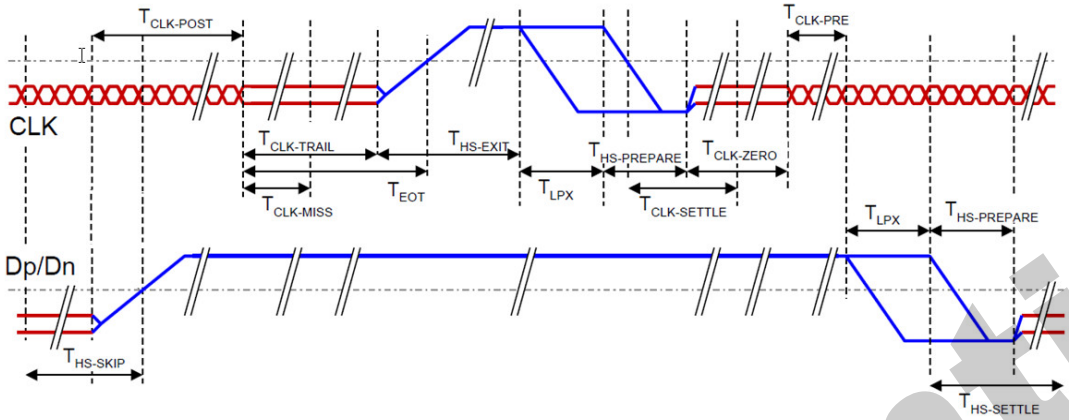
Parameter	Symbol	Min	Typ.	Max	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between a stop and a start	t_{buf}	1.3	--	--	μs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for a repeated start	$t_{su;sta}$	600	--	--	ns

Data hold time	$t_{hd;dat}$	0	--	900	ns
Data Set-up time	$t_{su;dat}$	100	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	300	ns
Fall time of SBCL, SBDA	t_f	--	--	300	ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	100	pf

6. MIPI Timing

6.1 Clock Lane Low-power

Figure 12: MIPI Clock Lane Time

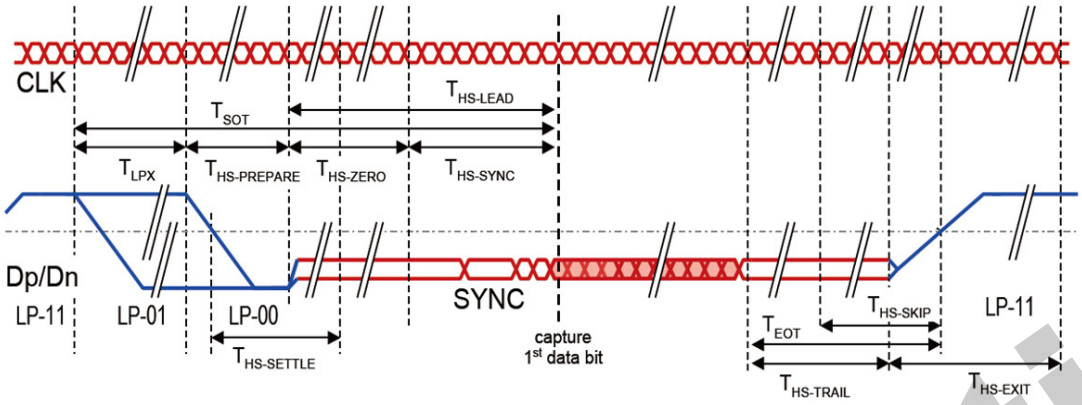


Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

6.2 Data Burst

Figure 13: MIPI Data Lane Time



Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

7. Function Description

7.1 Operation Mode

Figure 14: Operation Mode

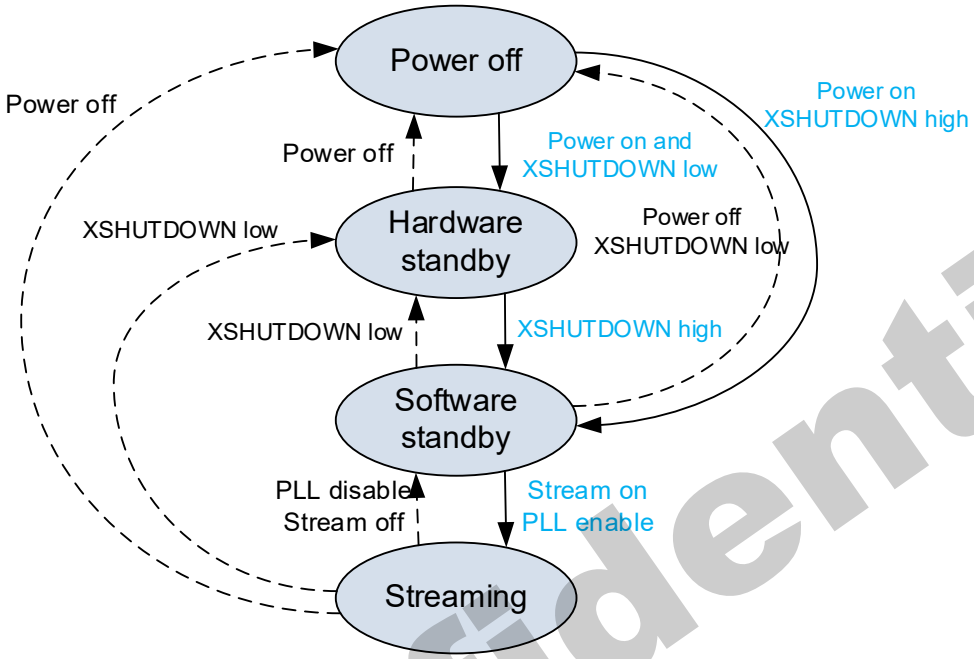


Table 12: Operate State

Power state	Description	Activate
Power off	Power supplies are turned off	None
Hardware standby	No communication with sensor, low level on XSHUTDOWN	XSHUTDOWN low
Software standby	Two- wire serial communication with sensor is possible, pll is ready for fast return to streaming mode	Stream mode off PLL disable XSHUTDOWN high
Streaming	Sensor is fully powered and streaming image data on the MIPI CSI-2 bus	All Pad Enabled

7.2 Power on Sequence

Figure 15: Power on Timing

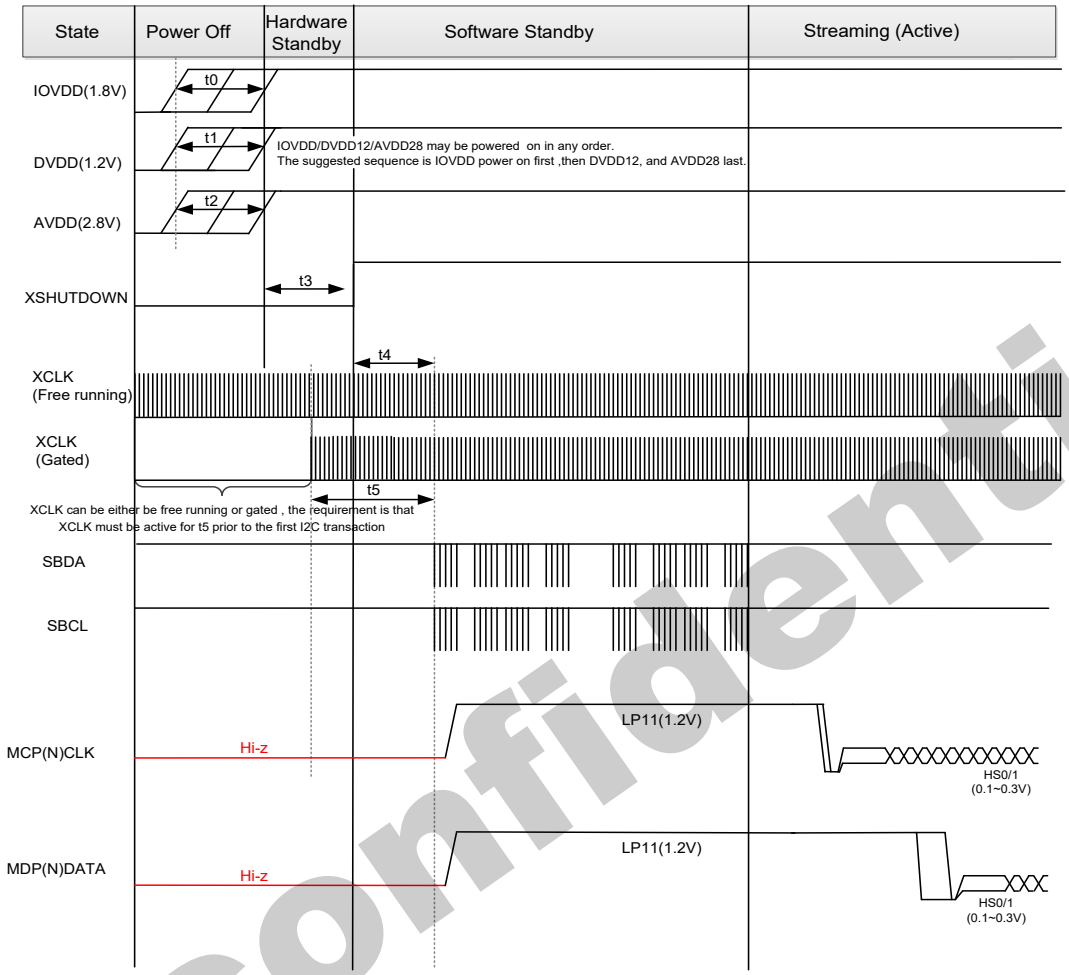


Table 13: Power on Timing

Parameter	Description	Min.	Max.	Unit
t0	IOVDD/DVDD12/AVDD28 may rise in any order. The rising separation can vary from 0μs to indefinite.	0	-	μs
t1				
t2				
t3	From power on to XSHUTDOWN pull high	0	-	μs
t4	XSHUTDOWN rising to first I2C transaction	50	-	μs
t5	Minimum No. of XCLK cycles prior to the first I2C transaction	1200	-	XCLK

Note: 1. IOVDD/DVDD12/AVDD28 may rise in any order.
2. The suggested sequence is IOVDD powered on first, then DVDD12, and AVDD28 last.
3. Register should be reloaded before works.

7.3 Power off Sequence

Figure 16: Power off Timing

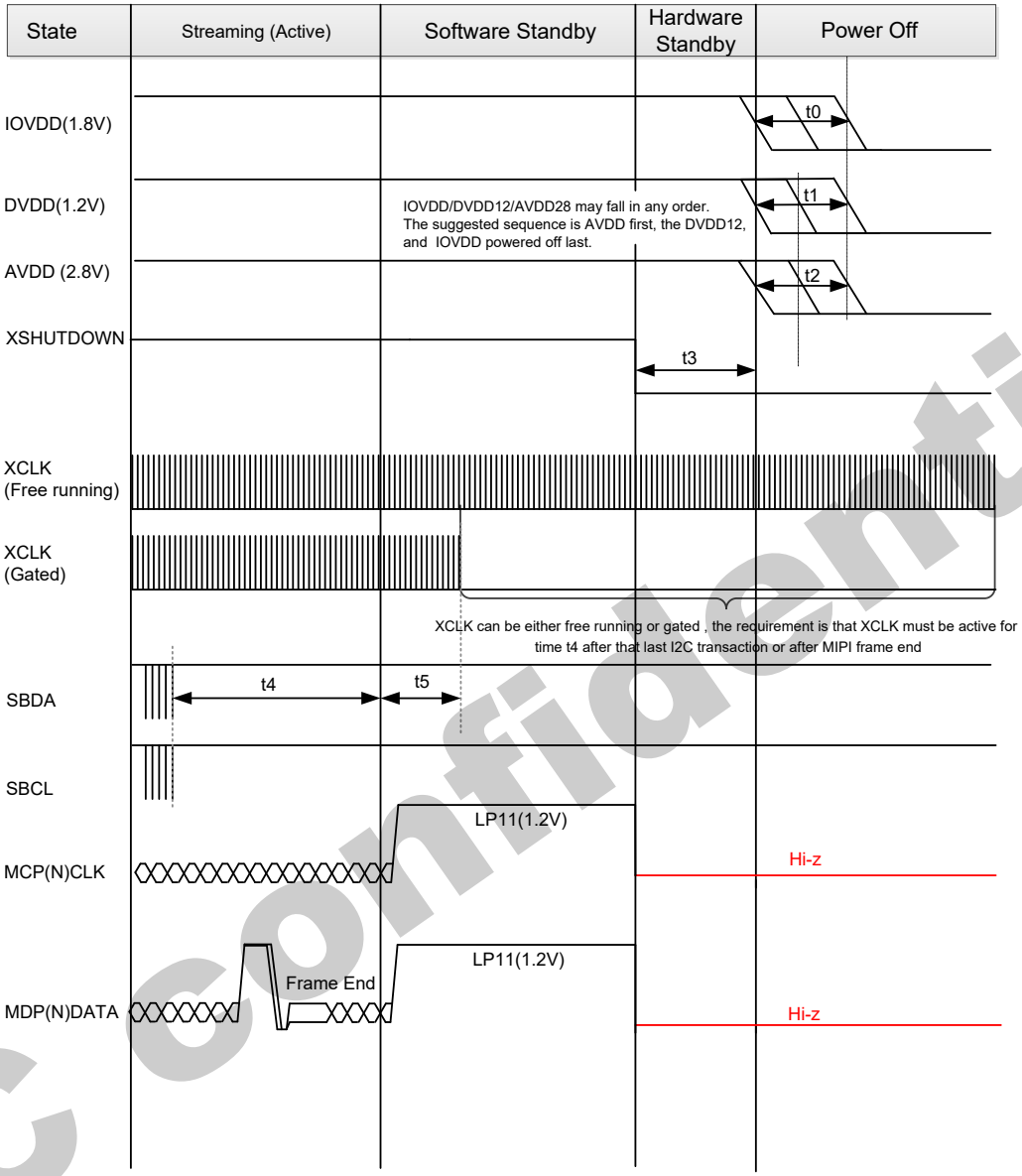


Table 14: Power off Timing

Parameter	Description	Min.	Max.	Unit
t0	IOVDD/DVDD12/AVDD28 may fall in any order. The fall separation can Vary from 0μs to indefinite.	0	-	μs
t1				
t2				
t3	From XSHUTDOWN pull down to power off	0		μs
t4	Enter Software Standby command – Device in Software Standby mode	0	-	μs

t5	Minimum number of XCLK cycles after the last transaction or MIPI frame end code.	2000		XCLK

Note: 1. IOVDD/DVDD12/AVDD28 may fall in any order. The suggested sequence is AVDD first, the DVDD12, and IOVDD powered off last.
2. If the sensor’s power cannot be cut off, please keep power supply, then set XSHUTDOWN pin low. It will make sensor standby.
3. If the standby sequence needs to be modified, please contact FAE of *Galaxycore Inc*.

7.4 Black Level Calibration

Black level is caused by pixel characteristics and analog channel offset, which makes poor image quality in dark condition and color balance, to reduce these, sensor automatically calibrates the black level every frame with light shield pixel array.

7.5 Integration Time

The integration time is controlled by the shutter time registers. When you want to set an exposure value that is bigger than the current frame length value, you should first set a new frame length and make sure that it’s bigger than the exposure value you’d like to set.

Table 15: Shutter Time Register

Addr.	Register name	Description
0x0603	Shutter time	[5:0] shutter time[13:8]
0x0604		[7:0] shutter time[7:0]

7.6 Windowing

GC1029 has a rectangular pixel array 1280 x 720, it can be windowed by output size control, the output image windowing can be used to adjust output size, and it will affect field angle.

Figure 17: Windowing Mode

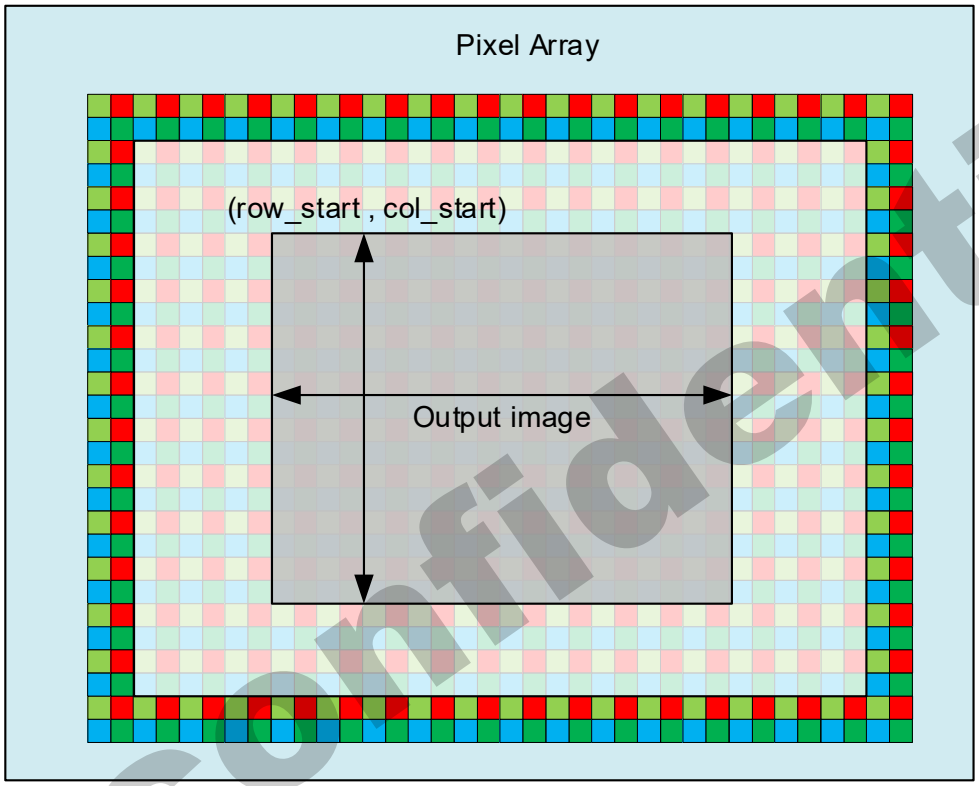


Table 16: Window Set Register

Addr.	Register name	Description
0x060d	win_height	[2:0]win_height[9:8]
0x060e		[7:0]win_height[7:0]
0x000f	win_width	[3:0]win_width[10:8]
0x0010		[7:0]win_width[7:0]
0x000b	Row start	[2:0]row_start[10:8]
0x000c		[7:0]row_start [7:0]
0x0609	Col start	[2:0]col_start[10:8]
0x060a		[7:0]col_start[7:0]

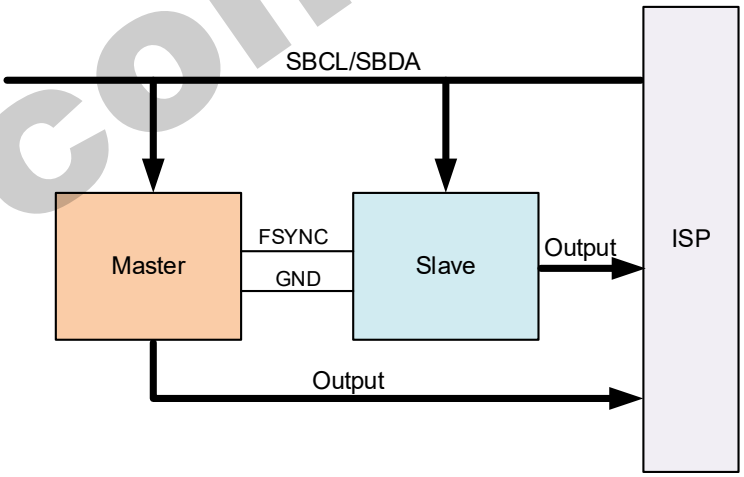
Table 17: Out Window Set Register

Addr.	Register name	Description
0x0191	out_win_y1	[3:0] out_win_y1[9:8]
0x0192		[7:0] out_win_y1[7:0]
0x0193	out_win_x1	[3:0] out_win_x1[10:8]
0x0194		[7:0] out_win_x1[7:0]
0x0195	out_win_height	[3:0] out_win_height[9:8]
0x0196		[7:0] out_win_height[7:0]
0x0197	out_win_width	[3:0] out_win_width[10:8]
0x0198		[7:0] out_win_width[7:0]

7.7 Frame Sync Mode

GC1029 can support hardware frame sync for dual camera application. It can be set both master and slave sensor. When use this mode, the two sensor's FSYNC pin must connect to each other.

Figure 18: Frame Sync Configuration



Master Mode:

When GC1029 operates as a master device, it controls vertical synchronous timings and outputs synchronous signal called Vsync signal or Fsync signal from the FSYNC pin.

Slave Mode:

GC1029 can be worked as a slave and automatically synchronized within a certain VSYNC time period. It is important to control two image sensors’ rolling shutters with the same timing.

7.8 Binning Mode

GC1029 has Binning mode which support a lower resolution output with high frame rate. The row or col can be independent controlled. However, only the row binning can increase frame rate.

Table 18: Binning mode Register

Addr.	Register name	Description
0x0015	Row Binning	[2] Row Binning enable
0x0040	Col Binning	[3] Col Binning enable

7.9 OTP memory

GC1029 sensor has 2K bits embedded OTP (One Time Programmable) memory.

7.10 Frame Structure

Frame structure is controlled by line length, frame length, window height, window width.

Frame length control:

Frame length is controlled by window height, and shutter time.

◆ Frame length depend shutter time.

- Minimum frame length = window height + 16 +VB (VB_min = 16)
- If shutter time < minimum frame length: Actual frame length = minimum frame length
- If shutter time > minimum frame length: Actual frame length = shutter time + 16 (recommended).

Table 19: Frame Length Register

Addr.	Register name	Description
0x0641	Frame length	[7:0] frame length[15:8]
0x0642		[7:0] frame length[7:0]

Line length control:

Line length control for internal set, and not recommended to be modified.

Table 20: Line Length Register

Addr.	Register name	Description
0x0607	Line length	[3:0] Line length[13:8]
0x0608		[7:0] Line length[7:0]

Blank time control:

Line blank time is controlled by line length.

Frame blank time = frame length – out window height

Figure 19: Frame Structure