



GC08A3 COB

1/4" 8Mega CMOS Image Sensor

Assembly Guide

V0.3

Preliminary

2021-03-05

Ordering Information

◆ GC08A3-WA1XA

(Color, 150um, back grinding, reconstructed wafer)

GENERATION REVISION HISTORY

Version.	Effective Date	Description of Changes	Prepared by
V0.0	2020-11-19	Preliminary version	AE Dept.
V0.1	2020-12-24	Update Pad info. and etc.	AE Dept.
V0.2	2021-02-02	Update Pixel size info. Update Pad size info.	AE Dept.
V0.3	2021-03-05	Update Module Application Circuit	AE Dept.

Galaxycore Incorporation

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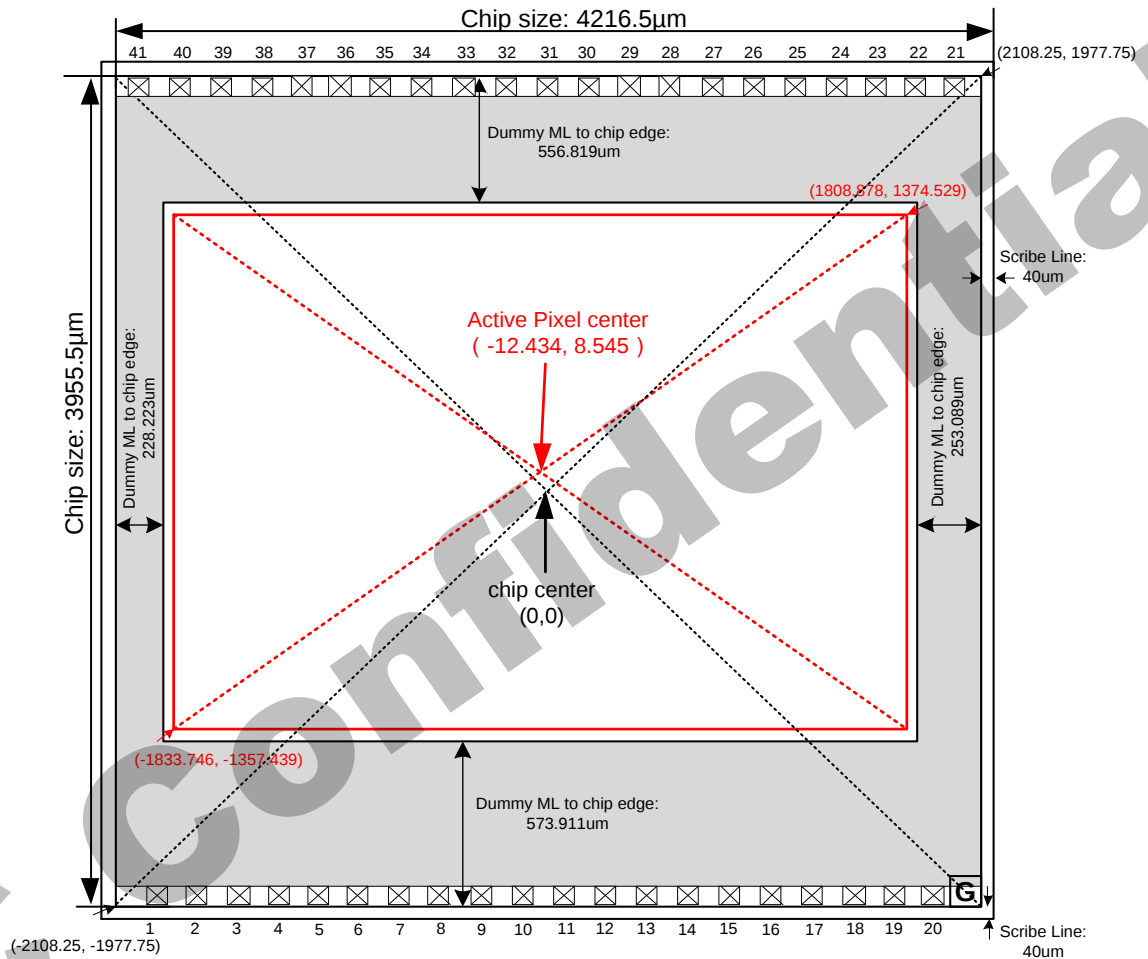
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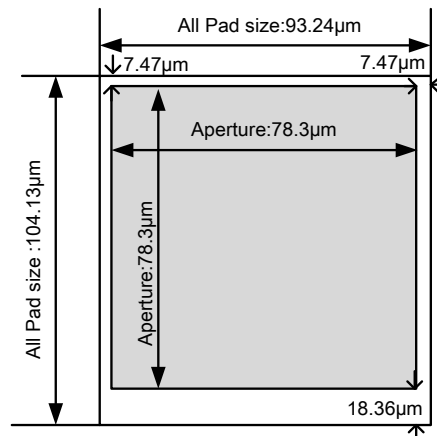
1. Device Description

Parameters	Description
Optical Format	1/4 inch
Unit Pixel Size	1.12μm x 1.12μm
Effective Resolution	3264 (H) x 2448(V) 8Mp
Color Filter	Bayer
Shutter Type	Electronic Rolling Shutter
Scan Mode	Line progressive readout
Operating Temperature	-20℃ to 70℃
Supply Voltage	AVDD28: 2.8 V DVDD: 1.2V IOVDD: 1.8V
Number of output	MIPI 4 lane
Dark Level	TBD
Sensitivity	TBD
Dynamic Range	TBD
Output Format	Raw 10
Max. frame rate	30fps@full size
ADC resolution	10 bit

2. Package Specification

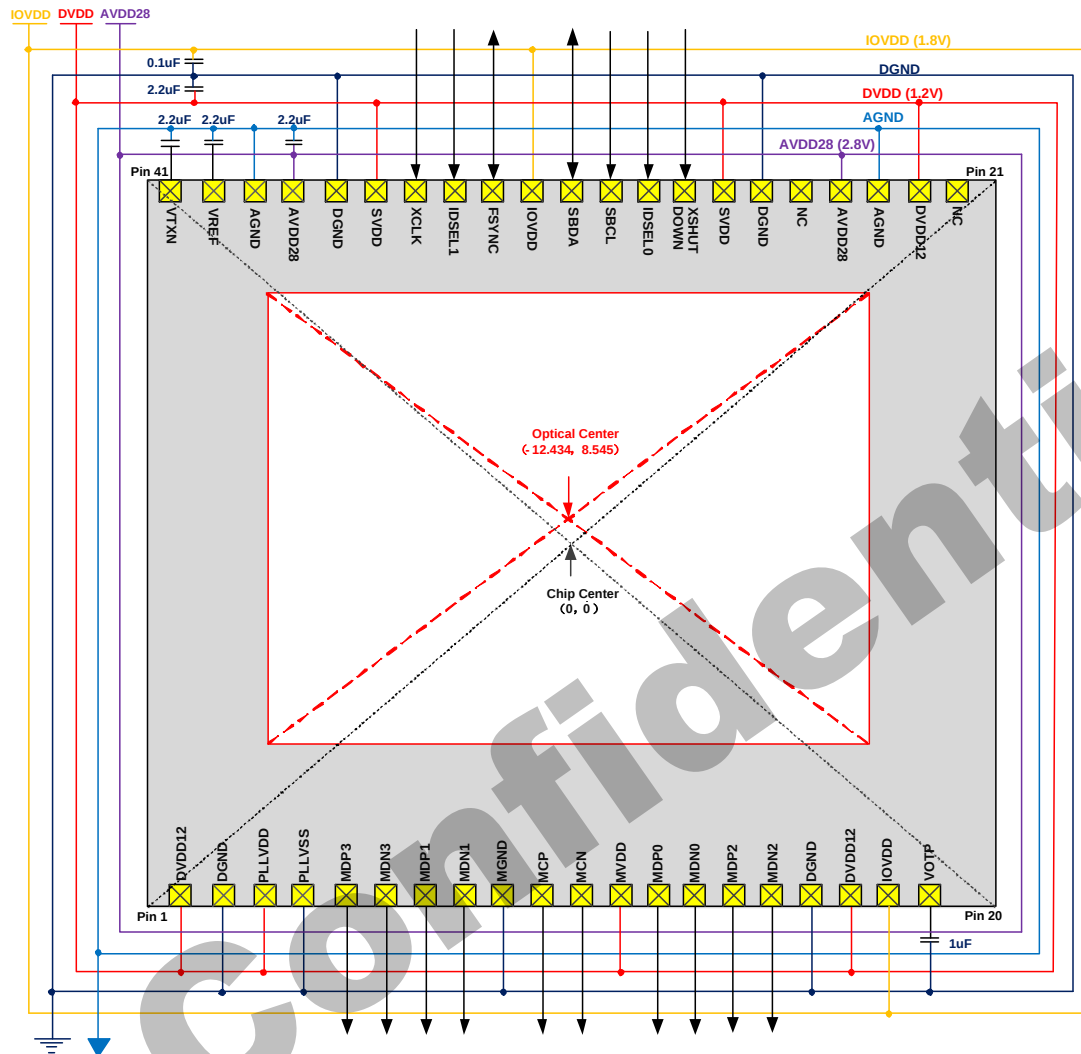
2.1 Bonding Diagram (Top View)





Die size	- Without Scribe Lane: 4216.5µm x 3955.5 µm - With Scribe Lane: 4296.5µm x 4035.5 µm
Pad Pitch	190µm
Bonding Pad Open size	78.3 µm x 78.3 µm
Total number of pads	41ea (w/o dummy PADs)
Total number of bonding pads	39ea
Optical Center	(-12.434µm , 8.545µm)

2.2 Module Application Circuit



NOTE:

- GC08A3 Chip requires three power supplies: AVDD28, DVDD, IOVDD ;
AVDD28 indicates analog power supply, 2.7~3.0V (Typ. 2.8V).
DVDD12 indicates digital power supply, 1.15~1.3V (Typ.1.2V).
IOVDD indicates I/O power supply, 1.7~1.9V (Typ.1.8V).
- The Ground for Auto Focus must be separated from Sensor Ground.
- In the case of GC08A3, the digital Ground (DGND) and the analog Ground (AGND) must be separated on the module PCB, but both Grounds (DGND

and AGND) should be merged at the phone PCB for better performance.

3. *MIPI Ground* (Pad #9) must be merged with digital ground.
4. *MIPI power* (Pad #12) must be merged with DVDD.
5. Differential Signals (MCP MCN, MDP0, MDN0, MDP1, MDN1, MDP2, MDN2, MDP3, MDN3): Differential impedance = 100 ohm $\pm$ 10%, C < 1 pF
7. PCB design should be considered to guarantee high speed differential pair signals go out to the most outer pad.
8. MIPI CLK/DATA pairs should have the same routing length to minimize intra-pair differential signals skew between DP and DN (CP and CN).
9. The metal lines from outer pads to CIS pads should be as straight as possible.
10. You should not place the other signals which do not relate to MIPI near the MIPI differential signals.
11. Capacitors:

Capacitor No.	Power	Capacitor(μ F)
C1	AVDD28	2.2
C2	DVDD	2.2
C3	IOVDD	0.1
C4	VTXN	2.2
C5	VREF	2.2
C6	VOTP	1

Note: The above capacitor solution is based on Galaxycore's testing environment.

2.3 COB Package Pin Description

- NC = Not connected

Pin	X(um)	Y(um)	Name	Type	A/D	Description
1	-1899.7	-1886.8	DVDD12	Power	D	Digital power supply pin: 1.15~1.3V
2	-1709.6	-1886.8	DGND	Ground	D	Ground for digital
3	-1519.5	-1886.8	PLLVD	Power	D	PLL power supply pin: 1.15~1.3V
4	-1329.4	-1886.8	PLLVS	Ground	D	Ground for PLL
5	-1102.3	-1886.8	MDP3	Output	D	MIPI data <3> (+)
6	-904.3	-1886.8	MDN3	Output	D	MIPI data <3> (-)
7	-706.3	-1886.8	MDP1	Output	D	MIPI data <1> (+)
8	-508.3	-1886.8	MDN1	Output	D	MIPI data <1> (-)
9	-310.3	-1886.8	MGND	Ground	D	Ground for MIPI
10	-112.3	-1886.8	MCP	Output	D	MIPI clock (+)
11	85.7	-1886.8	MCN	Output	D	MIPI clock (-)
12	283.7	-1886.8	MVDD	Power	D	MIPI power supply pin: 1.15~1.3V
13	481.7	-1886.8	MDP0	Output	D	MIPI data <0> (+)
14	679.7	-1886.8	MDN0	Output	D	MIPI data <0> (-)
15	877.7	-1886.8	MDP2	Output	D	MIPI data <2> (+)
16	1075.7	-1886.8	MDN2	Output	D	MIPI data <2> (-)
17	1316.4	-1886.8	DGND	Ground	D	Ground for digital
18	1506.5	-1886.8	DVDD12	Power	D	Digital power supply pin: 1.15~1.3V
19	1696.5	-1886.8	IOVDD	Power	D	Power supply for I/O circuits: 1.7~1.9V
20	1886.6	-1886.8	VOTP	Power	D	OTP power supply pin
21	1901.5	1886.8	NC			

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22	1711.4	1886.8	DVDD12	Power	D	Digital power supply pin: 1.15~1.3V
23	1521.3	1886.8	AGND	Ground	A	Ground for analog
24	1331.2	1886.8	AVDD28	Power	A	Main power supply pin: 2.7~3.0V
25	1141.1	1886.8	NC			
26	951.1	1886.8	DGND	Ground	D	Ground for digital
27	761.0	1886.8	SVDD	Power	D	Digital power supply pin: 1.15~1.3V
28	570.9	1886.8	XSHUTD OWN	Input	D	Reset and PWDN multiplexing 0: standby state 1: normal operation
29	380.8	1886.8	IDSEL0	Input	D	I2C slave address control
30	190.7	1886.8	SBCL	Input	D	Two-wire serial bus, clock
31	0.7	1886.8	SBDA	IO	D	Two-wire serial bus, data
32	-189.4	1886.8	IOVDD	Power	D	Power supply for I/O circuits: 1.7~1.9V
33	-379.5	1886.8	FSYNC	IO	D	Frame sync control
34	-569.6	1886.8	IDSEL1	Input	D	I2C slave address control
35	-759.7	1886.8	XCLK	Input	D	Sensor input clock
36	-949.7	1886.8	SVDD	Power	D	Digital power supply pin: 1.15~1.3V
37	-1139.8	1886.8	DGND	Ground	D	Ground for digital
38	-1329.9	1886.8	AVDD28	Power	A	Main power supply pin: 2.7~3.0V
39	-1520.0	1886.8	AGND	Ground	A	Ground for analog
40	-1710.1	1886.8	VREF	Power	A	Internal power supply
41	-1900.1	1886.8	VTXN	Power	A	Internal power supply

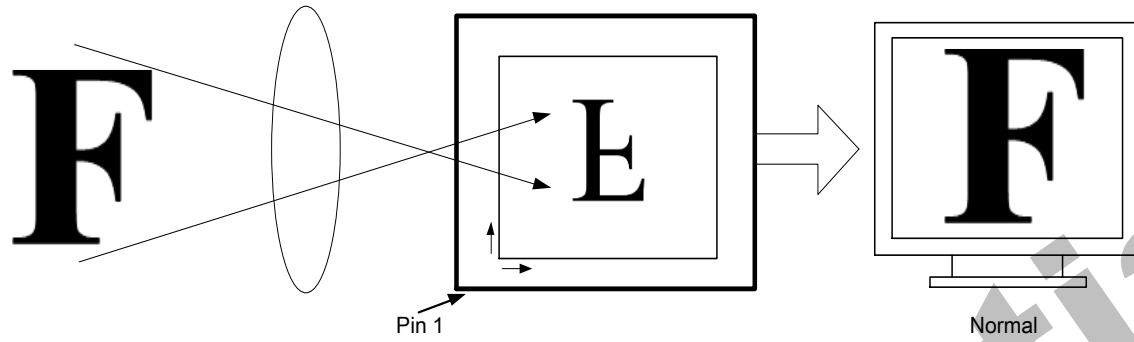
2.4 I2C ID Select Mode

Table for I2C option pad

IDSEL1 (PIN 34)	IDSEL0 (PIN 29)	Slave address
Low	Low	0x62/0x63
Low	High	0x20/0x21
High	Low	0x22/0x23
High	High	0x24/0x25

NOTE: When IDSEL0/IDSEL1 is "High", it means connect to IOVDD. When IDSEL0/IDSEL1 is "Low", you should connect it to DGND.

3. Chip Direction



4. u-Lens Specification (CRA Spec)

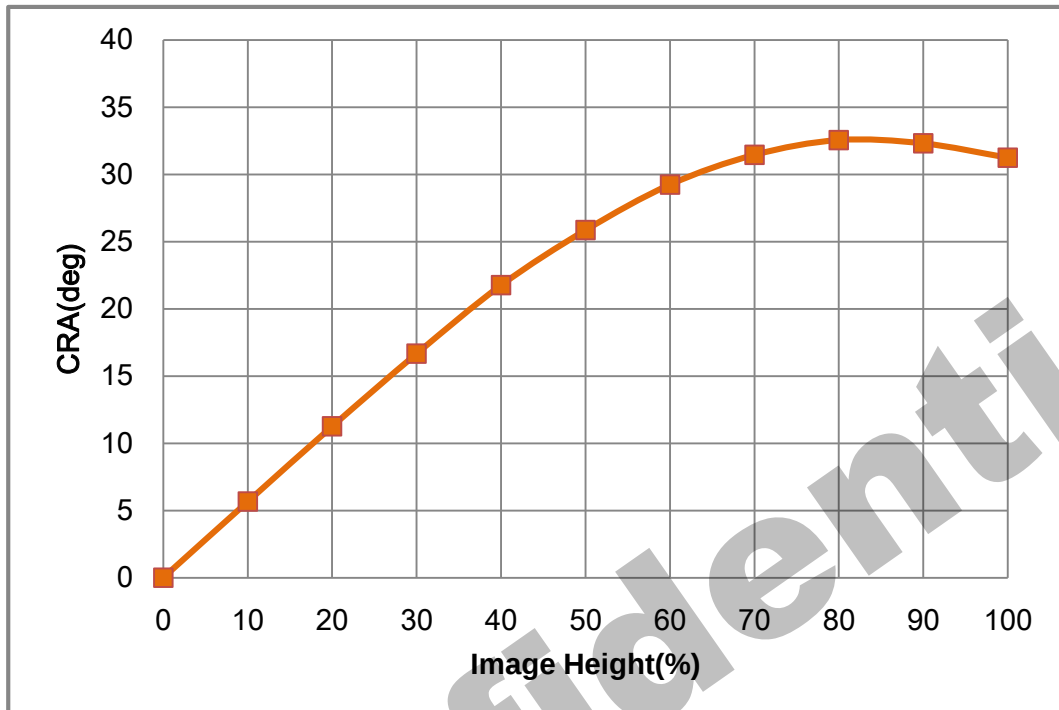


Image Height(%)	Image Height (mm)	CRA (degree)
00	0.000	0.00
10	0.228	5.65
20	0.455	11.25
30	0.683	16.66
40	0.911	21.75
50	1.138	25.85
60	1.366	29.24
70	1.594	31.45
80	1.821	32.55
90	2.049	32.30
100	2.277	31.24