GC030A CSP

1/10’’ VGA CMOS Image Sensor

Datasheet

Rev.1.03

2016-02-05

Ordering Information

- **GC030AC**

  (Color, 16pin-CSP)

GENERATION REVISION HISTORY

REV.	EFFECTIVE DATE	DESCRIPTION OF CHANGES	PREPARED BY
1.0	2015-9-25	Document Release	AE Dept.
1.01	2015-10-30	Update technical specifications	AE Dept.
1.02	2015-11-23	Update sensitivity, Chip ID	AE Dept.
1.03	2016-02-05	Update DC Parameter	AE Dept.

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1. Sensor Overview

1.1 General Description

The GC030A features 640V x 480H resolution with 1/10-inch optical format, and 4-transistorpixel structure for high image quality and low noise variations. It delivers superior image quality by powerful on-chip design of a 10-bit ADC, and embedded image signal processor.

The full scale integration of high-performance and low-power functions makes the GC030A fit the design, reduce implementation process, and extend the battery life of cell phones, PDAs, and a wide variety of mobile applications.

It provides RAW10 and RAW8 data formats with MIPI interface. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Standard optical format of 1/10 inch
- Output formats: Raw Bayer 10bit/8bit
- Power supply requirement: AVDD28: 2.7~3.0V
  IOVDD: 1.7~1.9V , 2.8V
- PLL support
- Windowing support
- MIPI interface support
- Horizontal/Vertical mirror
- Package: CSP/COB/wafer

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1.3 Application

- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipment

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/10 inch
Pixel Size	2.25um x 2.25um
Active pixel array	648 x 488
ADC resolution	10 bit ADC
Max Frame rate	VGA:30fps@24MHz,MCLK
Power Supply	AVDD28: 2.7~3.0V IOVDD: 1.7~1.9V ,2.8V
Power Consumption	70mW@30fps(active) <150uA @HW standby
SNR	40dB
Dark Current	4.2mV/s
Sensitivity	11000e-/lux.sec
Dynamic range	68dB
Operating temperature:	-20~70℃
Stable Image temperature	0~50℃
Optimal lens chief ray angle(CRA)	30 °(linear)
Package type	CSP/COB/Wafer

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2. DC Parameters

2.1 Standby Current

Hardware PWDN

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	15	100	uA
I/O	I_{IOVDD}(1.8V)	—	20	400	uA
Power off	-		0	0	uA

PWND: H

Typ. Analog: 2.8V, T_j=25℃

2.2 Operation Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	18	30	mA
I/O	I_{IOVDD}(1.8V)	—	12	25	mA

INCLK: 24MHz, Frame rate: 30fps , Raw 10

DCLK: 24MHz

Typ. Analog: 2.8V, T_j=25℃

2.3 DC Characteristics

Item	Symbol	Min	Typ	Max	Unit
Power supply	V_{AVDD}	2.7	2.8	3.0	V
	V_{IOVDD}	1.7	1.8	2.8	V
Digital Input(Conditions: AVDD = 2.8V,IOVDD = 1.8V)					
Input voltage HIGH	$\mathbf{V_{IH}}$	1.4			V
Input voltage LOW	$\mathbf{V_{IL}}$			0.6	V
Digital Output(Conditions: AVDD = 2.8V, IOVDD = 1.8V, standard Loading 25PF)					
Output voltage HIGH	$\mathbf{V_{OH}}$	1.6			V
Output voltage LOW	$\mathbf{V_{OL}}$			0.2	V

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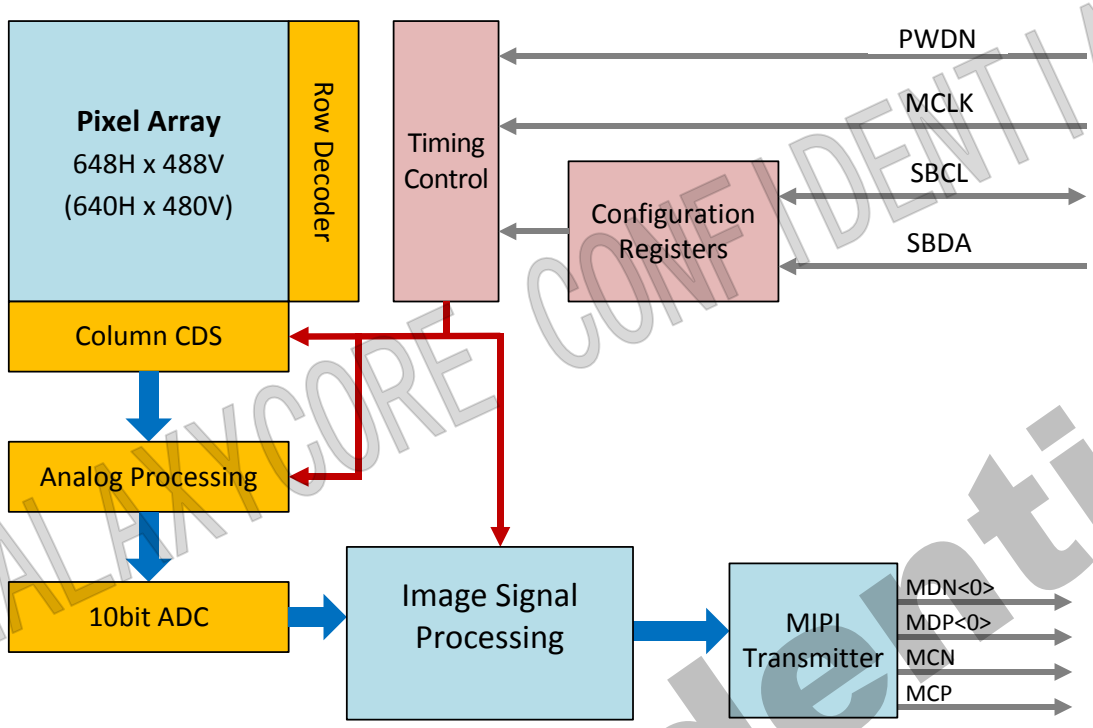
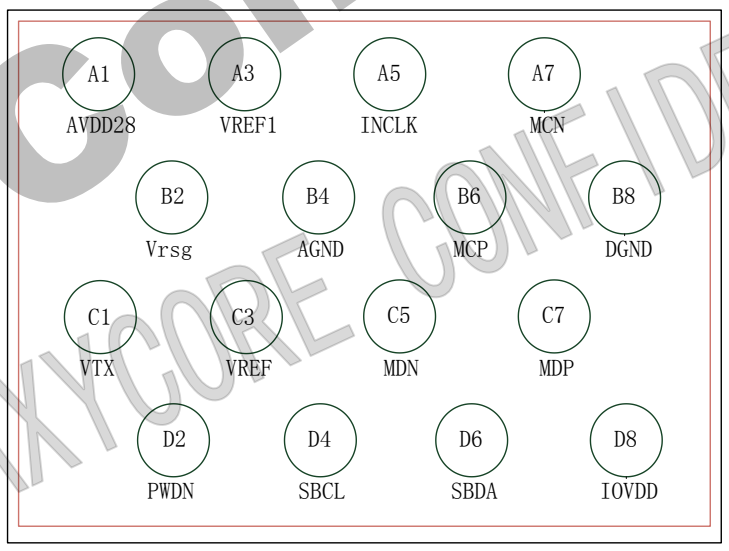
3. Block Diagram



4. CSP Package

4.1 Pin Diagram



Top View

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4.2 Pin Descriptions

Pin	Name	Pin Type	Description
A1	AVDD28	Power	Power for analog circuit/sensor array, 2.7~3.0V, connect Capacitor (≥1uF) to analog ground
A3	VREF1	Power	Internal analog reference voltage, connect Capacitor (≥0.1uF) to digital ground
A5	INCLK	Input	Sensor input clock
A7	MCN	Output	MIPI clock (-)
B2	Vrsg	power	Internal analog reference voltage, connect Capacitor (≥0.1uF) to analog ground
B4	AGND	Ground	Ground for Analog
B6	MCP	Output	MIPI clock (+)
B8	DGND	Ground	Ground for digital
C1	VTX	Power	Internal analog reference voltage, connect Capacitor (≥0.1uF) to analog ground
C3	VREF	Power	Internal analog reference voltage, connect Capacitor (≥0.1uF) to analog ground
C5	MDN	Output	MIPI data (-)
C7	MDP	Output	MIPI data (+)
D2	PWDN	Input	Power down (active high)
D4	SBCL	Input	SCCB input clock
D6	SBDA	I/O	SCCB data
D8	IOVDD	Power	Power Supply for I/O circuits, 1.7~3.0V , connect Capacitor (≥0.1uF) to digital ground

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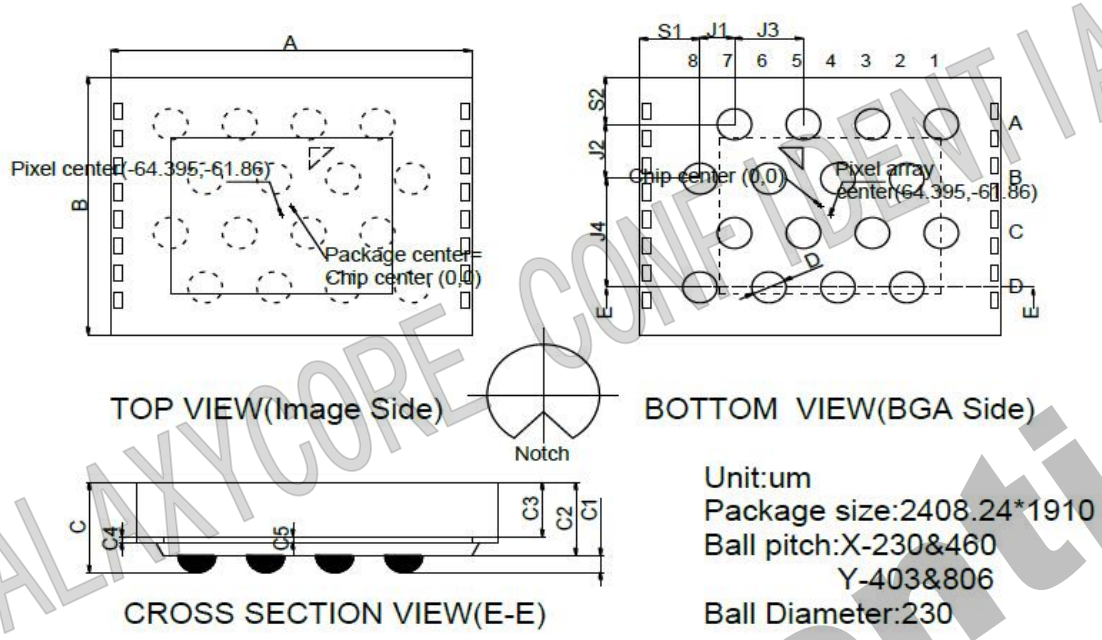
4.3 Package Specification (unit: mm)



Description	Symbol	Nominal	Min.	Max.
		Millimeters		
Package Body Dimension X	A	2.408	2.383	2.433
Package Body Dimension Y	B	1.910	1.885	1.935
Package Height	C	0.690	0.635	0.745
Ball Height	C1	0.130	0.100	0.160
Package Body Thickness	C2	0.560	0.525	0.595
Thickness from top glass surface to wafer	C3	0.400	0.390	0.410
Ball Diameter	D	0.230	0.200	0.260
Total Ball Count	N	16		
Pin Pitch X1 axis	J1	0.230		
Pin Pitch X2 axis	J3	0.460		
Pin PitchY1 axis	J2	0.403		
Pin PitchY2 axis	J4	0.806		
Edge to Pin Center Distance along X	S1	0.399	0.369	0.429
Edge to Pin Center Distance along Y	S2	0.3505	0.3205	0.3805

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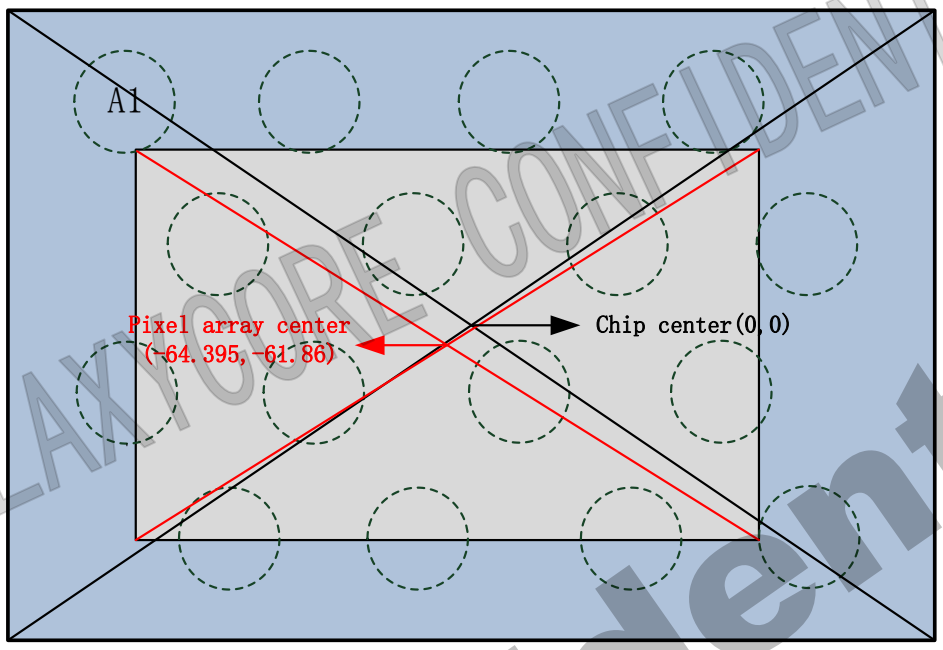
5. Optical Specifications

5.1 Optical Center (unit: μm)



Top View

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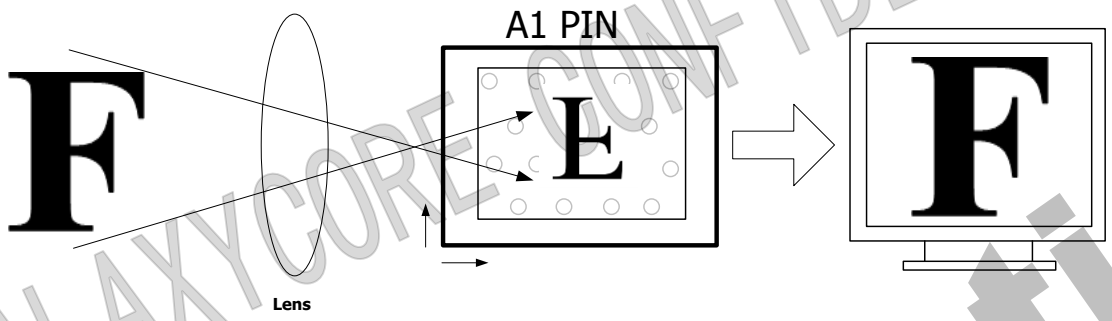
5.2 Readout Position

The 030A default status is readout from the lower left corner with pin A1 located in the upper left corner. The image is inverted vertically and horizontally by the lens, so mirrored image output results when Pin A1 is located in the upper left corner.



Readout direction can be set by the registers.

Function	Register Address	Register Value	First Pixel
Normal	P0:0x17[1:0]	00	R
Horizontal mirror	P0:0x17[1:0]	01	Gr
Vertical Flip	P0:0x17[1:0]	10	Gb
Horizontal Mirror and Vertical Flip	P0:0x17[1:0]	11	B

Horizontal Mirror　　Vertical Flip　　Horizontal Mirror and Vertical Flip

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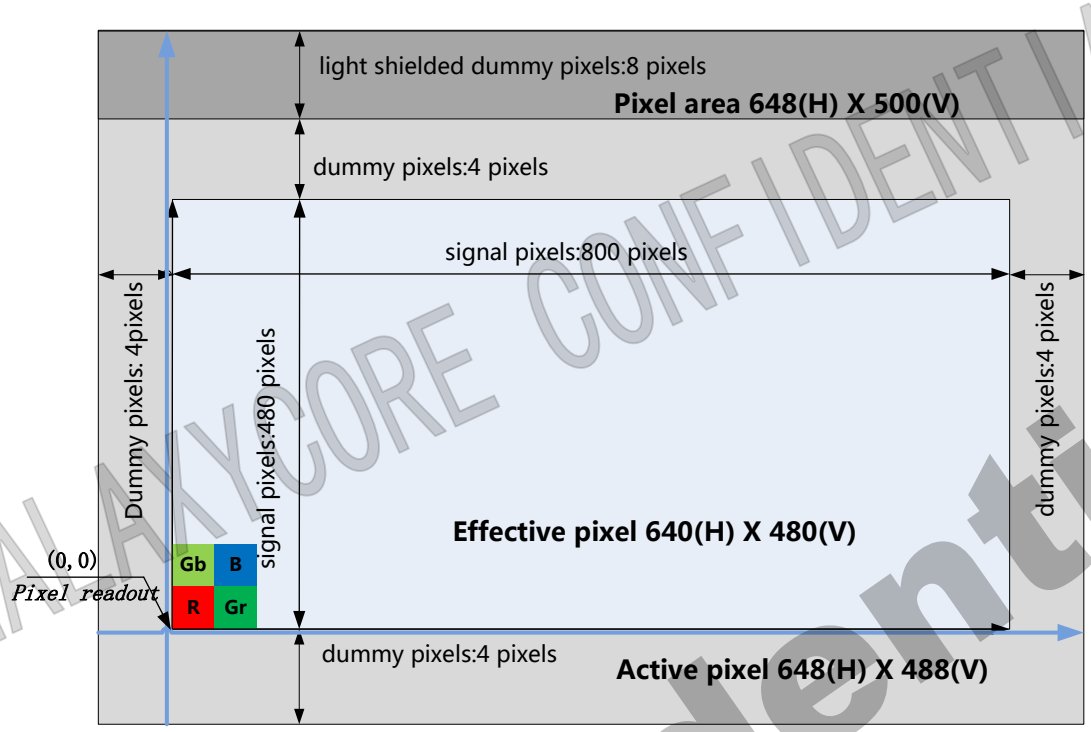
5.3 Pixel Array



Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 647.If flip in column, column is read out from 647 to 0.

If no flip in row, row is read out from 0 to 479.If flip in row, row is read out from 479 to 0.

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5.4 Lens Chief Ray Angle (CRA)

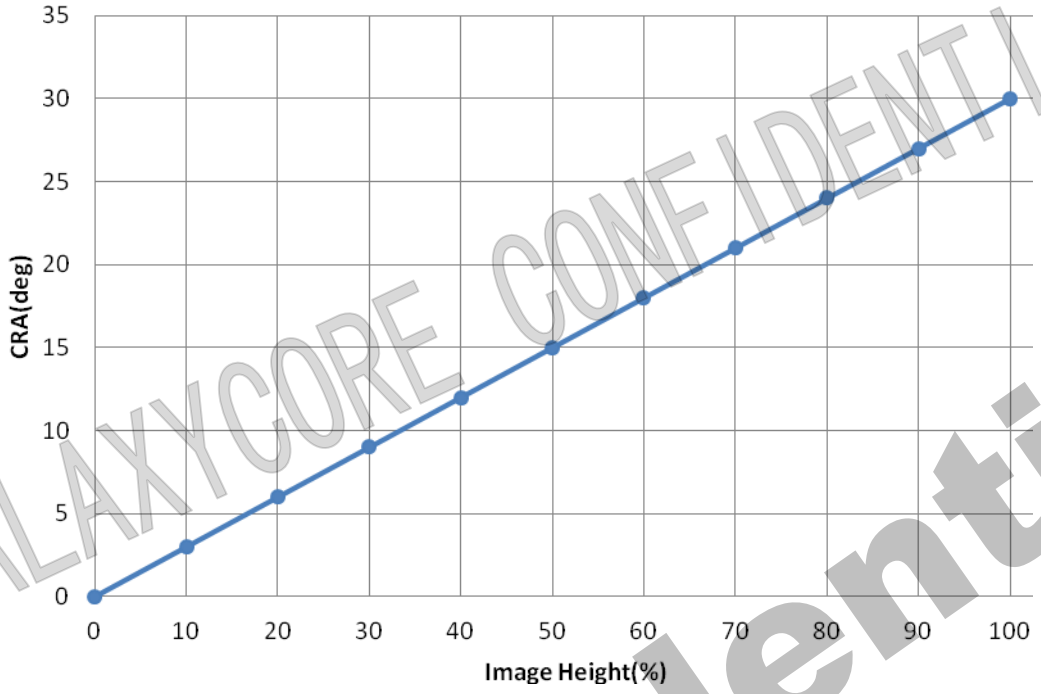

Image Height （%）	Image Height(mm)	CRA(degree)
0	0.000	0.00
10	0.090	3.00
20	0.180	6.00
30	0.270	9.00
40	0.360	12.00
50	0.450	15.00
60	0.540	18.00
70	0.630	21.00
80	0.720	24.00
90	0.810	27.00
100	0.900	30.00

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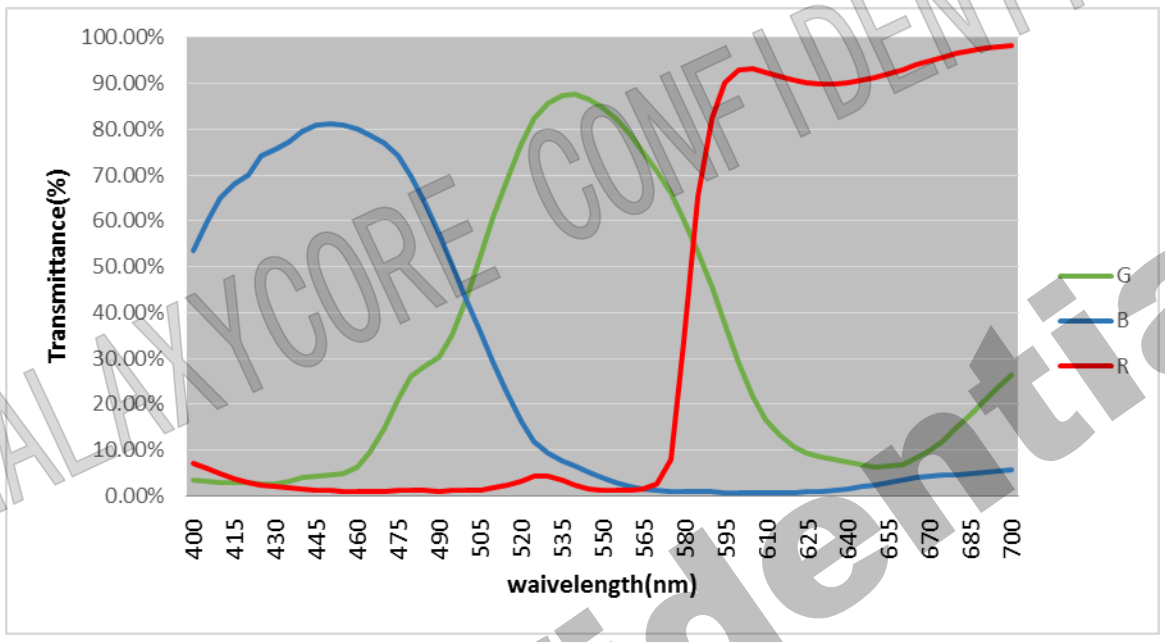
5.5 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below



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6. Two-wire Serial Bus Communication

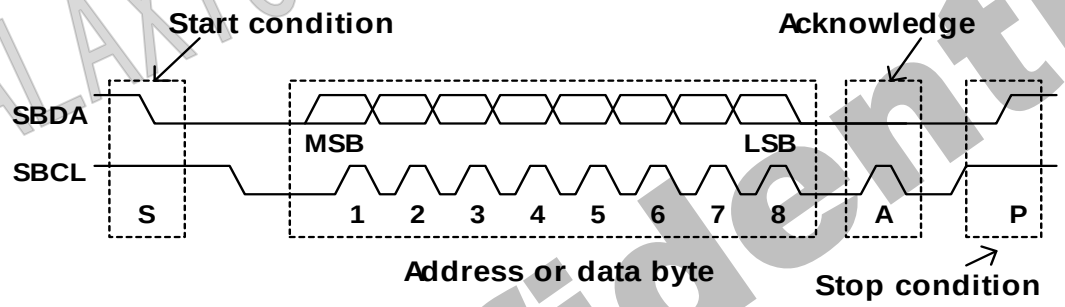
GC030A I2C Address:

Serial bus write address = 0x42, serial bus read address = 0x43

6.1 Protocol

The host must perform the role of a communications master and GC030A acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**.



Single Register Writing:

S	42H	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	42H	A	Register Address	A	Data(1)	A	……	Data(N)	A	P

Single Register Reading:

S	42H	A	Register Address	A	S	43H	A	Data	NA	P

Notes:

From master to slave From slave to master

S: Start condition **P:** Stop condition

A: Acknowledge bit **NA:** No acknowledge

Register Address: Sensor register address

Data: Sensor register value

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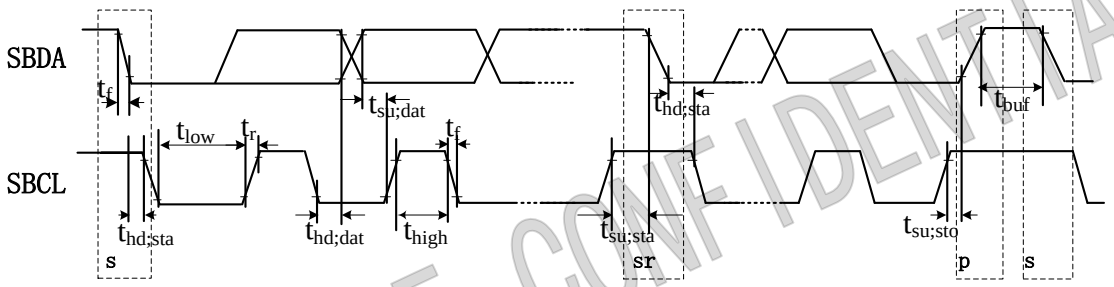
6.2 Serial Bus Timing



Parameter	Symbol	Min.	Typ.	Max.	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between stop and start condition	t_{buf}	1.3	--	--	μs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for a repeated start	$t_{su;sta}$	0.6	--	--	μs
Data hold time	$t_{hd;dat}$	0	--	0.9	μs
Data Set-up time	$t_{su;dat}$	100	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	300	ns
Fall time of SBCL, SBDA	t_f	--	--	300	ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	--	pf

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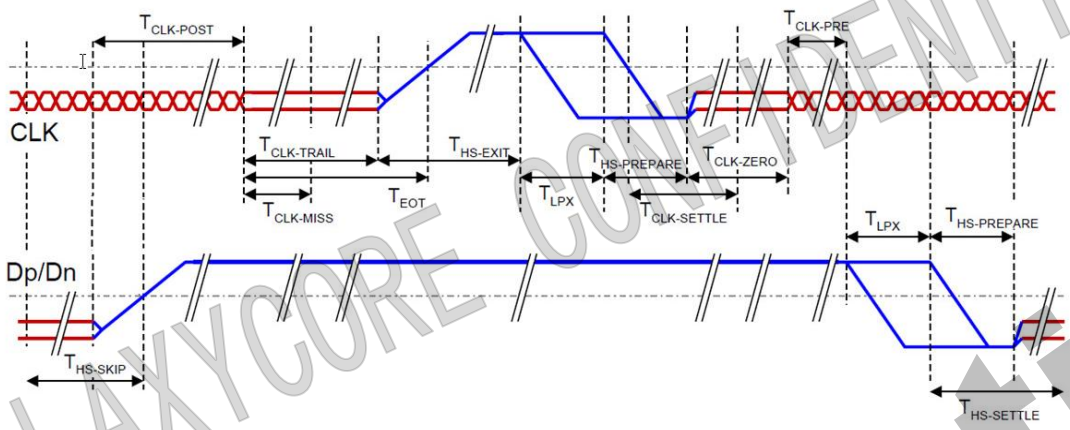
7. Applications

7.1 Clock lane low-power



Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

  $T_{CLK\_HS\_PRE}$: setting by Register P3: 0x22

  T_{CLK_ZERO}: setting by Register P3: 0x23

  T_{CLK_PRE}: setting by Register P3: 0x24

  T_{CLK_POST}: setting by Register P3: 0x25

  T_{CLK_TRAIL}: setting by Register P3: 0x26

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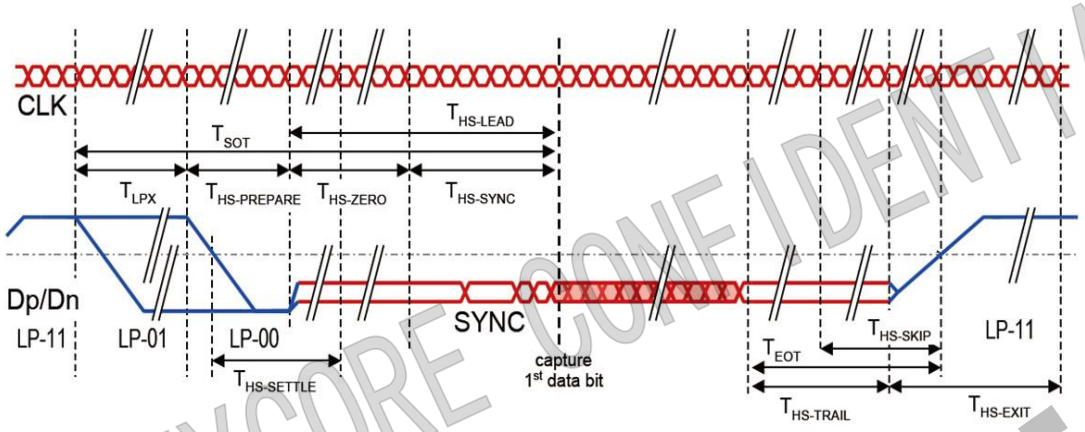
7.2 Data Burst



Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

T_{LPX}: setting by Register P3: 0x21

$T_{HS\_PREPARE}$: setting by Register P3: 0x29

T_{HS_ZERO}: setting by Register P3: 0x2a

T_{HS_TRAIL}: setting by Register P3: 0x2b

T_{HS_EXIT}: setting by Register P3: 0x27

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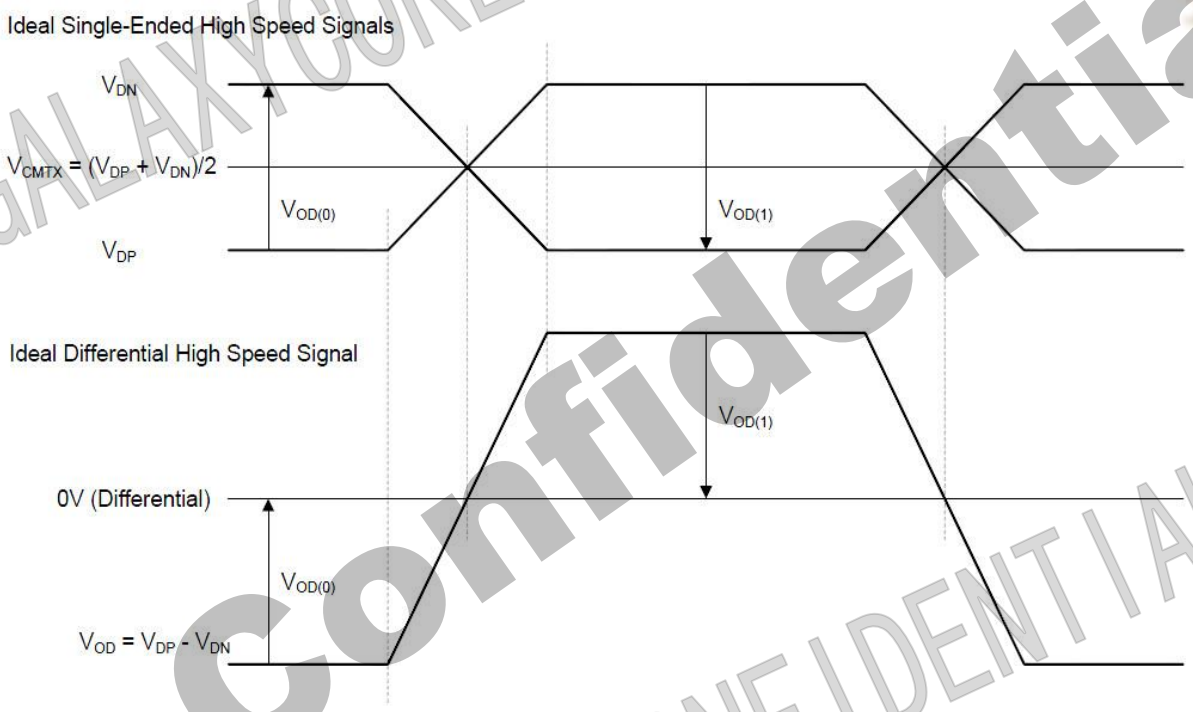
7.3 HS Transmitter DC specifications

Parameter	Description	Min	Type	Max	Unit
VCMTX	HS transmit static common-mode voltage	150	200	250	mV
|ΔVCMTX(1,0)|	VCMTX mismatch when output is Differential-1 or Differential-0			5	mV
VOD	HS transmit differential voltage	140	200	270	mV
|ΔVOD|	VOD mismatch when output is Differential-1 or Differential-0			360	mV



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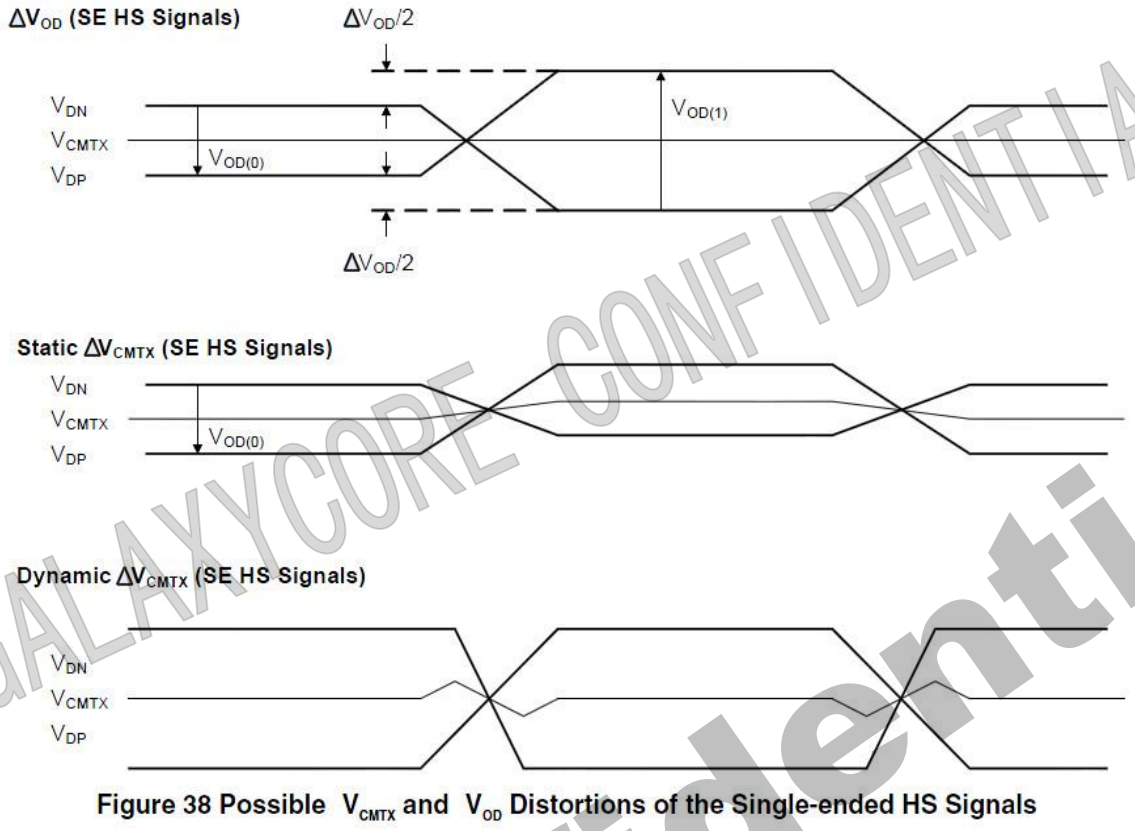

Figure 38 Possible V_{CMTX} and V_{OD} Distortions of the Single-ended HS Signals

7.4 LP Transmitter DC specifications

Parameter	Description	Min	Type	Max	Unit
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V
V_{OL}	Thevenin output low level	-50		50	mV

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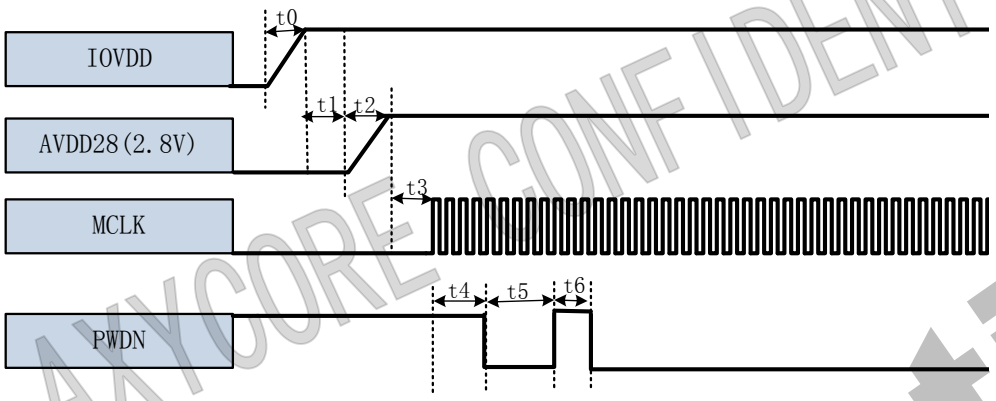
8. Power On/Off Sequence

Power On Sequence



Parameter	Description	Min.	Max.	Unit
t0	IOVDD rising time	50		μs
t1	From IOVDD to AVDD	5		μs
t2	AVDD rising time	50		μs
t3	From AVDD to MCLK applied	50		μs
t4	From MCLK applied to PWDN pull low	10		μs
t5	From PWDN pull low to PWDN pull high	0		μs
t6	From PWDN pull high to PWDN pull low	1		μs

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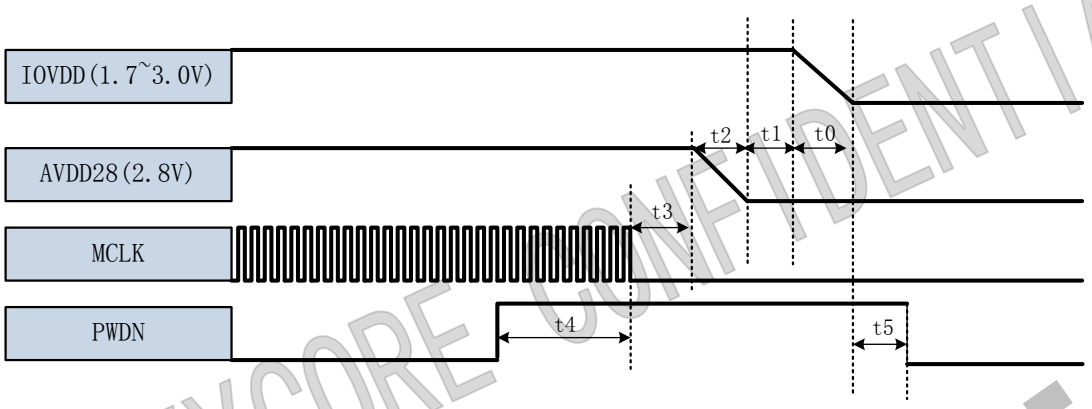
Power Off Sequence



Parameter	Description	Min.	Max	Unit
t0	IOVDD falling time	0		μs
t1	From IOVDD to AVDD falling time	0		μs
t2	AVDD falling time	0		μs
t3	From MCLK disable to sensor AVDD power down	0		μs
t4	From sensor disable to MCLK disable	0		μs
t5	From sensor disable to PWDN pull low	0		μs

- **Recommended power on/off sequence is above.**
- **If you have special requirements in application, please contact with us to confirm.**
- **If the sensor's power cannot be cut off, please keep power supply, then set PWDN pin high.**

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9. Register List

System Register

Address	Name	Width	Default Value	R/W	Description
0xf0	**Sensor_ID_highbit**	**8**	**0x03**	**RO**	**Sensor_ID**
0xf1	**Sensor_ID_low**	**8**	**0x0a**	**RO**	**Sensor_ID**
0xf4	I2C_open_ena	2	0x00	RW	[4] I2C_open_ena
0xf7	PLL_mode1	3	0x04	RW	[2] auto_div2en [1] div2en [0] pll_en
0xf8	PLL_mode2	8	0x00	RW	[7]freq_div2_en [6] freq_div2_close frame mode [5:0] divx4
0xf9	Cm_mode	8	0x0e	RW	[7] regf clk enable [6] use internal clk [5] clk_3_2_div [4] sync_use_pll_mode [3] isp all clock enable [2] serial clk enable [1] freq_div2_pad_mode [0] not_use_pll
0xfa	isp_clk_mode	8	0x00	RW	[7:4] ISP clock divider
0xfb	i2c_device_id	7	0x74	RW	[7:1] i2c_device_id
0xfc	analog_pwd	8	0x53	RW	[7:6]Reserved [0] apwd
0xfd	isp_div_mode2	8	0x11	RW	
0xfe	Reset control	8	0x00	RW	[7] soft_reset [6] cm_reset [5] mipi_reset [4] CISCTL_restart_n [3] PLL_reset [2:0] page_select

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Sensor control

Address	Name	Width	Default Value	R/W	Description
P0:0x03	exp [11:8]	4	0x00	RW	[7:4] NA [3:0] exposure[11:8], use line processing time as the unit.
P0:0x04	exp [7:0]	8	0x10	RW	[7:0] Exposure
P0:0x05	HB[11:8]	4	0x01	RW	H Blanking
P0:0x06	HB[7:0]	8	0x64	RW	
P0:0x07	VB[11:8]	4	0x00	RW	Vertical blanking, if current exposure < (Vb + window Height) , frame rate will be (Vb + window Height); otherwise frame rate will be determined by exposure
P0:0x08	VB[7:0]	8	0x16	RW	
P0:0x09	Row_start[8]	1	0x00	RW	Row Start
P0:0x0a	Row_start[7:0]	8	0x0c	RW	
P0:0x0b	Col_start[9:8]	2	0x00	RW	Col start
P0:0x0c	Col_start[7:0]	8	0x04	RW	
P0:0x0d	win_height[8]	1	0x01	RW	[7:1]NA [0] Window height[8]
P0:0x0e	win_height[7:0]	8	0xe8	RW	[7:0] Window height[7:0]
P0:0x0f	win_width[9:8]	2	0x02	RW	[7:2] NA [1:0] Window width[9:8]
P0:0x10	win_width[7:0]	8	0x88	RW	[7:0] window width[7:0]
P0:0x13	Vs_st	8	0x09	RW	Vs_st
P0:0x14	Vs_et	8	0x01	RW	Vs_et
P0:0x17	Flip-flop	8	0X14	RW	[7:2] reserved [1] updown [0] mirror

CSI/PHY1.0

Address	Name	Width	Default Value	R/W	Description
P3:0x01	DPHY_analog_mode1	8	0x00	RW	[5] CTD_lane0 [4] CTD_clk [2] phy-lane1_en [1] phy_lane0_en [0] phy_clk_en
P3:0x02	DPHY_analog_mode2	8	0x00	RW	[6:4] lane0_diff [2:0] clk_diff
P3:0x03	DPHY_analog_mo	8	0x00	RW	[7]clklane_p2s_sel

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	de3				[5] lane0_delay [4] clk_delay [2] lpldo_en [1:0]lpldo_r
P3:0x04	FIFO_prog_full_level[7:0]	8	0x01	RW	FIFO_prog_full_level[7:0]
P3:0x05	FIFO_prog_full_level[9:8]	2	0x00	RW	[7:2] NA [1:0] FIFO_prog_full_level[11:8]
P3:0x06	FIFO_mode	8	0x80	RW	[7]free clk mode [6] manual CSI2_up mode [4]fifo_rst_mode [3]write_gate_mode [2]data_mode [1]no flop mode [0] mipi_write_gate mode
P3:0x10	buf_CSI2_mode	8	0x94	RW	[7] lane_ena [6] NA [5] ULP_mode [4] MIPI_ena [3] bit10_swicth [2] RAW8 [1] line_sync_mode [0] double_lane
P3:0x11	LDI_set	8	0x2a	RW	RAW10 2b，RAW8 2a，YUV422 1e
P3:0x12	LWC_set[7:0]	8	0x20	RW	640x5/4 RAW10
P3:0x13	LWC_set[15:8]	8	0x03	RW	
P3:0x14	SYNC_set	8	0xb8	RW	SYNC_set
P3:0x15	DPHY_mode	8	0x00	RW	[7] DATA_gate [6]MIPI_para_inv [3:2]switch msb mode [1:0] clklane_mode
P3:0x16	LP_set	8	0x29	RW	[7:6] hi-z [5:4]one cycle [3:2] 1 [1:0] 0
P3:0x20	T_init_set	8	0x80	RW	Timing of initial setting, more than 100 us
P3:0x21	T_LPX_set	8	0x10	RW	Timing of LP setting, more than 50ns
P3:0x22	T_CLK_HS_PREPARE_set	8	0x05	RW	Timing of COCLK HS PREPARE setting, 38ns ~95ns LP00
P3:0x23	T_CLK_zero_set	8	0x30	RW	Timing of COCLK HS zero setting, more than 300ns
P3:0x24	T_CLK_PRE_set	8	0x02	RW	Timing of COCLK HS PRE of Data setting,

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					more than 8UI
P3:0x25	T_CLK_POST_set	8	0x10	RW	Timing of COCLK HS Post of Data setting, 60ns +52UI
P3:0x26	T_CLK_TRAIL_set	8	0x08	RW	Timing of COCLK tail setting, 60ns
P3:0x27	T_HS_exit_set	8	0x10	RW	Timing of HS exit setting, more than 100ns
P3:0x28	T_wakeup_set	8	0xa0	RW	Timing of wakeup setting, 1ms
P3:0x29	T_HS_PREPARE_set	8	0x06	RW	Timing of data HS PREPARE setting, 45+4UI~85+5UI
P3:0x2a	T_HS_Zero_set	8	0x0a	RW	Timing of data HS zero setting, 140ns
P3:0x2b	T_HS_TRAIL_set	8	0x08	RW	Timing of data HS trail setting, 60ns

ISP Related

Address	Name	Width	Default Value	R/W	Description
P0:0x88	start_num	8	0x50	RW	[7:4] BLK start cnt th [3:0] start cnt th
P0:0x89	Output mode	8	0x03	RW	Reserved
P0:0x90	win_mode	1	0x01	RW	[7:1]NA [0]crop out win mode
P0:0x91	out_win_y1[9:8]	2	0x00	RW	[7:2] NA [1:0] Crop _win_y1[9:8]
P0:0x92	out_win_y1[7:0]	8	0x00	RW	Crop _win_y1[7:0]
P0:0x93	out_win_x1[9:8]	2	0x00	RW	[7:2] NA [1:0] Crop _win_x1[9:8]
P0:0x94	out_win_x1[7:0]	8	0x00	RW	Crop _win_x1[7:0]
P0:0x95	out_win_height[9:8]	2	0x01	RW	[7:2] NA [1:0] Out window height[9:8]
P0:0x96	out_win_height[7:0]	8	0xe0	RW	Out window height[7:0]
P0:0x97	out_win_width[9:8]	2	0x03	RW	[7:2] NA [1:0] Out window width[9:8]
P0:0x98	out_win_width[7:0]	8	0x20	RW	Out window width[7:0]
P0:0x40	Blk_mode1	8	0x27	RW	[7:2] reserved [1:0] offset enable
P0:0x52	offset_X_ratio_inv	8	0x08	RW	offset_X_ratio_inv, 1.7bits
P0:0x5e	offset_ratio_G1_odd	8	0x00	RW	offset_ratio, 1.7bits
P0:0x6a	manual_G1_offset	6	0x00	RW	[5:0] manual_G1_offset S5，low align to 11

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P0:0x6b	manual_R1_offset	6	0x00	RW	[5:0] manual_R1_offset S5，low align to 11
P0:0x6c	manual_B2_offset	6	0x00	RW	[5:0] manual_B2_offset S5，low align to 11
P0:0x6d	manual_G2_offset	6	0x00	RW	[5:0] manual_G2_offset S5，low align to 11

AGC

Address	Name	Width	Default Value	R/W	Description
P0:0xa0	channel_gain_G1	8	0x80	RW	G1 Channel gain , 0x80 =1x
P0:0xa1	channel_gain_R1	8	0x80	RW	R1 Channel gain
P0:0xa2	channel_gain_B2	8	0x80	RW	B2 channel gain
P0:0xa3	channel_gain_G2	8	0x80	RW	G2 channel gain
P0:0xb0	Global gain[7:3]	8	0x40	RW	[7:3]global gain[7:3] [2:0]reserved
P0:0xb1	pregain_sync[9:6]	4	0x01	RW	[7:4] NA [3:0] pregain_sync[9:6]
P0:0xb2	pregain[5:0]	6	0x00	RW	[7:2] pregain [1:0] NA
P0:0xb3	WB R gain	8	0x40	RW	WB R gain
P0:0xb4	WB G gain	8	0x40	RW	WB G gain
P0:0xb5	WB B gain	8	0x40	RW	WB B gain ,0x40=1x
P0:0xb6	Analog gain	3	0x00	RW	[7:3] NA [2:0]Analog gain

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