1/4 inch 1M Global Shutter CIS

BF314FCS-W

Datasheet

content

1. General Description

BF314FCS-W is a Global shutter CMOS image sensor. It supports up to 120fps @ 1280Hx 800V with MIPI interface and 60fps @ 1280Hx 800V with DVP interface. BF314FCS-W outputs mono image, and the active pixel array is 1280H x 800V. Complex on-chip operations are supported, such as Trigger(global shutter), vertical/horizontal mirror or flip.

BF314FCS-W integrates some ISP modules.

BF314FCS-W is supported to be configured by standard IIC interface.

BF314FCS-W is supported to be triggered by Pin TRIG and internal register.

2. Features

- Standard optical format of 1/4 inch for 1M.
- 3.0μm Square Pixels with Micro-lens
- 120 frames/sec 1280H X 800V mode @ 168MHz inner clock with MIPI output.
- 60 frames/sec 1280H X 800V mode @ 84MHz inner clock with DVP output.
- 30 frames/sec 1280H X 800V @ 42MHz inner clock with DVP output.
- Input Frequency: 6MHz~27 MHz
- Output formats: Raw Bayer
- Horizontal mirror /Vertical flip.
- Auto black level control.
- Sensor Control function: Exposure control, Gain control, Test pattern, Image size control.
- Image processing function: Gamma Correction, Bad Pixel Correction, Low Pass Filter, Edge Enhancement, Auto exposure, Contrast, Lens shading correction.
- Package: CSP.

3. Applications

- Security systems
- Automotive
- Scanning system
- Digital still cameras and camcorders
- Video telephony and conferencing equipment
- Industrial and environmental systems

4. Technical Specifications

● Active pixel array:	1280*800
● Pixel size:	3.0um×3.0um
● Sensitivity:	TBD
● Dark current:	TBD
● Power supply:	1.75V~3.5V for I/O 1.45V~1.55V for VDDD 3.1V~3.5V for VDD3A
● Power consumption:	250mW@120fps(full resolution output);
● Standby current:	<150uA
● S/N Ratio:	TBD
● Dynamic range:	TBD
● Operating temperature:	-20~70℃
● Optimal lens chief ray angle:	26.78º no-linear
● Package:	CSP

NOTE:

The above specifications are typical value unless otherwise specified.

5. Functional Overview

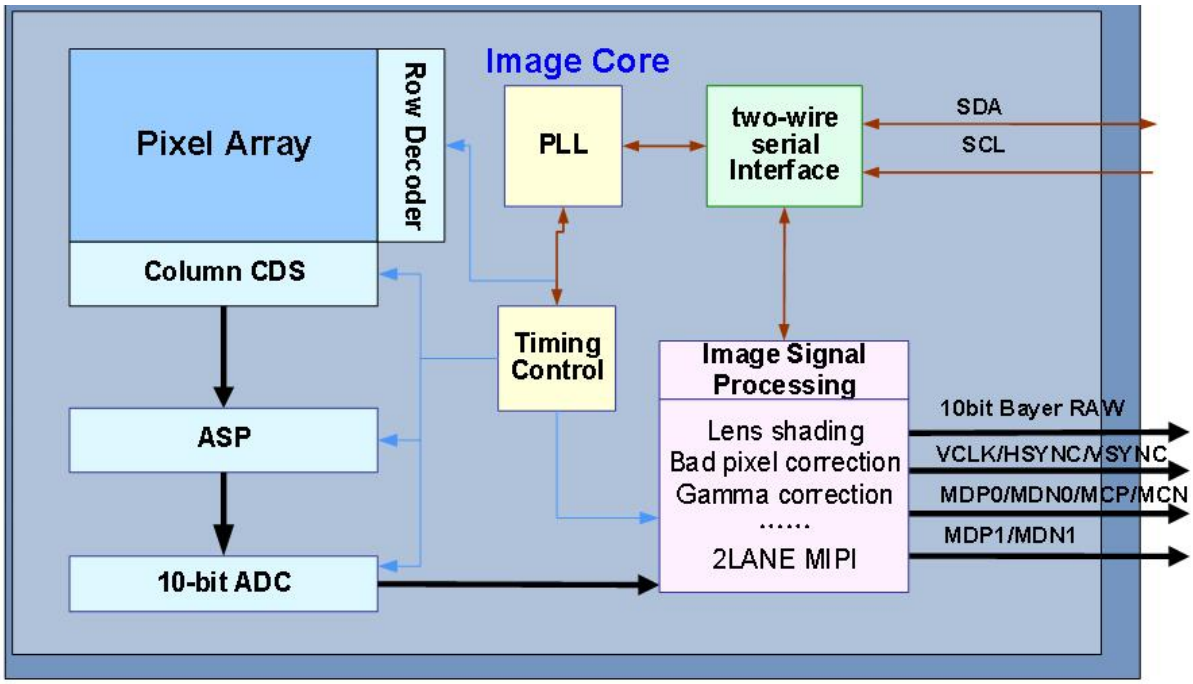


Figure 1.Block Diagram

BF314FCS-W has an active image array of 1280X800 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are

adopted. The analog signal is transferred to digital signal by A/D converter. The digital signals are controlled by Sensor control Block, including Exposure control, Gain control, Test pattern, Image size control and so on.

BF314FCS-W has on-chip PLL, it can be used by two-wire serial interface bus setting.

5.1 Pixel Array

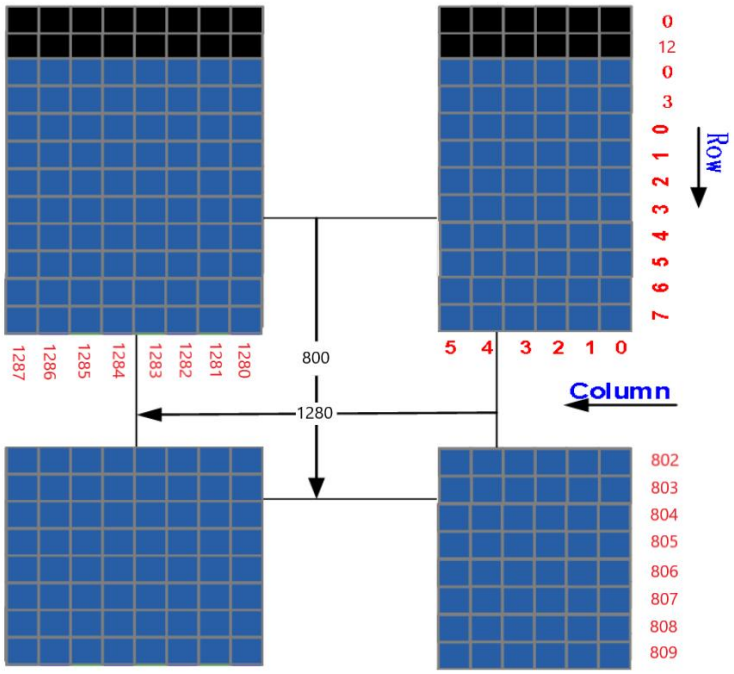


Figure 2.Sensor Array Region

The pixel array includes 1280×800 effective pixels for imaging, in order to improve the image uniformity, there are extra dummy rows and dummy columns around active array. And dark rows at the top side are for black level control.

BF314FCS-W can provide the Raw Bayer data through an 10-bit output data bus.

5.2 Column CDS

BF314FCS-W has column/row driver circuits to read out the pixel data progressively. The CDS (Correlated Double Sampling) circuit reduces temporal noise and pixel level FPN (Fixed Pattern Noise). The unique patented column buffer and ASP (Analog Signal Processing) circuit remove column level FPN caused by various sources of manufacturing process variations.

5.3 Sensor control

- Array control and frame generation

- Internal timing signal generation and distribution
- Exposure control, Gain control, Test pattern
- Image size control
- Frame rate timing
- External timing outputs (VSYNC, HSYNC and PCLK)

Table 1. Registers for Sensor_control

Address	Name	Width	Default value	Description
P0:0x01	***SC_CNTL1***	8	0xc2	Bit[7]: FRAME line select; Bit[6]: 1'b1: VBLANK update netx frame; 1'b0: VBLANK update netx 2 frame; Bit[5]: 1'b1: GLB_GAIN_IN no delay; 1'b0: GLB_GAIN_IN delay one frame; Bit[4]: Control the VSYNC of MIPI; Bit[3]: Soft power on pixel array reset again; Bit[2:0]: Control the delay of HSYNCE to HREF_DAT 3'b000: Delay 0 pclk; 3'b001: Delay 1 pclk; 3'b010: Delay 2 pclk; 3'b011: Delay 3 pclk; 3'b100: Delay 4 pclk; 3'b101: Delay 5 pclk; 3'b110: Delay 6 pclk; 3'b111: Delay 7 pclk;
P0:0x02	***SC_CNTL2***	8	0x42	Bit[7]: 1'b1: Pixel array reset interval also reset operate; 1'b0: Pixel array reset interval do nothing; Bit[6]: 1'b1: Reset interval address is 648; 1'b0: Reset interval address is 649; Bit[5]: 1'b1: READEN signal controlled by bit[7] of 34h; 1'b0: READEN signal will be a pulse; Bit[4]: 1'b1: CLAMP_EN signal always be 0; 1'b0: CLAMP_EN will be a pulse; Bit[3]: 1'b1: GTX signal always be 0; 1'b0: GTX will be a pulse; Bit[2]: 1'b1: MN test mode on; 1'b0: MN test mode off; Bit[1:0]: 2'b00: GGRST signal always 0; 2'b01: GGRST signal in short pulse mode; 2'b10: GGRST signal in long pulse mode; 2'b11: GGRST signal always 1;
P0:0x03	***SC_CNTL3***	8	0x02	Bit[7:6]: 2'b0X: GTXS signal in pulse mode; 2'b10: GTXS signal always 0; 2'b11: GTXS signal always 1; Bit[5:3]: Reserved; Bit[2:0]: GGRST signal length value;

Address	Name	Width	Default value	Description
P0:0x05	***SC_CNTL5***	8	0x40	Bit[7:6]: Reserved; Bit[5]: 1'b1: Dual sync delay counter operation mode on; 1'b0: Dual sync delay counter operation mode off; Bit[4]: FSIN signal edge mode control; Bit[3]: 1'b0: Master sync mode; 1'b1: Slave sync mode; Bit[2]: 1'b1: Dynamic mismatch sync mode on; 1'b0: Dynamic mismatch sync mode off; Bit[1:0]: Dual sync offset;
P0:0x06	***SC_CNTL6***	8	0x82	Bit[7]: 1'b0: Low Frame Rate Streaming Mode off; 1'b1: Low Frame Rate Streaming Mode on; Bit[6]: 1'b0: LED mode1:led start fix; 1'b1: LED mode2:led start with int time; Bit[5]: 1'b0: BINNING disable; 1'b1: BINNING enable; Bit[4]: 1'b0: Mode 1 Digital and analog mix mode; 1'b1: Mode 2 Black and white mode; Bit[3:2]: 2'b00: Led out model1; 2'b01: Led out model2; 2'b10: Led out model3; Bit[1]: 1'b0: Window disable; 1'b1: Window enable; Bit[0]: 1'b0: Group disable; 1'b1: Group enable;
P0:0x07	***VBLANK_MIN[7:0]***	8	0x00	Dummy line low 8 Bits;
P0:0x08	***VBLANK_MIN[15:8]***	8	0x00	Dummy line high 8 Bits;
P0:0x09	***HSYST***	8	0x20	Control the rising edged of HSYNC,HSYNC rising edge low 8 Bits;
P0:0x0a	***HSYEN***	8	0x14	Control the falling edged of HSYNC,HSYNC falling edge low 8 Bits;
P0:0x0b	***H_HSYNC_EDGE***	8	0x03	Bit[7:4]: HSYNC rising edge[11:8]; Bit[3:0]: HSYNC falling edge[11:8];
P0:0x0c	***LINE_LREG***	8	0x39	LINE_LENGTH[7:0];
P0:0x0d	***LINE_HREG***	4	0x03	LINE_LENGTH[11:8];
P0:0x22	***FRAME_LENGTH_OUT [7:0]***	8	0x52	Bit[7:0] :FRAME_LENGTH_DEFAULT[7:0];
P0:0x23	***FRAME_LENGTH_OUT [15:8}***	8	0x03	Bit[7:0] :FRAME_LENGTH_DEFAULT[15:8];

5.4 A/D converter

The analog signals are converted to digital forms one line at a time and data are streamed out column by column. BF314FCS-W provides the 10-bit Raw Bayer data through an internal 10-bit data bus.

5.5 Automatic Black Control

The automatic black level control calculates the data of the dark row and controls the lowest black level for output image data.

Table 2. Registers for ABLC

Address	Name	Width	Default value	Description
P0:0x60	***AVER_E0***	8	RO	Read out black aver for E row E col,this value has been adjusted;
P0:0x61	***AVER_O0***	8	RO	Read out black aver for E row O col,this value has been adjusted;
P0:0x62	***AVER_E1***	8	RO	Read out black aver for O row E col,this value has been adjusted;
P0:0x63	***AVER_O1***	8	RO	Read out black aver for O row O col,this value has been adjusted;
P0:0x64	***AVER_E0[9:8]*** ***AVER_O0[9:8]*** ***AVER_E1[9:8]*** ***AVER_O1[9:8]***	8	RO	Bit[7:6]: Read out black level for even col and even row; Bit[5:4]: Read out black level for odd col and even row; Bit[3:2]: Read out black level for even col and odd row; Bit[1:0]: Read out black level for odd col and odd row;
P0:0x65	***AVER_E0[10]*** ***AVER_O0[10]*** ***AVER_E1[10]*** ***AVER_O1[10]*** ***DARKE0_AVER[10]*** ***DARKO0_AVER[10]*** ***DARKE1_AVER[10]*** ***DARKO1_AVER[10]***	8	RO	Bit[7]: Read out black level for even col and even row; Bit[6]: Read out black level for odd col and even row; Bit[5]: Read out black level for even col and odd row; Bit[4]: Read out black level for odd col and odd row; Bit[3]: Current frame BLC value for E row E col; Bit[2]: Current frame BLC value for E row O col; Bit[1]: Current frame BLC value for O row E col; Bit[0]: Current frame BLC value for O row O col;
P0:0x66	***DARKE0_AVER[9:8]*** ***DARKO0_AVER[9:8]*** ***DARKE1_AVER[9:8]*** ***DARKO1_AVER[9:8]***	8	RO	Bit[7:6]: Current frame BLC value for E row E col; Bit[5:4]: Current frame BLC value for E row O col; Bit[3:2]: Current frame BLC value for O row E col; Bit[1:0]: Current frame BLC value for O row O col;
P0:0x67	***DARKE0_AVER***	8	RO	Current frame BLC value for E row E col;
P0:0x68	***DARKO0_AVER***	8	RO	Current frame BLC value for E row O col;
P0:0x69	***DARKE1_AVER***	8	RO	Current frame BLC value for O row E col;
P0:0x6a	***DARKO1_AVER***	8	RO	Current frame BLC value for O row O col;
P0:0x6b	***AVER_TAR_E0***	8	0x00	Black level target for E row E col;
P0:0x6c	***AVER_TAR_O0***	8	0x00	Black level target for E row O col;
P0:0x6d	***AVER_TAR_E1***	8	0x00	Black level target for O row E col;
P0:0x6e	***AVER_TAR_O1***	8	0x00	Black level target for O row O col;
P0:0x6f	***AVER_TAR_E0[9:8]*** ***AVER_TAR_O0[9:8]*** ***AVER_TAR_E1[9:8]*** ***AVER_TAR_O1[9:8]***	8	0x00	Bit[7:6]: Black level target for even col and even row; Bit[5:4]: Black level target for odd col and even row; Bit[3:2]: Black level target for even col and odd row; Bit[1:0]: Black level target for odd col and odd row;
P0:0x70	***COEF***	8	0x80	Black aver adjust coef;

Address	Name	Width	Default value	Description
P0:0x71	***MODE_CNTL***	8	0x23	Bit[7]: BYPASS_BC 1'b1: Bypass digital black cntl; 1'b0: Don't bypass digital black cntl; Bit[5:4]: DARKROW_SEL 2'b00: Select 1~8 of the 8 dark rows; 2'b01: Select 1~4 of the 8 dark rows; 2'b10: Select 3~6 of the 8 dark rows; 2'b11: Select 5~8 of the 8 dark rows; Bit[3]: DGAD_MODE 1'b1: Use this frame black level as AVER; 1'b0: Use last frame black level variety 1 as AVER; Bit[1]: MODE_CTL 1'b1: Auto; 1'b0: Manual; Bit[0]: DIG_MODE_CTL 1'b1: When the black aver is adjust inside the lock, then adjust one more step; 1'b0: When the black aver is adjust inside the lock ,then keep the value;
P0:0x72	***MODE_CNTL1***	8	0x1e	Bit[7]: SINGLE_PATH_EN:four channels use same value as one of them 1'b1: Enable; 1'b0: Disable; Bit[6:5]: SINGLE_PATH_SEL 2'b00: Four channels use E row E co value; 2'b01: Four channels use E row O co value; 2'b10: Four channels use O row E co value; 2'b11: Four channels use O row O co value; Bit[4]: LAST_EN: Remove single bad pixel 1'b1: Enable; 1'b0: Disable; Bit[3]: SINGLE_FILT_EN :use single frame filt before multiframe 1'b1: Enable; 1'b0: Disable; Bit[2]: BW_MODE_EN :black and white mode 1'b1: Use the aver of four channels; 1'b0: Use each of the four channel values; Bit[1]: MUL_FRAME_EN 1'b1: Use multiframe black level average as AVER; 1'b0: Use current frame black level as AVER;
P0:0x73	***AVER_LOCK***	8	0x21	Bit[7:4]: Lock value to update with current frame black level; Bit[3:0]: Lock value to update with previous frame black level +1 / -1;
P0:0x74	***AVER_LOCK_SUB***	2	0x00	Bit[7]:AVER_LOCK1:{AVER_LOCK[7:4],AVER_LOCK_SUB[1],1'b0}; Bit[6]: AVER_LOCK2:{AVER_LOCK[3:0],AVER_LOCK_SUB[0]};

Address	Name	Width	Default value	Description
P0:0x75	***FRAME_AVER_TH***	8	0x10	Used as black level update threshold when multi frame is enable;

5.6 Lens Shading Correction

BF314FCS-W provides Lens Shading Correction to adjust images.The main purpose of this function is to compensate for lens imperfection. Each pixel has different compensate gains.

Table 3. Registers for LSC

Address	Name	Width	Default value	Description
P0:0x88	***OFFSET_REG***	8	0x00	Lens shading offset selection; Bit[7:0]: Offset value;
P0:0x89	***LENS_CTR1***	8	0xc5	Bit[7]: VFLIP mode control; Bit[6]: HFLIP mode control; Bit[3:2]: Center Y coordinate MSB; Bit[1:0]: Center X coordinate MSB;
P0:0x8a	***y0l_r***	8	0x94	Center Y coordinate LSB;
P0:0x8b	***x0l_r***	8	0x42	Center X coordinate LSB;
P0:0x8c	***R_COEF***	8	0x50	Lens shading gain of R;
P0:0x8d	***G_COEF***	8	0x50	Lens shading gain of G1;
P0:0x8e	***B_COEF***	8	0x50	Lens shading gain of B;
P0:0x8f	***G0_COEF***	8	0x50	Lens shading gain of G0;

5.7 Gamma Correction

BF314FCS-W provides Gamma Correction to adjust images.It is used for compensate the non-linear of sensor.

Table 4. Registers for GMC

Address	Name	Width	Default value	Description
P0:0xb0	***k0***	8	0x80	Gamma correction slope coefficients 0;
P0:0xb1	***k1***	8	0x70	Gamma correction slope coefficients 1;
P0:0xb2	***k2***	8	0x64	Gamma correction slope coefficients 2;
P0:0xb3	***k3***	8	0x54	Gamma correction slope coefficients 3;
P0:0xb4	***k4***	8	0x4a	Gamma correction slope coefficients 4;
P0:0xb5	***k5***	8	0x42	Gamma correction slope coefficients 5;
P0:0xb6	***k6***	7	0x3c	Gamma correction slope coefficients 6;
P0:0xb7	***k7***	7	0x36	Gamma correction slope coefficients 7;
P0:0xb8	***k8***	7	0x32	Gamma correction slope coefficients 8;
P0:0xb9	***k9***	7	0x2e	Gamma correction slope coefficients 9;

Address	Name	Width	Default value	Description
P0:0xba	***k10***	7	0x2a	Gamma correction slope coefficients 10;
P0:0xbb	***k11***	7	0x28	Gamma correction slope coefficients 11;
P0:0xbc	***k12***	7	0x24	Gamma correction slope coefficients 12;
P0:0xbd	***k13***	7	0x22	Gamma correction slope coefficients 13;
P0:0xbe	***k14***	7	0x20	Gamma correction slope coefficients 14;
P0:0xc2	***COEF_SEL*** ***OFFSET_ME***	7	0x00	Bit[7]: COEF_SEL 1'b0:Normal; 1'b1:BW mode; Bit[6:0]: The manual written gamma offset;

5.8 Test pattern mode

BF314FCS-W provides a test pattern mode to output different fixed images.

Table 5. Registers for TP

Address	Name	Width	Default value	Description
P0:0x80	***TEST_MODE***	8	0x00	Bit[7]: Test mode enable; Bit:[6:5]: 2'b00: Color bar pattern; 2'b01: Gradual pattern; 2'b10: Manual write R/G/B; Bit[4]:1'b0: Vertical pattern; 1'b1: Horizontal pattern; Bit[3:0]: Gradual gray pattern mode control; Bit[3:0]=0h,1h,2h,3h: red; Bit[3:0]=4h,5h,6h,7h: green; Bit[3:0]=8h,9h,ah,bh: blue; Bit[3:0]=ch,dh,eh,fh: gray;
P0:0x81	***MAN_R***	8	0x80	Define R value;
P0:0x82	***MAN_G***	8	0x80	Define G value;
P0:0x83	***MAN_B***	8	0x80	Define B value;

5.9 AEC/AGC

AEC/AGC is adjusted change the image brightness.BF314FCS-W adjusts exposure time by AEC, and it adjusts gain value by AGC. They work together to adjust the image brightness into the range of setting threshold.

Table 6. Registers for AEC/AGC

Address	Name	Width	Default value	Description
P1:0x62	***STEP_NUM***	4	0x06	Bit[7:4]: Reserved; Bit[3:0]: Int_time adjust step every frame;
P1:0x63	***Reserved***	8	0x00	Bit[7:0]: Reserved;
P1:0x64	***DIG_TAR_MEN Y_Tar_DG***	8	0x40	Bit[7]: Digital gain target modify switch 1'b0: Off; 1'b1: On; Bit[6:0]: Digital gain target(Y_Tar_DG*2);
P1:0x65	***Coe_MIN***	8	0x0f	Bit[7:4]: Reserved; Bit[3:0]: The minimum integration time when bright to dark;
P1:0x66	***COM8***	8	0x05	Bit[7]: 1'b1: AE_TAR; 1'b0: AE_TAR_MODIFY (decrease the target brightness based on the number of over exposure pixels); Bit[6]: 1'b0: Digital gain disable; 1'b1: Digital gain enable; Bit[5]: Reserved; Bit[4]: The high Bit of INT_STEP_50; Bit[3]: GLB_GAIN0 written is effective when AGC disable 1'b0: GLB_GAIN0 written disable; 1'b1: GLB_GAIN0 written enable; Bit[2]: 1'b1: AGC Enable; 1'b0: AGC disable; Bit[1]: Group switch; 1'b1: On; 1'b0: Off; Bit[0]: AEC Enable; 1'b0: Disable; 1'b1: Enable;
P1:0x67	***COM1***	8	0x8a	Bit[7]: Reserved; Bit[6]: Minimum STEP control 1'b1: 2 steps; 1'b0: 1 step; Bit[5:4]: WINDOW_SEL center window select 2'b00: ROW*12/16 COL*12/16; 2'b01: ROW*10/16 COL*10/16; 2'b10: ROW*8/16 COL*8/16; 2'b11: ROW*6/16 COL*6/16; Bit[3]: Control the adjustable speed of digital gain 1'b0: Y_DIFF_D[7:1] (1times); 1'b1: Y_DIFF_D (2 times); Bit[2:0]: WEIGHT_SEL 3'b000: 4/8*center+4/8*border; 3'b 001: 5/8*center+3/8*border; 3'b010: 6/8*center+2/8*border; 3'b011: 7/8*center+1/8*border; 1'b100~111: Center 100%;
P1:0x68	***Y_AVER***	8	RO	Bit[7:0]: The Y_aver of the current frame;
P1:0x69	***P_PIXEL_OE***	8	RO	Bit[7:0]: The number of the over exposure pixels used to modify the target brightness and the adjusting speed;
P1:0x6a	***GLB_GAIN0***	8	0x18	Bit[7:0]: GLB_GAIN0 register;
P1:0x6b	***INT_TIM[15:8]***	8	0x00	Bit[7:0]: Real integration time MSB;

Address	Name	Width	Default value	Description
P1:0x6c	***INT_TIM[7:0]***	8	0x72	Bit[7:0]: Real integration time LSB;
P1:0x6d	***DIG_GAIN***	8	0x10	Bit[7:0]: The value of DIG_GAIN;
P1:0x6e	***DIG_GAIN_MAX***	8	0xa4	Bit[7:4]: The smallest value the target brightness can achieve; (AE_TAR_M=AE_TAR*TAR_BASE1[3:0]/16); The smaller TAR_BASE1[3:0] is, the quicker the AE adjusting, to calculate AE_TAR_M; Bit[3:0]: DIG_GAIN_MAX[3:0]*16 as the limit of DIG_GAIN;
P1:0x6f	***AE_TAR1***	8	0x4f	Bit[7]: Reserved; Bit[6:0]: Y target value Actually, {0x04[6:0],1'b0} is used;
P1:0x71	***AE_LOC***	8	0x88	Bit[7:4]: Lock for AEC; Bit[3:0]: Lock for AGC;
P1:0x72	***AE_MODE***	8	0xda	Bit[7]: AE test mode control 1'b1: Normal; 1'b0: Test mode; Bit[6]: 1'b0: AE adjusts every two frames; 1'b1: AE adjusts every frame enable; Bit[5:4]: G_MIN_SLOPE When INT_TIM >INT_MID, gain Coefficients 2'b00: 0; 2'b01: 1; 2'b10: 2; 2'b11: 3; Bit[3:2]: P_OE_SEL (what is P_OE_SEL) 2'b00: /2^15; 2'b01: /2^16; 2'b10: /2^17; 2'b11: /2^18; Bit[1]: Reserved; Bit[0]: AE is adjusted by men, effective when test mode(0x72[7]==1'b0);
P1:0x73	***AE_SPEED***	8	0x00	Bit[7:4]: The speed of adjusting from light to dark; Bit[3:0]: The speed of adjusting from dark to light;
P1:0x74	***INT_MAX_I2C***	8	0x87	Bit[7]: INT_ENABLE:switch for select the speed when AE adjust form bright to dark 1'b1: Fast; 1'b0: Slow.(disable in PAL mode); Bit[6]: Reserved; Bit[5:0]: INT_MAX:the MAX steps of integral time;
P1:0x75	***INT_MID_I2C***	8	0x45	Bit[7:4]: The lock(Bit[7:4]*4) threshold for when the next frame's P_PIXEL_OE is larger than the former frame's P_PIXEL_OE, then update the P_PIXEL_OE value; Bit[3:0]: INT_MID: the integral time when the GLB_MIN begin to become larger in order to adjust the picture more fast;
P1:0x76	***INT_MIN***	8	0x81	Bit[7]: 1'b0: One step is the least integration time(as INT_STEP_60 or INT_STEP_50); 1'b1: INT_MIN is Bit[6:0]. (the minimum integration time will be INT_MIN[6:0] row; Bit[6:0]: INT_MIN;
P1:0x77	***INT_STEP_50***	8	0x72	Bit[7:0]: The low 8 Bits of the minimum integration time for

Address	Name	Width	Default value	Description
				every step to avoid flicker for 50HZ light, Bit[8] is in 0x66[4] (COM8[4]);
P1:0x79	***YAVER_LOCK***	8	0xc0	Bit[7:0]: YAVER_LOCK: threshold for AE adjustment from bright to dark;
P1:0x7a	***DIG_LOCK_TH Y_OV_TH***	8	0x82	Bit[7:4]: DIG_LOCK_TH, lock for DIG_GAIN; Bit[3:0]: Y_OV_TH, When (Y_AVER- AE_TAR) > Y_OV_TH[3 :0]*16, if AE adjusts every frame enabled,it will adjusts every frame;
P1:0x7b	***TAR_BASE0***	8	0x03	Bit[7:4]: (192+Bit[7:4]*4) as threshold to judge one pixel whether to be over exposure pixel; Bit[3:0]: Used to control the start of AE;
P1:0x7c	***TAR_BASE1***	8	0x84	Bit[7:4]: Is used to modify the difference of Y_AVER and modified AE_TAR) . The smaller TAR_BASE1[7:4] is, the slower the AE adjusting; Bit[3:0]: It is set to limit the speed of AE to avoid over adjusting. The bigger the value, the quicker the AE adjusting;
P1:0x7d	***YBRIGHT_TH***	8	0xb5	Bit[7:4]: The speed of AE to adjust from dark to bright. The bigger the value, the quicker the AE adjusting; Bit[3:0]: YBRIGHT_TH[3:0] *16 as the threshold for Y_AVER to judge outdoor scene;
P1:0x7e	***INT_TIM_TH***	8	0x50	Bit[7:0]: Threshold for INT_TIME to judge outdoor scene;
P1:0x7f	***GAIN_ALL***	8	RO	GAIN_ALL=GLOBE_GAIN*DIG_GAIN;
P1:0x80	***Gain_OR_Last[7 :0]***	8	0x18	Bit[7:0]: The value of gain_or_last to get the GLB_GAIN0 through some operation;
P1:0x81	***GLB_MIND1***	8	0x18	Bit[7:0]: GLB_MIN1 8 Bits;
P1:0x82	***GLB_MAXD1***	8	0x4b	Bit[7:0]: GLB_MAX1 8 Bits;
P1:0x83	***GLB_MIND2***	8	0x4b	Bit[7:0]: GLB_MIN2 8 Bits;
P1:0x84	***GLB_MAXD2***	8	0x6b	Bit[7:0]: GLB_MAX2 8 Bits;
P1:0x85	***GLB_MAXD3***	8	0xff	Bit[7:0]: GLB_MAX3 8 Bits;

5.10 MIPI

BF314FCS-W provides mobile industry processor interface(MIPI).Sensor supports 1-2 lanes to transfer 8/10 bit image data.

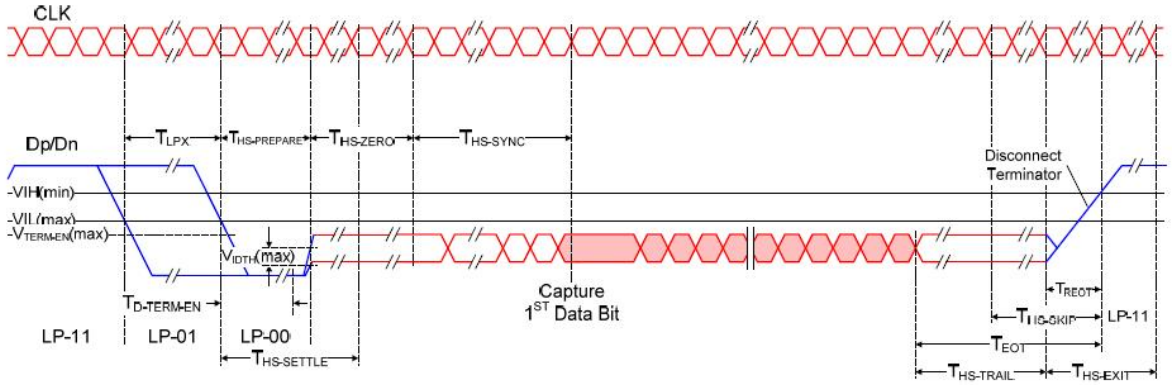


Figure 3.High-Speed Data Transmission in Bursts

Table 7. Registers for MIPI_control

Address	Name	Width	Default value	Description
P1:0x00	***D_LPX***	4	0x08	Bit[7:4]: Reserved; Bit[3:0]: The length of LPX;
P1:0x01	***HS_PREPARE***	5	0x07	Bit[7:5]: Reserved; Bit[4:0]: The length of HS_PREPARE;
P1:0x02	***HS_ZERO***	5	0x16	Bit[7:5]: Reserved; Bit[4:0]: The length of HS_ZERO;
P1:0x03	***HS_TRAIL***	5	0x09	Bit[7:5]: Reserved; Bit[4:0]: The length of HS_TRAIL;
P1:0x04	***Clk_LPX***	4	0x08	Bit[7:4]: Reserved; Bit[3:0]: The length of Clk_LPX;
P1:0x05	***Clk_PREPARE***	5	0x06	Bit[7:5]: Reserved; Bit[4:0]: The length of Clk_PREPARE;
P1:0x06	***Clk_ZERO***	6	0x30	Bit[7:6]: Reserved; Bit[5:0]: The length of Clk_ZERO;
P1:0x07	***Clk_PRE***	4	0x02	Bit[7:4]: Reserved; Bit[3:0]: The length of Clk_PRE;
P1:0x08	***Clk_POST***	6	0x10	Bit[7:6]: Reserved; Bit[5:0]: The length of Clk_POST;
P1:0x09	***Clk_TRAIL***	4	0x0a	Bit[7:4]: Reserved; Bit[3:0]: The length of Clk_TRAIL;
P1:0x0a	***VC*** ***image_type***	8	0x2b	Bit[7:6]: VC, Virtual Channel Identifier 2'b01: 2-Lane system; 2'b00: 1-Lane system; Bit[5:0]: Image_type 0x00–0x07: Synchronization Short Packet Data; Type Codes: 0x00: Frame Start Code; 0x01: Frame End Code; 0x02: Line Start Code (Optional); 0x03: Line End Code (Optional); 0x04–0x07: Reserved; 0x08–0x0F: Generic Short Packet Data Type Codes; 0x28–0x2F: RAW Data; 0x2A: RAW8; 0x2B: RAW10; 0x30–0x37: User Defined Byte-based Data; 0x30–0x33: User Defined 8-bit Data Type 1~4; 0x34–0x37: Reserved; 0x38–0x3F: Reserved;
P1:0x0b	***frame_num_max_H***	8	0x00	High Byte of Max Frame_Counter of Frame Sync Short Packet;
P1:0x0c	***frame_num_max_L***	8	0x00	Low Byte of Max Frame_Counter of Frame Sync Short Packet;
P1:0x0d	***ECC_CNTL***	8	0x1f	Bit[7:5]: Control the ECC Generation

Address	Name	Width	Default value	Description
	EN_MIPI_CLK Dat_Lane_en2 Dat_Lane_en1 CLk_Lane_en Clk_Switch			3'b000: {WC,DI} ; 3'b001: {WC[7:0],WC[15:8],DI}; 3'b010: {DI,WC} ; 3'b011: {DI,WC[7:0],WC[15:8]}; 3'b100: {WC[0:15],DI[0:7]} ; 3'b101: {WC[0:7],WC[8:15],DI[0:7]}; 3'b110: {DI[0:7],WC[0:15]} ; 3'b111: {DI[0:7],WC[8:15],WC[0:7]}; Bit[4]: 1'b1: MIPI enable; 1'b0: MIPI disable; Bit[3]: Reserved; Bit[2]: 1'b1: Data lane 1 enable; 1'b0: Data lane disable; Bit[1]: 1'b1: Clock lane enable; 1'b0: Data lane disable; Bit[0]: 1'b0: Continuous clock mode; 1'b1: Non-continuous clock mode;
P1:0x0e	***MIPI_2LANE_EN FIX_data_EN Lane_change EN_Bit10 Line_SP_sel Line_cnt_en frame_cnt_en Vsync_sel***	7	0x90	Bit[7]: 1'b1: 2-Lane system; 1'b0: 1-Lane system; Bit[6]: 1'b1: Fix data output,the fix data is FIX_data; 1'b0: Normal data output; Bit[5]: Reserved; Bit[4]: Raw10 enable 1'b1: The data is raw10; 1'b0: The data is raw8; Bit[3]: 1'b1: LS and LE will be output ; 1'b0: LS and LE didn't be output; Bit[2]: 1'b0: WC in LS and LE is always 0; 1'b1: WC in LS and LE isn't 0; Bit[1]: 1'b0: WC in FS and FE is always 0; 1'b1: WC in FS and FE isn't 0; Bit[0]: 1'b0: VSYNC_IMAGE is be packed; 1'b1: VSYNC_DAT is be packed;
P1:0x0f	***Continue_HS_E N CLK_ULPS_EN DAT_ULPS_EN1 EM_LP_length***	8	0x08	Bit[7]: 1'b1: Between line and line,frame and frame, the state of the DP and DN is HS; 1'b0: Between line and line,frame and frame, the state of the DP and DN is LP; Bit[6]: 1'b1: Enable clock lane ULPS state; 1'b0: Disable clock lane ULPS state; Bit[5]: Reserved; Bit[4]: 1'b1: Enable data lane 1 ULPS state; 1'b0: Disable data lane 1 ULPS state; Bit[3:0]: The length of each individual LP state period. EM_LP_length > = D_LPX. The mode enter into ULPS mode at this time;
P1:0x10	***FIX_data_H CLK_Lane_DIS_ LP***	8	0x3f	Bit[7:6]: FIX_data[9:8]; Bit[5:4]: When CLk_Lane_en=1, CLK_LP=CLK_Lane_DIS_LP;

Address	Name	Width	Default value	Description
	Dat_Lane2_DIS_LP ***Dat_Lane1_DIS_LP***			Bit[3:2]: When Dat_Lane_en1=1, LANE2_LP=Dat_Lane2_DIS_LP; Bit[1:0]: When Dat_Lane_en1=1, LANE1_LP=Dat_Lane1_DIS_LP;
P1:0x11	***FIX_data_L***	8	0x00	Bit[7:0]: FIX_data[7:0];
P1:0x12	***MASK_1ST_EN***	4	0x01	Bit[5]: 1'b1: LANE test mode off; 1'b0: LANE test mode on; Bit[3]: 1'b1: SRAM test mode on; 1'b0: SRAM test mode off; Bit[2]: 1'b1: When softpowerup transmission start with LP state; 1'b0: When softpowerup transmission start with HS state; Bit[1]: 1'b1: Disable SRAM; 1'b0: Enable SRAM; Bit[0]: 1'b1: Normal; 1'b0: Mask 1ST Frame ;
P1:0x13	***SRAM_CNTL***	5	0x00	Bit[4:1]: MS; Bit[0]: MSE ;

5.11 Trigger mode

Trigger signal can be controlled by input PAD or internal registers. When the signal occurs from 0 to 1,BF314FCS-W starts to exposure. Image data output starts after exposure time setting by INT_TIM registers. The trigger signal must be a pulse and the minimum width is 4 master clock periods. For any one pulse,BF314FCS-W can output N<16 frames setting by registers.

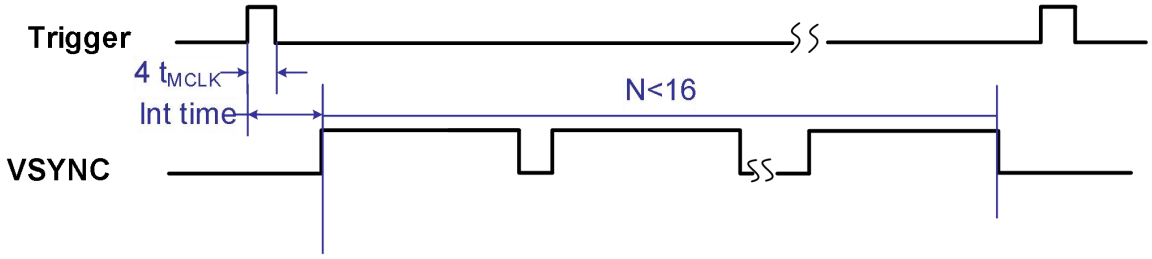


Figure 4.output with trigger mode

Table 8. Registers for Trigger_control

Address	Name	Width	Default value	Description

Address	Name	Width	Default value	Description
P0:0x04	***SC_CNTL4***	8	0x81	Bit[7]: 1'b1: TRIGGER mode enable; 1'b0: TRIGGER mode disable; Bit[6]: 1'b1: Master TRIGGER mode; 1'b0: Slave TRIGGER mode; Bit[5]: The trigger register in TRIGGER mode; Bit[4]: 1'b1: Master TRIGGER mode ,trigger by pin; 1'b0: Slave TRIGGER mode enable,trigger by register; Bit[3:0]: Output frame number in TRIGGER mode;

5.12 Flash control

LED_STB_OFFSET register is used for controlling the LED signal. When internal exposure started,LED signal will occur from 0 to 1,it can be adjusted by delay time changed.When the integration time end,LED signal will occur from 1 to 0.

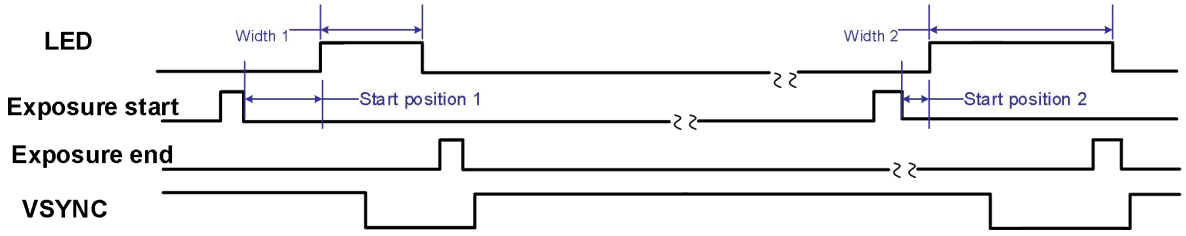


Figure 5.LED/FLASH control mode

Table 9. Registers for LED_control

Address	Name	Width	Default value	Descriptions
P0:0x2b	***STROBE_OFFSET***	8	0x00	Control the offset of LED signal;
P0:0x49	***LED_FMST_HSB*** ***INTVL***	8	0x01	Bit[7:4]: LED_FMST high 4 bits; Bit[3:0]: INTVL;
P0:0x4a	***LED_FMST_LSB***	8	0x20	LED_FMST low 8 bits;

5.13 Serial/Overlap

BF314FCS-W includes serial output mode and overlap mode controlled by P0:0x02[7], it has different integration time control and output position.

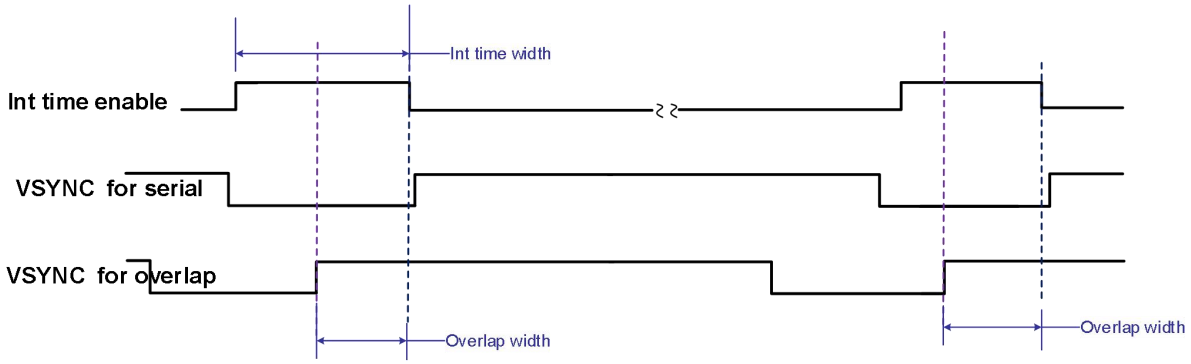


Figure 6.different VSYNC output mode

5.14 Output mode

BF314FCS-W can output different size and different image data.

Table 10. Registers for Output_control

Address	Name	Width	Default value	Description
P0:0xc8	***REG_C8***	4	0x08	Bit[3]: BIT0_EN, control input data bit0 1'b1: Dark data; 1'b0: Original data; Bit[2]: Reserved; Bit[1]: UV_MODE, control CB/CR data 1'b1: The same as Y; 1'b0: Original CB/CR; Bit[0]: RAW0_EN,raw data output enable 1'b1: Enable; 1'b0: Disable;
P0:0xc9h	***REG_C9***	8	0x00	Bit[7]: DAT_MODE 1'b0: Output normal dat; 1'b1: Output fixed value: dat=dat_VAL,dat=dat_VAL; Assign DATA_VALU = COM4[6]; Bit[6]: Fixed value of output DATA If DAT_MODE=1&DATA_VALU=0,output DATA_VALU=0; If DAT_MODE=1&DATA_VALU=1,output DATA_VALU=1; Else, data output normal mode; Bit[5]:1'b0: Output normal HSYNC/VSYNC; 1'b1: Output fixed value: HSYNC=HSYNC_VAL,VSYNC=VSYNC_VAL; Bit[4]: Reserved; Bit[3]: Output HSYNC selection 1'b1: HSYNC; 1'b0: HREF; Bit[2]: the polarity of HREF 1'b1: Active low; 1'b0: Active high; Bit[1]: The polarity of VSYNC 1'b1: Active low; 1'b0: Active high; Bit[0]: The polarity of HSYNC 1'b1: Active low; 1'b0: Active high;

Address	Name	Width	Default value	Description
P0:0xcah	***HSTART***	8	0x00	Bit[7:0]: Output Format-Horizontal Frame (HREF column) start high 8-bit(low 2bits are at VHREF[1:0]);
P0:0xcbh	***HSTOP***	8	0xa0	Bit[7:0]: Output Format-Horizontal Frame (HREF column) end high 8-bit (low 2 bits are at VHREF[3:2]);
P0:0xcch	***VSTART***	8	0x00	Bit[7:0]: Output Format-Vertical Frame (row) start high 8-Bit (low 2 bits are at VHREF[5:4]);
P0:0xcdh	***VSTOP***	8	0xb4	Bit[7:0]: Output Format-Vertical Frame (row) end high 8-Bit (low 2 bits are at VHREF[7:6]);
P0:0xceh	***VHREF***	8	0x00	Bit[7:6]: VREF end low 2 bits (high 8 bits at VSTOP[7:0]); Bit[5:4]: VREF start low 2 bits (high 8 bits at VSTART[7:0]); Bit[3:2]: HREF end low 2 bits (high 8 bits at HSTOP[7:0]); Bit[1:0]: HREF start low 2 bits (high 8 bits at HSTART[7:0]);
P0:0xcfh	***REG_CF***	8	0x10	Bit[7:6]:YUV_ORDER_SELECT 2'b00:YCYC; 2'b11:CYCY; Bit[5]: DARK_ROW_OUTPUT 1'b1: Enable; 1'b0: Disable; Bit[4]: VSYNC output selection 1'b1: VSYNC_DAT; 1'b0: VSYNC_IMAGE ; Bit[3]: HREF_MODE 1'b0: No href when vsync_dat=0; 1'b1: Always has href no matter vsync_dat=0 or not; Bit[2]: CROSS_CTL 1'b0: Output 8'h00 during hblank; 1'b1: Output normally during hblank; Bit[1]: AE_OP_MARK,symbol for bright pixels; Bit[0]: Reserved;
P0:0xd0h	***REG_D0***	8	0x00	Bit[7]: Reserved; Bit[6]: Negative Pixel 1'b0: Normal; 1'b1: Enable negative pixel; Bit[5]: Signed Pixel 1'b0: Normal; 1'b1: Enable signed pixel (When the pixel's Y_AVER > 128); Bit[4]: Reserved; Bit[3:0]: Skip frame counter; If FRAME_CNT_REG=0,skip no frame;
P0:0xd1h	***MANU***	8	0x80	Bit[7:0]: Manual U value (Effectively only when register COM10 [2] is high);
P0:0xd2h	***MANV***	8	0x80	Bit[7:0]: Manual V value (Effectively only when register COM10[2] is high);

6. Specifications

6.1 Electrical Characteristics

6.1.1 Absolute Maximum Ratings

- Supply voltage (VDDIO): 1.7 ~ 3.5 V
- Supply voltage (VDDD): 1.45 ~ 1.55 V
- Supply voltage (VDD3A): 3.1~ 3.5 V
- Operating temperature: -20~70℃
- ESD Rating, Human Body mode: 3000 V

Caution: Stresses exceeding the absolute maximum ratings may induce failure.

6.1.2 DC Parameters

Table 11.DC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
VDDIO	I/O power supply	V	1.7	3.3	3.5	1
VDDD	Digital power supply	V	1.45	1.5	1.55	2
VDD3A	Analog power supply	V	3.1	3.3	3.5	--
Vih	Input voltage logic “1”	V	0.7*VDDIO	--	--	--
Vil	Input voltage logic “0”	V	--	--	0.2*VDDIO	--
Voh	Output voltage logic “1”	V	0.9*VDDIO	--	--	--
Vol	Output voltage logic “0”	V	--	--	0.1*VDDIO	--
I_vddio	VDDIO supply current, normal operation mode	mA	0.1	22	--	2
I_vddd	VDDD supply current,	mA	-- --	30	70	2
I_vdd3a	VDD3A supply current,	mA	--	30	--	2

Note：

1. VDDIO=3.3V default or VDDIO=1.8V
2. The current of VDDD and VDDIO will have different value in MIPI mode and parallel mode,the current of power is decided by the work mode, ex. Frequency of clock and output format. The maximum current will not appear at the same time.

6.1.3 Clock Requirement

Table 12.AC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
XCLK	External clock frequency	MHz	--	6~27	--	1
PCLK	Master clock	MHz	--	42M@30fps 84M@60fps 168M@120fps MIPI	--	2
SCL	two-wire serial interface clock frequency	KHz	--	400	--	3

Note:

1. XCLK is the input clock and it is the input of PLL.
2. PCLK is the pixel clock of the system, and it can be generated by PLL.For MIPI output mode,the frequency will be higher.
3. SCL is driven by host processor. For the detail serial bus timing, refer to two-wire serial Interface section.

6.2 Electro-Optical Characteristics

Operating voltage: VDDIO=3.3V,VDD3A=3.3V,VDDD=1.5V

Operating temperature: 25°C

Table 13.Electro-Optical Characteristics

Parameter	Unit	Min.	Typ.	Max.	Notes
Sensitivity	V/Lux·sec	--	TBD		1
Dark current	mV/sec	--	TBD	--	2
S/N ratio	dB	--	TBD	--	--
Dynamic Range	dB	--	TBD	--	--
Frame Rate	fps	--	120	120	3

Notes:

1. With measured at 50 lux green light condition at room temperature.
2. Measured at dark condition for exposure time of 1s (25 Celsius).
3. With 1280×800 window size at PCLK 168MHz for MIPI 2-lane mode.

6.3 Timing

6.3.1 The Sensor-core Readout Mode

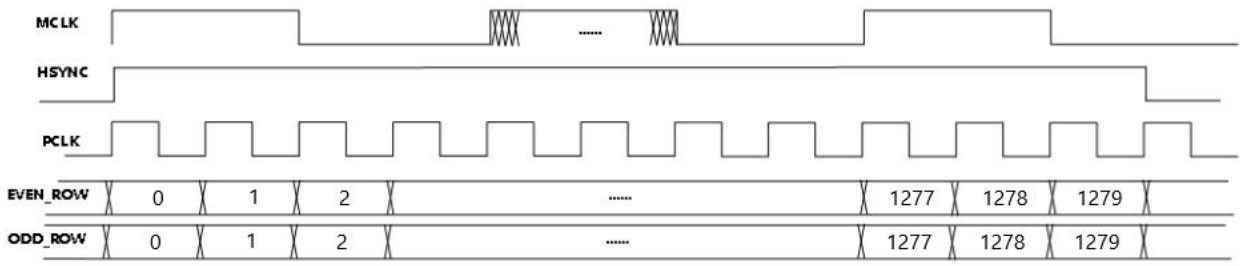


Figure 7.Horizontal Timing Raw Bayer Data

6.3.2 The output Frame Timing

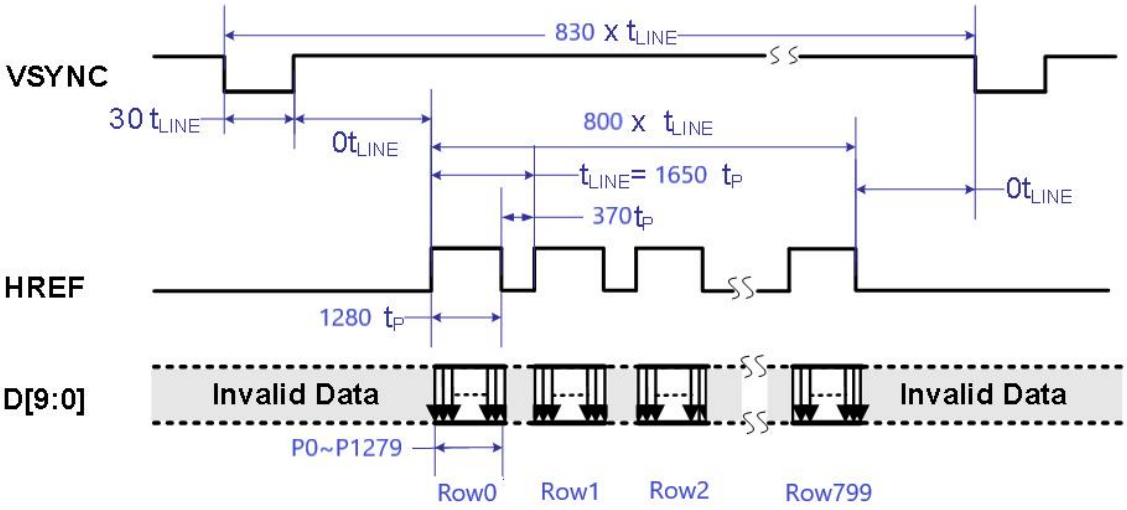


Figure 8.Output Frame Timing

Table 14. AC Characteristics

Symbol	Descriptions	Min.	Typ.	Max.	Unit
t_P	Pixel output clock period	--	11.9	--	ns
f_{PCLK}	Video Clock Frequency f_{VCLK} can be adjusted by PLL	--	84	--	MHz
t_{LINE}	Line length	--	1650x t_P	--	ns

6.4 CRA(Chief Ray Angle linear 26.78°)

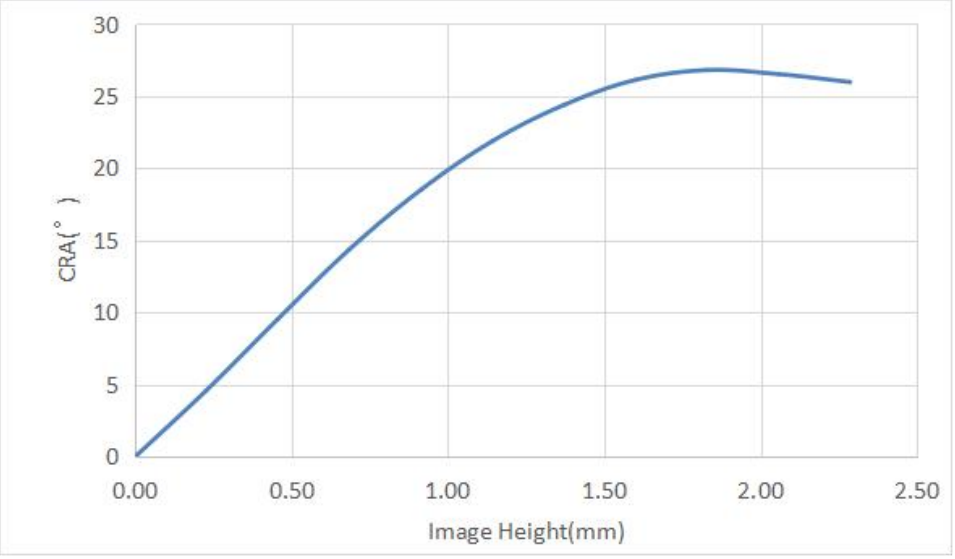


Figure 9. CRA information

Table 15. CRA versus image height plot

Field(%)	Image Height(mm)	CRA(degree)
0.00	0.00	0.00
0.10	0.23	4.58
0.20	0.46	9.56
0.30	0.69	14.38
0.40	0.91	18.50
0.50	1.14	21.87
0.60	1.37	24.37
0.70	1.60	26.10
0.80	1.83	26.78
0.90	2.06	26.50
1.00	2.29	25.95

7. Two-wire serial interface& Register

7.1 Theory of Operation

The registers of BF314FCS-W are written and read through the two-wire serial interface. BF314FCS-W has two-wire serial interface slave. BF314FCS-W is controlled by the two-wire serial interface clock (SCL), which is driven by the two-wire serial interface master. Data is transferred into and

out of BF314FCS-W through the two-wire serial interface data (SDA) line. The SCL and SDA lines are pulled up to VDDIO by a 2kΩ off-chip resistor. Either the slave or the master device can pull the lines down. The two-wire serial interface protocol determines which device is allowed to pull the two lines down at any given time.

Note: Two-wire serial interface device address of BF314FCS-W is 7'b1101110 (0X6e) or 7'b1101111 (0X6f),it can control by input ID_SEL PAD,it doesn't include W/R bit.

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A0 in the LSB of the address indicates write mode, and A1 indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The two-wire serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock: it can only change when the two-wire serial interface clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a write and a 1 indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received.

The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The BF314FCS-W uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit.

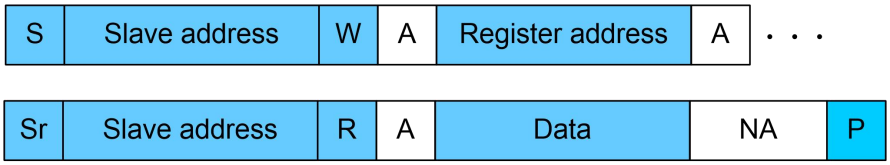
A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

7.2 Two-wire Serial Interface Functional Description

Single Write Mode Operation

Multiple Write Mode (Register address is increased automatically) [1] operation

Single Read Mode Operation



Multiple Read Mode (Register address is increased automatically) [1] Operation

From master to slave From slave to master

S: Start condition. Sr: Repeated Start (Start without preceding stop)

Slave Address: for device address 7'b1101110 (0X6e)

write address = DCh = 11011100b

read address = DDh = 11011101b

Slave Address: for device address 7'b1101111 (0X6f)

write address = DEh = 11011110b

read address = DFh = 11011111b

R/W: Read/Write selection. High = read, LOW = write.

A: Acknowledge bit. NA: No Acknowledge.

Data: 8-bit data P: Stop condition

Note1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

7.3 The Two-wire Serial Interface Timing

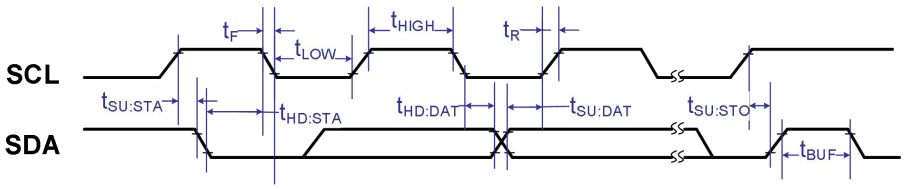


Figure 10.Two-Wire Serial Interface Timing

Table 16.AC Characteristics

Symbol	Descriptions	Min.	Typ.	Max.	Unit
t_R, t_F	two-wire serial interface rise/fall times	--	--	300	ns
t_{LOW}	Clock Low Period	1.3	--	--	us
t_{HIGH}	Clock High Period	600	--	--	ns
$t_{HD:STA}$	Start condition Hold Time	600	--	--	ns
$t_{SU:STA}$	Start condition Setup Time	600	--	--	ns
$t_{HD:DAT}$	Data-in Hold Time	0	--	--	ns
$t_{SU:DAT}$	Data-in Setup Time	100	--	--	ns
$t_{SU:STO}$	Stop condition Setup Time	600	--	--	ns

7.4 Registers for system control

Table 17. BF314FCS-W system control registers

Address	Name	Width	Default value	Description

Address	Name	Width	Default value	Description
P1:0xe0	***REG_CTR0***	8	0x96	Bit[7:6]: Current reserved for VCO MIPI Bit[5:4]: Up down current reserved for VCO MIPI; Bit[3:0]: PLL pre divider select;
P1:0xe1	***REG_CTR1***	8	0xa5	Bit[7:0]: PLL loop divider LSB;
P1:0xe2	***REG_CTR2***	8	0x64	Bit[7:6]: Up down current reserved for VCO AD; Bit[5:4]: Current reserved for VCO AD; Bit[3]: En_ivco; Bit[2]: VCO AD select; Bit[1]: PLL CLK bypass; 1'b0: XCLK input; 1'b1: Normal clock; Bit[0]: PLL loop divider HSB;
P1:0xe3	***REG_CTR3***	8	0x6a	Bit[7:5]: VDDC voltage select V=0.8V+Bit[7:5]; Bit[4:2]: Control bias of CMP 3'b000: 0uA; 3'b001: 1uA; 3'b010: 2uA; 3'b011: 3uA; 3'b100: 4uA; 3'b101: 5uA; 3'b110: 6uA; 3'b111: 7uA; Bit[1]: Counter buffer clock delay select 1'b0: delay 0ns; 1'b1: delay 2ns; Bit[0]: Ramp clock select 1'b0: 1/2 frequency clock; 1'b1: normal clock;
P1:0xe4	***REG_CTR4***	8	0xdd	Bit[7]: VDDP power down 1'b0: Work normal; 1'b1: VDDP=VDD3A; Bit[6:4]: VDDP for pixel voltage select V=2.4V+Bit[6:4]; Bit[3]: VAB power down 1'b0: work normal; 1'b1: VAB=VDD3A; Bit[2:0]: VAB for pixel voltage select V=2.4V+Bit[2:0];
P1:0xe5	***REG_CTR5***	8	0x8b	Bit[7:4]: PCP voltage select 4'b0000: 2.6V; 4'b1000: 3.4V; 4'b0001: 2.7V; 4'b1001: 3.5V; 4'b0010: 2.8V; 4'b1010: 3.6V; 4'b0011: 2.9V; 4'b1011: 3.7V; 4'b0100: 3.0V; 4'b1100: 3.8V; 4'b0101: 3.1V; 4'b1101: 3.9V; 4'b0110: 3.2V; 4'b1110: 3.95V; 4'b0111: 3.3V; 4'b1111: 3.95V; Bit[3:0]: RAMP1 voltage select 4'b0000: 515mV; 4'b1000: 750mV; 4'b0001: 536mV; 4'b1001: 796mV; 4'b0010: 559mV; 4'b1010: 847mV; 4'b0011: 583mV; 4'b1011: 905mV; 4'b0100: 611mV; 4'b1100: 973mV;

Address	Name	Width	Default value	Description
				4'b0101: 640mV; 4'b1101: 1052mV; 4'b0110: 673mV; 4'b1110: 1144mV; 4'b0111: 710mV; 4'b1111: 1255mV;
P1:0xe6	***REG_CTR6***	8	0x11	Bit[7:6]: Test_MUX output select 2'b00: VDDP; 2'b01: VR_CP; 2'b10: VAB; 2'b11: PIXOUT; Bit[5]: Pclk in mipi output select 1'b0: 1/5 divider(MIPI); 1'b1: 1/2 divider; Bit[4:2]: Adjust Vref of LVDS 3'b000: 488.8mV; 3'b001:469.6mV; 3'b010: 449.2mV; 3'b011: 427.8mV; 3'b100: 405.0mV; 3'b101: 380.9mV; 3'b110: 355.3mV; 3'b111: 328.1mV; Bit[1:0]: Reference of LVDS(MIPI LP) 2'b00: 1274mV; 2'b01:1206mV; 2'b10: 1160mV; 2'b11:1115mV;
P1:0xe7	***REG_CTR7***	8	0x4b	Bit[7:4]: NCP0P5 voltage select 4'b0000: -0.1V; 4'b1000: -0.85V; 4'b0001: -0.2V; 4'b1001: -0.9V; 4'b0010: -0.3V; 4'b1010: -0.95V; 4'b0011: -0.4V; 4'b1011: -1.0V; 4'b0100: -0.5V; 4'b1100: -1.05V; 4'b0101: -0.6V; 4'b1101: -1.1V; 4'b0110: -0.7V; 4'b1110: -1.15V; 4'b0111: -0.8V; 4'b1111: -1.2V; Bit[3:0]: NCP1P0 voltage select 4'b0000: -0.1V; 4'b1000: -0.85V; 4'b0001: -0.2V; 4'b1001: -0.9V; 4'b0010: -0.3V; 4'b1010: -0.95V; 4'b0011: -0.4V; 4'b1011: -1.0V; 4'b0100: -0.5V; 4'b1100: -1.05V; 4'b0101: -0.6V; 4'b1101: -1.1V; 4'b0110: -0.7V; 4'b1110: -1.2V; 4'b0111: -0.8V; 4'b1111: -1V;
P1:0xe8	***REG_CTR7***	8	0x40	Bit[7:6]: Osc clk for NCP select; 2'b00: 25M~50M; 2'b01: 33M~66M; 2'b10: 42M~84M; 2'b11: 50M~100M; Bit[5]: PCP ibias power down; 1'b0: Work normal; 1'b1: Power down; Bit[4:2]: Control bias of pixel: 3'b000: 0uA; 3'b001: 1uA; 3'b010: 2uA; 3'b011: 3uA; 3'b100: 4uA; 3'b101: 5uA; 3'b110: 6uA; 3'b111: 7uA;

Address	Name	Width	Default value	Description
				Bit[1:0]: DEC clock delay; 2'b00: Delay 0ns; 2'b01: Delay 2ns; 2'b10: Delay 4ns; 2'b11: Delay 6ns;
P1:0xe9	***REG_CTR9***		0x08	Bit[7:6]: ISP clock delay 2'b00: Delay 0ns; 2'b01: Delay 2ns; 2'b10: Delay 4ns; 2'b11: Delay 6ns; Bit[5]: CLK_CNT clock select 1'b0: Normal clock; 1'b1: 1/2 divider clock; Bit[4]: DEC clock delay 1'b0: Delay 2ns; 1'b1: Delay 0ns; Bit[3]: CLK_system clock select 1'b0: 1/2 divider clock; 1'b1: Normal clock; Bit[2]: Video output clock control: 1'b0: Normal; 1'b1: Inverse; Bit[1:0]: Video output clock delay 2'b00: Delay 0ns; 2'b01: Delay 2ns; 2'b10: Delay 4ns; 2'b11: Delay 6ns;
P1:0xea	***REG_CTRA***		0x35	Bit[7]: Powerdown trigger PAD control 1'b0: PAD normal; 1'b1: Powerdown PAD,(when powerdown PAD,output disable); Bit[6]: Powerdown other output PAD control 1'b0: PAD normal; 1'b1: Powerdown PAD,(when powerdown PAD,output disable); Bit[5]: Trigger select 1'b0: Trigger from FSIN PAD; 1'b1: Trigger from TRIG PAD; Bit[4]: Trigger control 1'b0: TRIGGER output disable; 1'b1: TRIGGER output enable; Bit[3:2]: SD/VCLK output drive capability 2'b00: 4mA; 2'b01: 8mA; 2'b10: 12mA; 2'b11: 16mA; Bit[1]: XCLK_SEL 1'b0: Clock normal; 1'b1: Clk_in with deglitch; Bit[0]: SDA output drive capability 1'b0: 4mA; 1'b1:8mA;

Address	Name	Width	Default value	Description
P1:0xeb	***REG_CTRB***		0x0f	Bit[7]: Powerdown MIPI PLL control 1'b0: PLL normal; 1'b1: Powerdown PLL,(when powerdown PLL,SYSTEM CLOCK=CLKIN); Bit[6]: Powerdown AD PLL control 1'b0: PLL normal; 1'b1: Powerdown PLL,(when powerdown PLL,SYSTEM CLOCK=CLKIN); Bit[5]: Powerdown ncp0 buffer 1'b0: Work normal; 1'b1: Buffer bypass; Bit[4]: Powerdown ncp1 buffer 1'b0: Work normal; 1'b1: Buffer bypass; Bit[3]: Powerdown TEST_MUX control 1'b0: TEST_MUX normal; 1'b1: Powerdown TEST_MUX; Bit[2]: Powerdown PCP control 1'b0: PCP normal; 1'b1: Powerdown PCP,(when powerdown PCP,PCP for TX power is VDD3A); Bit[1]: Powerdown NCP0P5 control 1'b0: NCP0 normal; 1'b1: Powerdown NCP0, (when powerdown NCP1,the groud of TX for global read is VSSA); Bit[0]: Powerdown NCP1p0 control 1'b0: NCP1 normal; 1'b1: Powerdown NCP1,(when powerdown NCP2, the groud of TX for rolling read is VSSA);
P1:0xec	***REG_CTRC***	8	0x00	Bit[7]: NCP clock select 1'b0: Normal; 1'b1:1/2 divider clock; Bit[6]:Ramp gain min select 1'b0: Limit gain; 1'b1: Normal gain; Bit[5:4]: Data1 lane Adjust Rout of LVDS(MIPI) 2'b00: 50ohm; 2'b01: 42ohm; 2'b10: 38ohm; 2'b11: 35ohm; Bit[3:2]: Clock lane Adjust Rout of LVDS(MIPI) 2'b00: 50ohm; 2'b01: 42ohm; 2'b10: 38ohm; 2'b11: 35ohm; Bit[1:0]: Data0 lane Adjust Rout of LVDS(MIPI) 2'b00: 50ohm; 2'b01: 42ohm; 2'b10: 38ohm; 2'b11: 35ohm;

Address	Name	Width	Default value	Description
P1:0xed	***REG_CTRD***	8	0x00	Bit[7]: NCP clock select 1'b0: Normal; 1'b1: Osc clock; Bit[6]:PN module for NCP work enable 1'b0: Disable; 1'b1: Enable; Bit[5:4]: Data1 lane output delay control 2'b00: 0ns; 2'b01: 0.1ns; 2'b10: 0.2ns; 2'b11: 0.3ns; Bit[3:2]: Clock lane output delay control 2'b00: 0ns; 2'b01: 0.1ns; 2'b10: 0.2ns; 2'b11: 0.3ns; Bit[1:0]: Data0 lane output delay control 2'b00: 0ns; 2'b01: 0.1ns; 2'b10: 0.2ns; 2'b11: 0.3ns;
P1:0xee	***REG_CTRE***	8	0x66	Bit[7:4]: PLL pre divider select; Bit[3]: En current for VCO; Bit[2]: VCO select for mipi clock; Bit[1]: PLL mipi post divider select; 1'b0: 1/2 output; 1'b1: Normal output; Bit[0]: RDEC mode control;
P1:0xef	***REG_CTRF***	8	0x42	Bit[7:0]: PLL loop divider LSB;
0xf0	***MODE***	8	0x01	Bit[7]:PLL work mode 1'b0: Controlled by registers; 1'b1: Always work; Bit[6]: System clock control 1'b0: Controlled by PDA; 1'b1: Always work; Bit[5]: Gated clock control 1'b0: normal clock; 1'b1: clock disable; Bit[4]: VSYNC master enable 1'b0: Output enable; 1'b1: Output disable; Bit[3]: System clock mode 1'b0: PLL MIPI; 1'b1: PLL AD; Bit[2:1]: Reserved; Bit[0]: Black and white mode enable 1'b0: Color mode; 1'b1: B/W mode;
0xf1	***ISPBYPS***	8	0x00	Bit[7:3]: Reserved; Bit[2]: Contrast enable 1'b0: Enable; 1'b1: Disable; Bit[1]: Gamma Correction enable 1'b0: Enable; 1'b1: Disable; Bit[0]: Lens Correction enable 1'b0: Enable; 1'b1: Disable;
0xf2	***REGF2***	1	0x00	Bit[7:1]: Reserved; Bit[0]: SCCB reset,register reset 1'b1: On; 1'b0: Off;

Address	Name	Width	Default value	Description
0xf3	***REGF3***	2	0x00	Bit[1]: PDA_SYNC,PDA synchronized by VSYNC_IMAGE; 1'b0: Work normal; 1'b1: Standby mode; Bit[0]: normal PWD 1'b0: Work normal; 1'b1: Standby mode;
0xf4	***HVFLIP***	2	0x00	Bit[1]: Mirror 0: Normal image, 1: Mirror image; Bit[0]: Vertical Flip 0: Normal image, 1: Vertically flip image;
0xfb	***VER_BME***	8	0x00	Bit[7:4]: Reserved; Bit[3:0]: RO;
0xfc	***PIDH_BME***	8	0x31	Bit[7:0]: BME ID;
0xfd	***PIDL_BME***	8	0x4D	Bit[7:0]: BME version;
0xfe	***REGFE***	2	0x00	Bit[7:2]: Reserved; Bit[1:0]: I2C Page selection 2'b00: Page 0; 2'b01: Page 1;

8. Package Dimensions

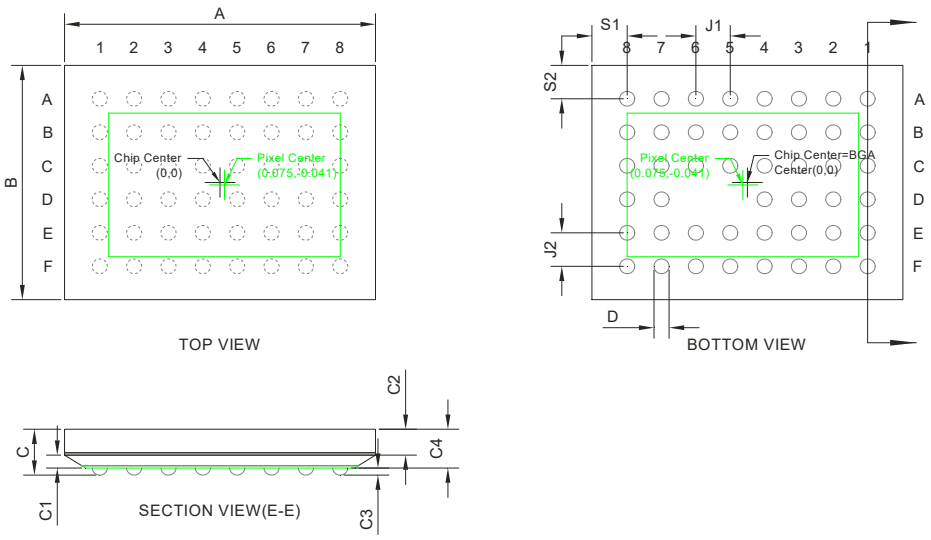


Figure11.CSP dimension description

Table 18.CSP Dimension

Parameter	Symbol	Nominal	Min	Max
		Millimeters		
Package Body Dimension X	A	5. 150	5. 125	5. 175
Package Body Dimension Y	B	3. 975	3. 950	4. 000
Package Height	C	0. 690	0. 635	0. 745
Si Thickness	C1	0. 100	0. 095	0. 105
Thickness from top glass surface to wafer	C2	0. 4325	0. 4225	0. 4425
Ball Height	C3	0. 120	0. 090	0. 150
Package Body Thickness	C4	0. 570	0. 540	0. 600
Ball Diameter	D	0. 250	0. 200	0. 300
Total Ball Count	/	46. 000	\	\
Ball Count X axis	/	8. 000	\	\
Ball Count Yaxis	/	6. 000	\	\
Pins Pitch X axis1	J1	0. 570	0. 560	0. 580
Pins Pitch Y axis2	J2	0. 570	0. 560	0. 580
Edge to Ball Center Distance along X	S1	0. 580	0. 550	0. 610
Edge to Ball Center Distance along Y	S2	0. 5625	0. 5325	0. 5925

Table 19. CSP Pin Descriptions

	1	2	3	4	5	6	7	8
A	VDD3A	VSSA/VSSC	D5	D6	D9	TRIG	VSYNC	VREF
B	VDDD	PDN	HSYNC	D7	D8	VSSD	VDDIO	VSSA/VSSC
C	D4	D3	D0	VDDIO	ID_SEL	LED	VDDD	VDD3A
D	D1	D2	SCL	VDDD	/	/	MEN	VTN0
E	VDDD	VDDIO	PCLK	MDP0	MCP	MDP1	VDD3A	VTN1
F	MCLK	SDA	VSSD	MDN0	MCN	MDN1	VSSD	VSSA/VSSC

PIN NO.	PIN Name	PIN Type	Function/Description
A1	VDD3A	Power	Analog power supply(3.3v)
A2	VSSA/VSSC	Ground	Analog ground
A3	D5	Output	RGB/YUV image data output port [5]
A4	D6	Output	RGB/YUV image data output port [6]
A5	D9	Output	RGB/YUV image data output port [9]
A6	TRIG	InOut	Input:1:Trigger enable,int_time=pulse width 0:Trigger disable Output:Internal int_time pulse for LED
A7	VSYNC	InOut	Vertical synchronization output/Input Vsync for Synchronization
A8	VREF	Output	Reference power
B1	VDDD	Power	Digital power supply(1.5v)

PIN NO.	PIN Name	PIN Type	Function/Description
B2	PDN	Input	Power Down or Reset,0: Power down and Reset mode;1: Normal mode
B3	HSYNC	Output	Horizontal reference output
B4	D7	Output	RGB/YUV image data output port [7]
B5	D8	Output	RGB/YUV image data output port [8]
B6	VSSD	Ground	Digital ground
B7	VDDIO	Power	I/O power supply(3.3v)
B8	VSSA/VSSC	Ground	Analog ground
C1	D4	Output	RGB/YUV image data output port [4]
C2	D3	Output	RGB/YUV image data output port [3]
C3	D0	Output	RGB/YUV image data output port [0]
C4	VDDIO	Power	I/O power supply(3.3v)
C5	ID_SEL	Input	ID select(default 0) 1: 6eh ;0: 6fh.
C6	LED	Output	LED pulse
C7	VDDD	Power	Digital power supply(1.5v)
C8	VDD3A	Power	Analog power supply(3.3v)
D1	D1	Output	RGB/YUV image data output port [1]
D2	D2	Output	RGB/YUV image data output port [2]
D3	SCL	InOut	SCCB serial interface clock I/O
D4	VDDD	Power	Digital power supply(1.5v)
D5	/	/	/
D6	/	/	/
D7	MEN	Input	Master_en,0: slave_mode;1: E2prom mode
D8	VTN0	Output	negative power for TX0
E1	VDDD	Power	Digital power supply(1.5v)
E2	VDDIO	Power	I/O power supply(3.3v)
E3	PCLK	Output	image clock output
E4	MDP0	Output	MIPI data lane0 positive output
E5	MCP	Output	MIPI clock lane positive output
E6	MDP1	Output	MIPI data lane1 positive output
E7	VDD3A	Power	Analog power supply（3.3v)

PIN NO.	PIN Name	PIN Type	Function/Description
E8	VTN1	Output	negative power for TX1
F1	MCLK	Input	System clock input (27Mhz)
F2	SDA	InOut	SCCB serial interface data I/O
F3	VSSD	Ground	Digital ground
F4	MDN0	Output	MIPI data lane0 negative output
F5	MCN	Output	MIPI clock lane negative output
F6	MDN1	Output	MIPI data lane1 negative output
F7	VSSD	Ground	Digital ground
F8	VSSA/VSSC	Ground	Analog ground

9. Application Timing Diagram

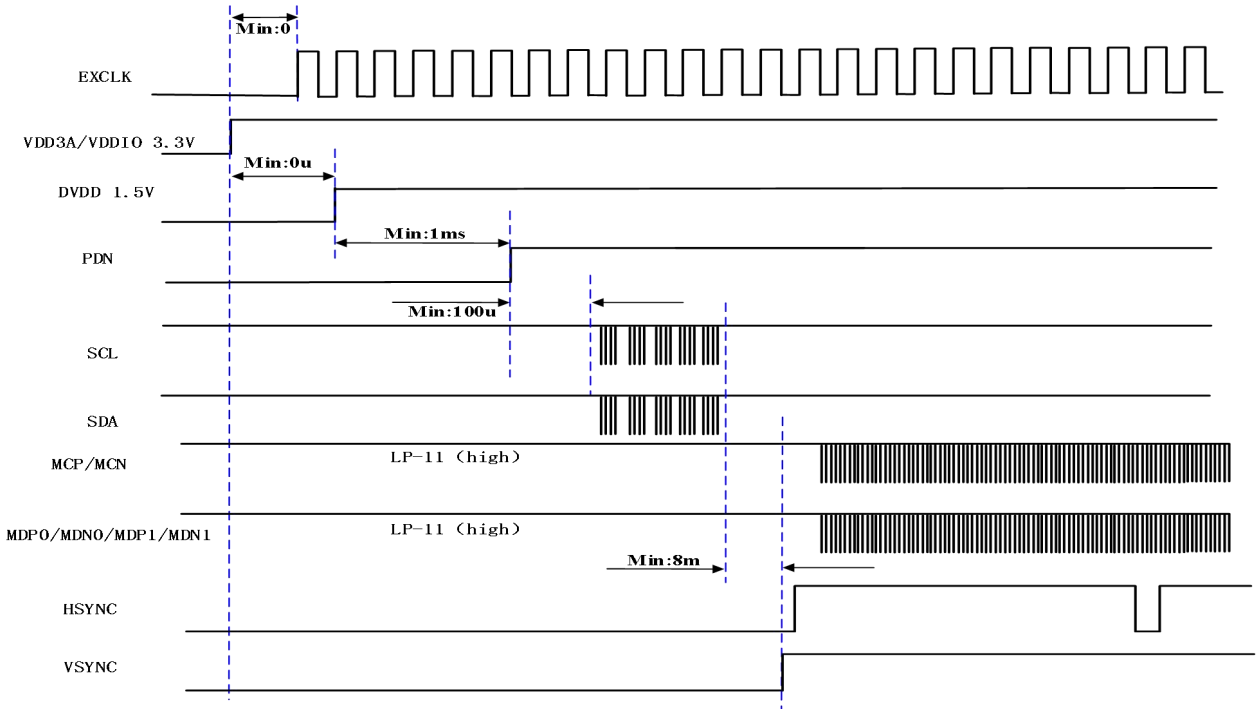


Figure 13.Power-on Sequence

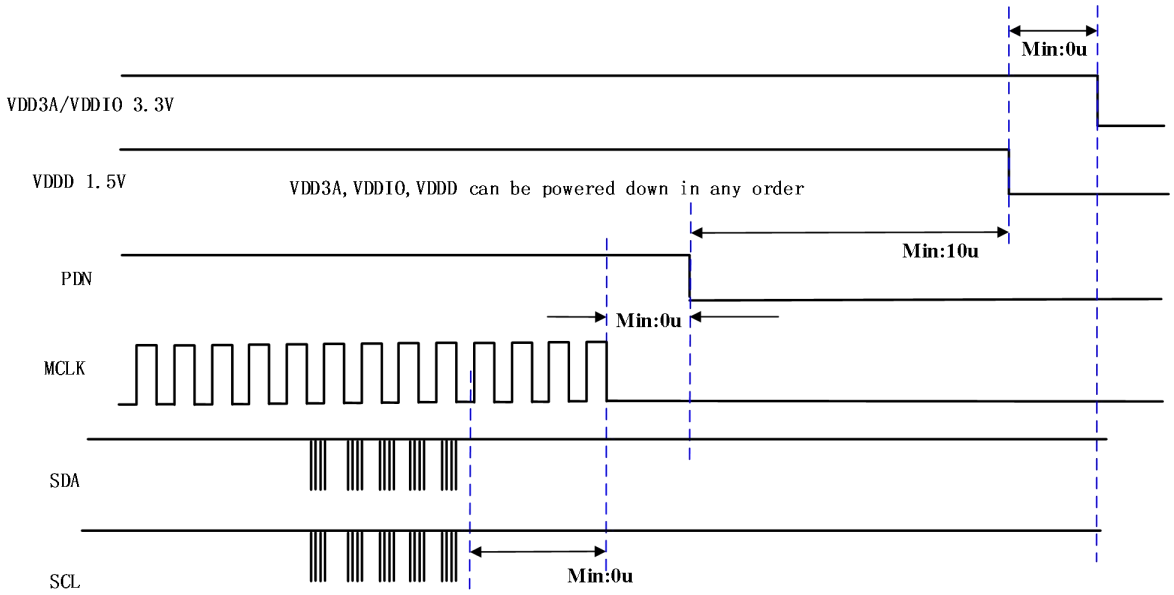


Figure 14.Power-off Sequence

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