1/3.55' inch 1.3M Rolling Shutter CIS

BF314C

Datasheet

content

1. General Description

BF314C is a Rolling shutter CMOS image sensor. It supports up to 30fps @ 1280H×960V full resolution mode using MIPI interface and 30 fps @ 1280H×960V Parallel mode. BF314C outputs color raw image, and the max array size is 1340H × 1020V. Complex on-chip operations are supported, like Trigger (Rolling shutter), vertical/horizontal mirror or flip.

BF314C is supported to be configured by standard IIC interface.

BF314C is supported to be triggered by Pin VSYNC and internal register.

2. Features

- Standard optical format of 1/3.55 inch for 1.3 million pixel
- 3.0μm Square Pixels with Micro-lens
- 30 frames/sec 1280H×960V HDR mode @ 70.875MHz inner clock with MIPI output
- 30 frames/sec 1280H×960V HDR mode @ 70.875MHz inner clock with Parallel output
- Input Frequency: 6 /24 /27 MHz
- Output formats: Raw / YUV422
- Horizontal /Vertical mirror
- Auto black level control
- Sensor Control function: Auto-Exposure control, Auto-Gain control, Test pattern, Image size control
- Package: COB/CSP/ imBGA

The BF314C is designed to provide a complete system solution using a fully processed YUV output with overlay features. The BF314C integrates a high performance ISP with improved HDR function to deliver high quality images. The processed video is output from a DVP/MIPI interface.

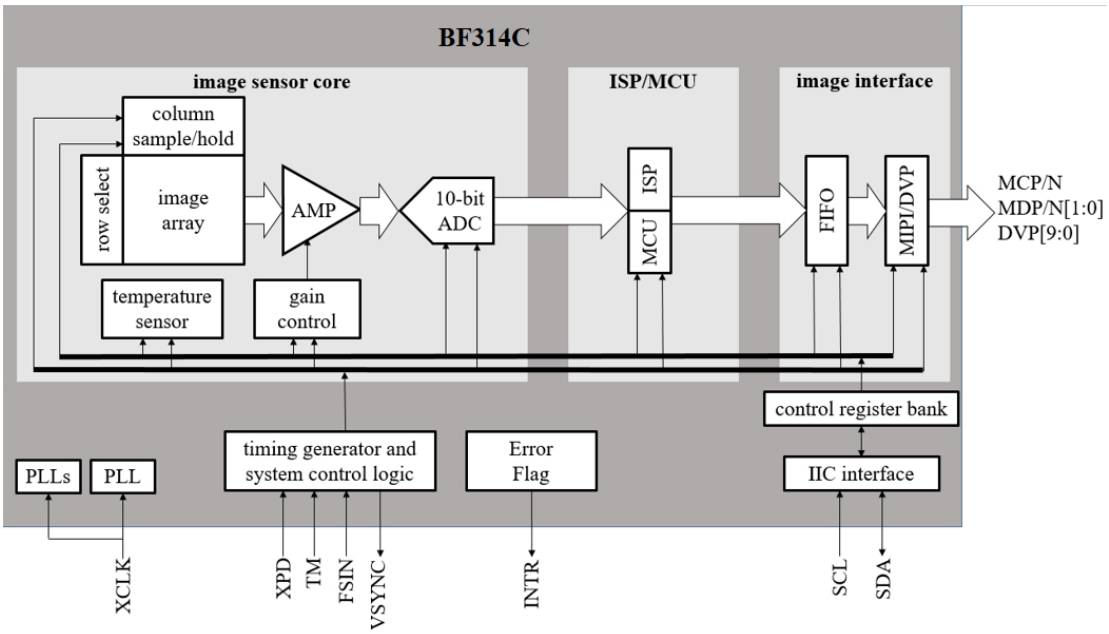


Figure 2-1 BF314C block diagram

The sensor consists of three major functional blocks: Sensor core, Image processor, and Output interface.

The sensor core receives the photo signal and coverts it to an electric signal. The signal is then amplified and digitized. Dark current and circuit offset are canceled by the black level calibration (BLC) function. The correction is purely implemented in the digital domain. Dark current increases exponentially with temperature and the BLC can be configured to automatically re-trigger with changes in exposure, output format, applied gain, and out of range offsets, in addition to manually triggering it.

The video stream is then fed into the image processor where it is fully processed to the format ready for display. AEC/AGC statistics are collected in the image processor and sent back to the automatic exposure control (AEC), automatic

gain control (AGC), and automatic dynamic range control (ADRC) to control the exposure time and gain of the long, middle channel, and short channel.

The processed image is formatted and output through the digital video port (DVP) or MIPI interface. The supported image formats include 10-bit RAW data of the long, short and very short channel, up to 18-bit linear HDR RAW data, and the fully processed 8-bit YUV422 format.

The BF314C supports dual conversion gain, which means a switchable two conversion gain in one exposure (integration time): low conversion gain (LCG) for large charge handling capacity in bright scenes and a high conversion gain (HCG) mode with increased sensitivity with low read noise for low-light scenes. Higher CG means higher sensitivity, as one single electron can be more easily detected. Higher CG also means that the sensor will realize a reduction in read noise. The sensor core supports two different readout schemes of three capture that can be used to process a high dynamic range image. The first mode consists of dual exposure staggered (HCG, LCG, and VS), the alternative readout mode consists of three exposure staggered (long, short and very short).

The reference voltage and current required in the pixel read out, amplifier, and ADC are generated by the reference generator. All functional blocks are controlled by registers. The host controller can program and read back through the IIC interface.

3. Applications

- Security systems
- Automotive：360° surround view system and rear view camera
- Scanning system
- Digital still cameras and camcorders
- Video telephony and conferencing equipment
- Industrial and environmental systems

4. Technical Specifications

Table 4- 1 Sensor Key Features

● Active pixel array:	1340×1020
● Pixel size:	3.0um×3.0um
● Sensitivity:	TBD
● Dark current:	TBD
● Power supply:	1.8/2.8V for I/O 1.2V~1.4V for VDDD 2.75V~3.2V for VDD3A
● Power consumption:	<350mW@30fps HDR Mode (full resolution
● Standby current:	TBD
● S/N Ratio:	TBD
● Dynamic range:	TBD
● Operating temperature:	-40~105°C
● Stable Image temperature:	-40~105°C
● Optimal lens chief ray angle:	20º linear
● Package:	COB/CSP/ imBGA

NOTE:

The above specifications are typical value unless otherwise specified.

5. Functional Overview

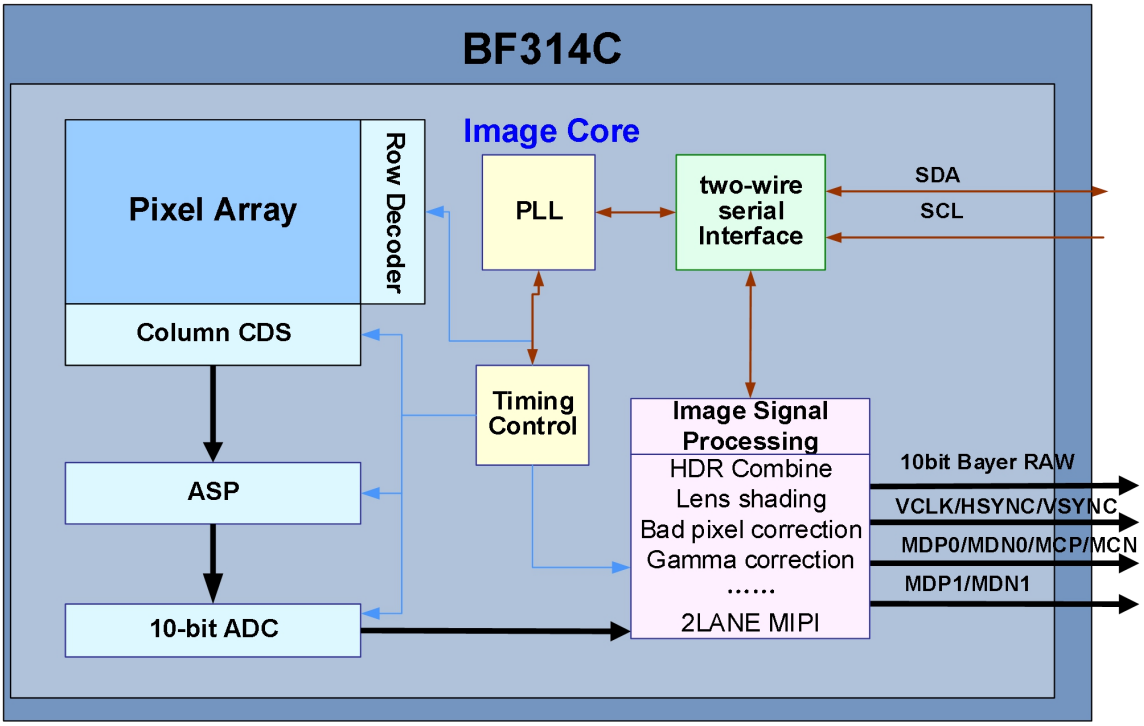


Figure 5-1 Block Diagram

BF314C has an active image array of 1340 × 1020 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The ASP block is mainly used to control global gain to get accurate exposure under different light condition. The analog signal is transferred to digital signal by A/D converter. The digital signals are controlled by Sensor control Block, including Auto-Exposure control, Auto-Gain control, Test pattern, Image size control and so on.

BF314C has on-chip PLL, it can be used by via two-wire serial interface bus setting.

5.1 Pixel Array

The pixel array includes 1340×1020 effective pixels for imaging, in order to improve the image uniformity, there are extra dummy rows and dummy columns around active array. And dark rows at the top side are for black level control.

Pixel array is covered by Bayer color filters as can be seen in the Figure 5-2. The primary color BG/GR array is arranged in line-alternating fashion. Since each pixel can have only one type of color filter on it, only one color component can be obtained by a pixel. BF314C can provide the Raw Bayer data through an 10-bit output data bus.

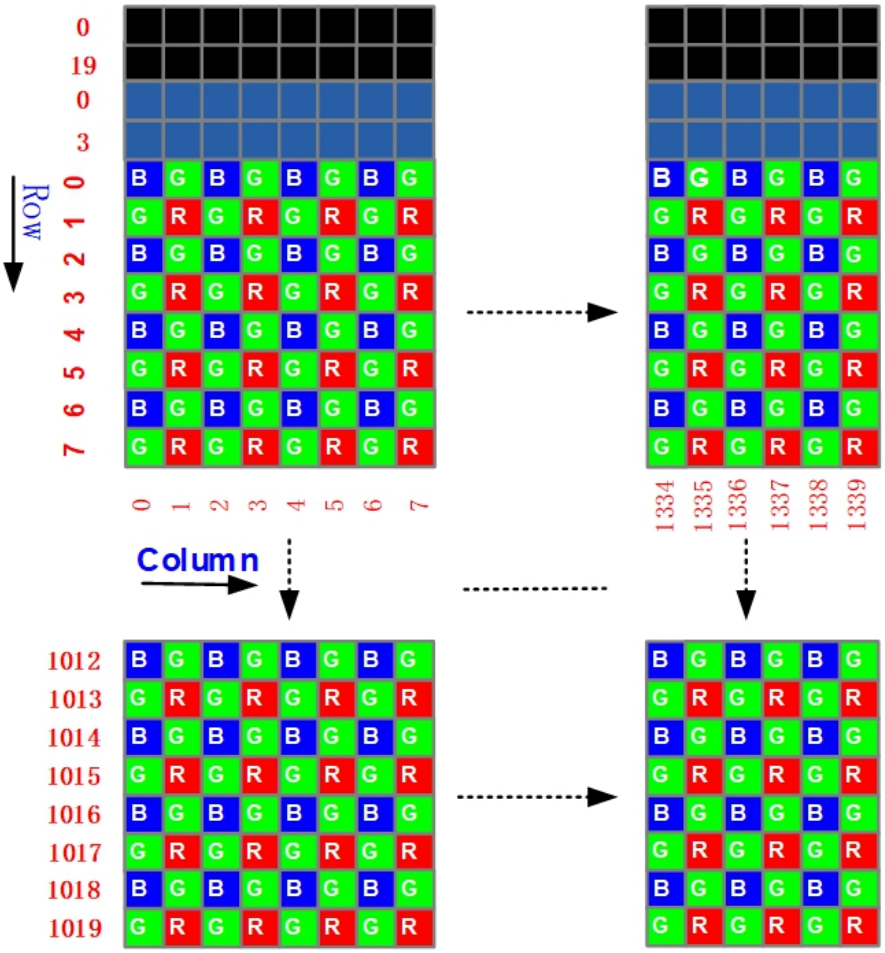


Figure 5-2 Sensor Array Region

Pixel array output signal order is changed by Vertical Flip or Horizontal Mirror.

Table 5- 1 Flip function

Function	**First Pixel**	Register setting
Normal	B	0xf4=0x00
Horizontal Mirror	Gb	0xf4=0x02
Vertical Flip	Gr	0xf4=0x01
Horizontal Mirror and Vertical Flip	R	0xf4=0x03

The readout image array size is supported the resolution of 720p and 960p by the registers setting.

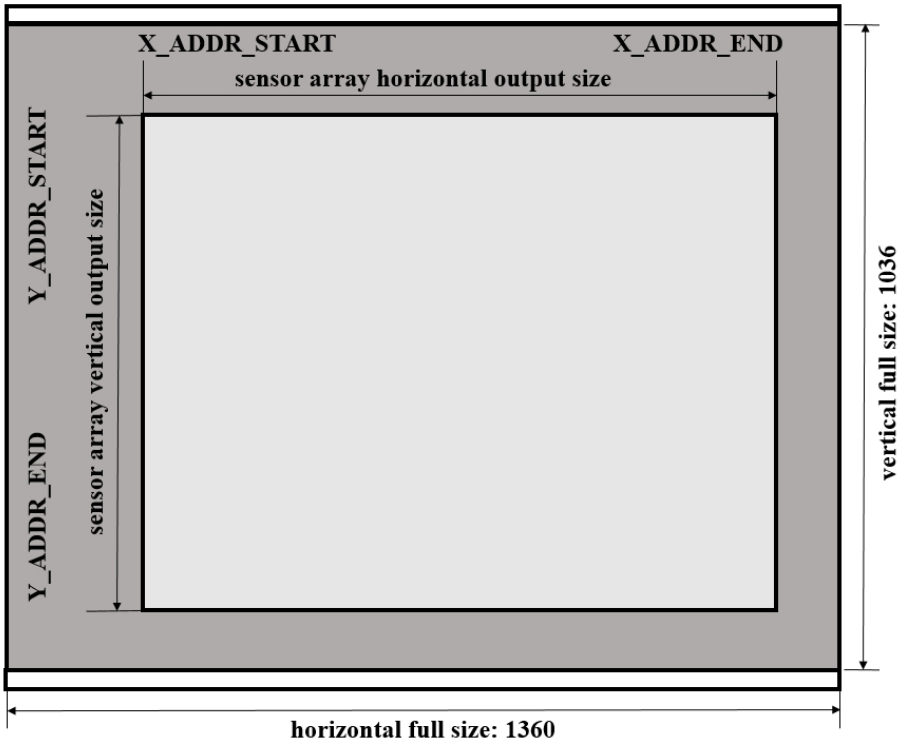


Figure 5-3 pixel array access diagram

5.2 Column CDS

BF314C has column/row driver circuits to read out the pixel data progressively. The CDS (Correlated Double Sampling) circuit reduces temporal noise and pixel level FPN (Fixed Pattern Noise). The unique patented column buffer and ASP (Analog Signal Processing) circuit remove column level FPN caused by various sources of manufacturing process variations.

5.3 Sensor control

- Array control and frame generation
- Internal timing signal generation and distribution
- Exposure control, Gain control, Test pattern,
- Image size control
- Frame rate timing
- External timing outputs (VSYNC, HSYNC and PCLK)

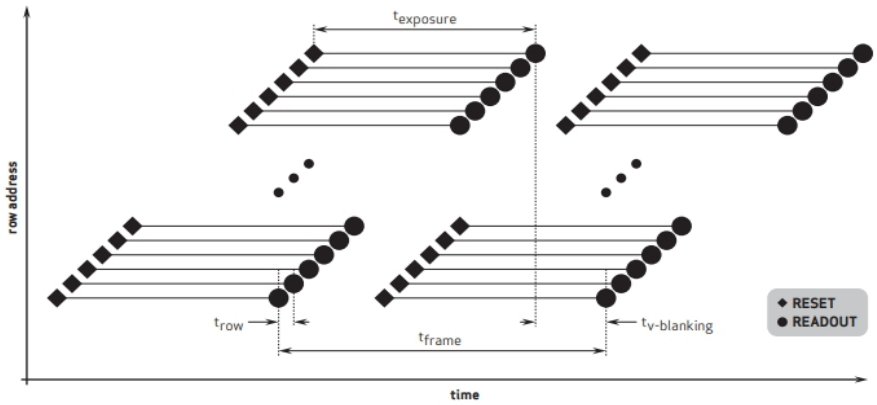


Figure 5-4 row address versus time graph

The BF314C employs an electronic rolling shutter (ERS) for exposure control (see Figure 5-4). The pixel array is first reset row by row and when the exposure time has elapsed, the readout of the pixel array is done row by row.

The timing generator generates all the control signals based on a row counter and column counter. Refer to Figure 5-5 for frame timing. The row period consists of an active output period and a horizontal blanking period. A vertical blanking period is also required to perform frame-based operation. The vertical blanking period seen by the back-end processor is usually longer than the internal vertical blanking because the BLC is reading the optical black rows required to perform the correction.

A minimum number of clock periods are required to complete all the required operations per row (blanking time).

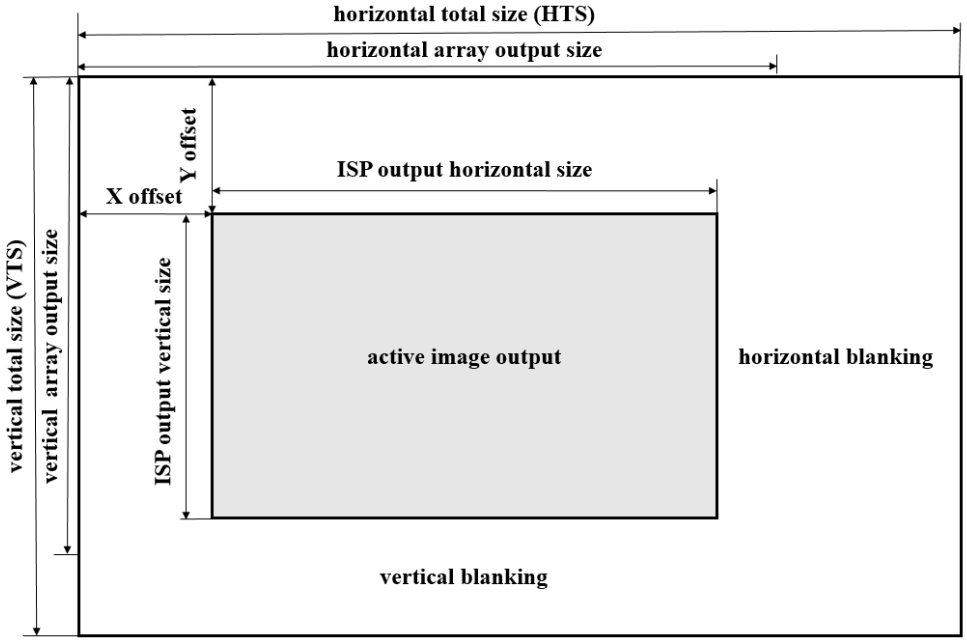


Figure 5-5 frame output timing diagram

5.4 A/D converter

The analog signals are converted to digital forms one line at a time and data are streamed out column by column.

BF314C provides the 10-bit Raw Bayer data through an internal 10-bit data bus.

5.5 Automatic Black Level Control

The automatic black level control calculates the data of the dark row and controls the lowest black level for output image data.The pixel array contains several optically shielded (black) rows. That section of the pixel array is used as reference for black level correction. The main function of the BLC is to adjust all normal pixel values based on the values of the black levels.

5.6 Image Signal Processor

This block performs all image processing functions including Lens Shading Correction, Gamma Correction, Bad pixel correction, Color Interpolation, Low Pass Filter, Color Space Conversion, Color Correction, Edge Enhancement, Auto exposure, Auto White Balance, Color Saturation, Contrast, Data Format Conversion.

5.7 Test pattern mode

The BF314C provides many types of test pattern mode.

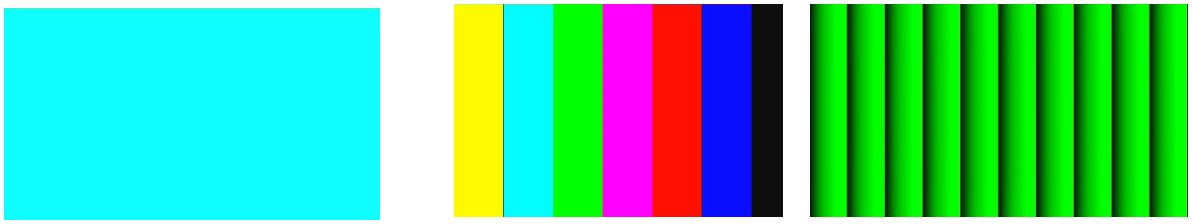


Figure 5-6 test pattern types

The BF314C also offers test patterns with transparent effect , bar effect or Manual definition effect.

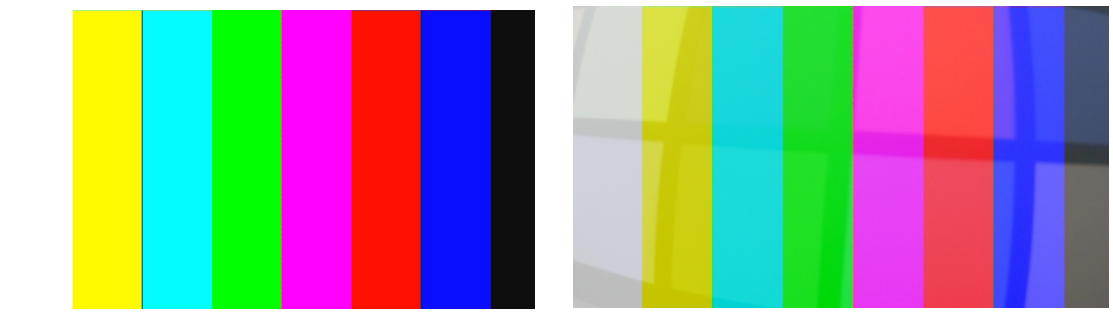


Figure 5-7 test pattern effects

Test pattern control registers are separated for long channel, short channel, and very short channel.

5.8 AEC/AGC

AEC/AGC is adjusted to change the image brightness. BF314C adjusts exposure time by AEC, and it adjusts gain value by AGC. They work together to adjust the image brightness into the range of setting threshold.

In the BF314C, the exposure/gain control is designed to adjust the weighted frame average to a user defined range. The weight of each pixel includes three parts: position weight, combination weight, and luminance weight. In HDR mode, the AEC/AGC adjusts the exposure and gain for both long, short, and very short channels. The dynamic range extension is dependent on the long to very short channel exposure ratio. By default, the exposure ratio is automatically adjusted according to the dynamic range of the scene and the target stable range.

5.9 MIPI

BF314C provides mobile industry processor interface (MIPI). Sensor supports 1-2 lanes to transfer 8/10 bit image data.

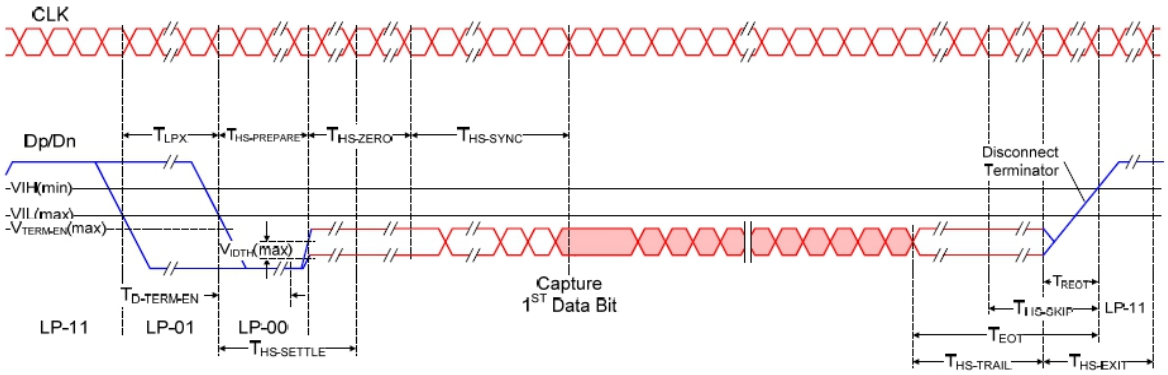


Figure 5-8 High-Speed Data Transmission in Bursts

The BF314C has a configurable MIPI output port with programmable number of lanes (1 or 2) and a maximum bit rate of 960 Mbps per lane. Both virtual channel and no-virtual channel is supported.

The BF314C has a 2-lane data MIPI transmitter which can run at various MIPI clock frequencies to match with the MIPI receiver at host. The MIPI CSI output supports up to 4 virtual channels of video output. It can be programmed to transfer a single video stream, side-by-side video images, and stereo video output. The maximum data rate can be up to 960 Mbps/lane by the constraint of I/O pad sharing with DVP signals. Figure 5-10 shows the sequence of events during the transmission of a data burst. Transmission can be started and ended independently for any lane by the protocol. However, for most applications the lanes will start synchronously, but may end at different times due to an unequal amount of transmitted bytes per lane.

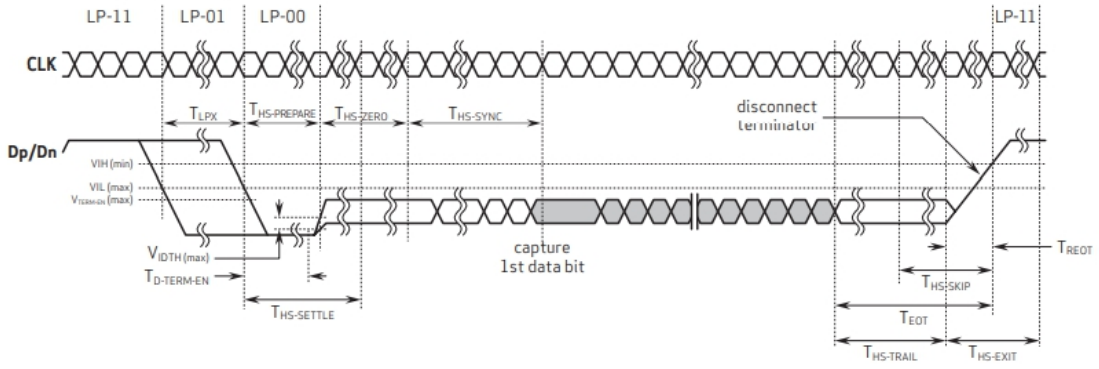


Figure 5-9 High speed data transmission in bursts

A clock lane is similar to a unidirectional data lane. However, there are some timing differences and a clock lane transmits a high speed DDR clock signal instead of data bits. The clock lane module is controlled by the protocol via the clock lane PPI. The protocol shall only stop the clock lane when there are no high speed transmissions active in any data lane.

The high speed data transmission start-up time of a data lane is extended if the clock lane is in low power mode. In this case, the clock lane must first return to high speed operation before the transmit request can be handled.

The high speed clock signal will continue running for a period TCLK-POST after the last data lane switches to low power mode and ends with a HS-0 state.

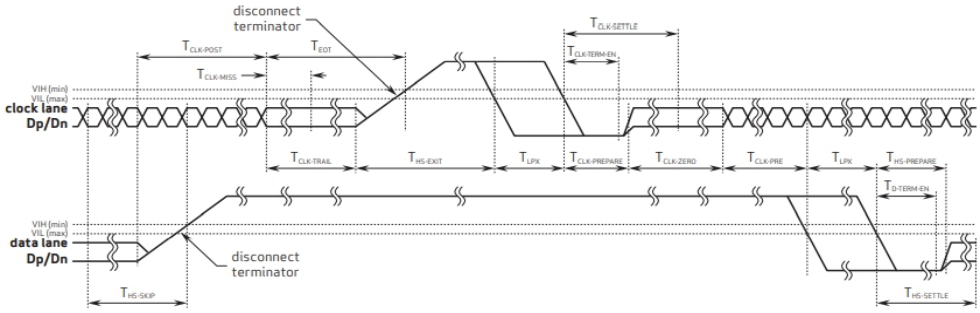


Figure 5-10 Switching clock lane between clock transmission and low power mode

5.10 Multi-sensor synchronization mode

Trigger signal can be controlled by input VSYNC PAD. When the signal occurs from 0 to 1, the slave BF314C sensors restart to exposure. Image data output starts follow the edge of trigger signal from master sensor or generator. The frequency of trigger signal must be the same with output frame rate of the slave sensor.

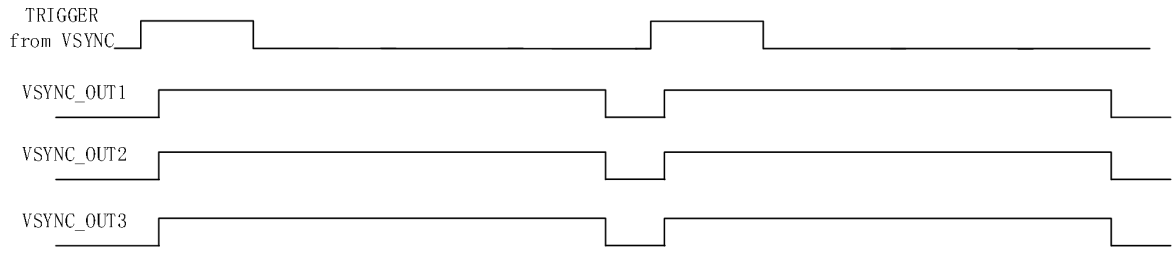


Figure 5-11 Output with synchronization mode

5.11 Serial/Overlap

BF314C includes serial output mode and overlap mode controlled by Bit[7] of Page0:02h, it has different integration time control and output position.

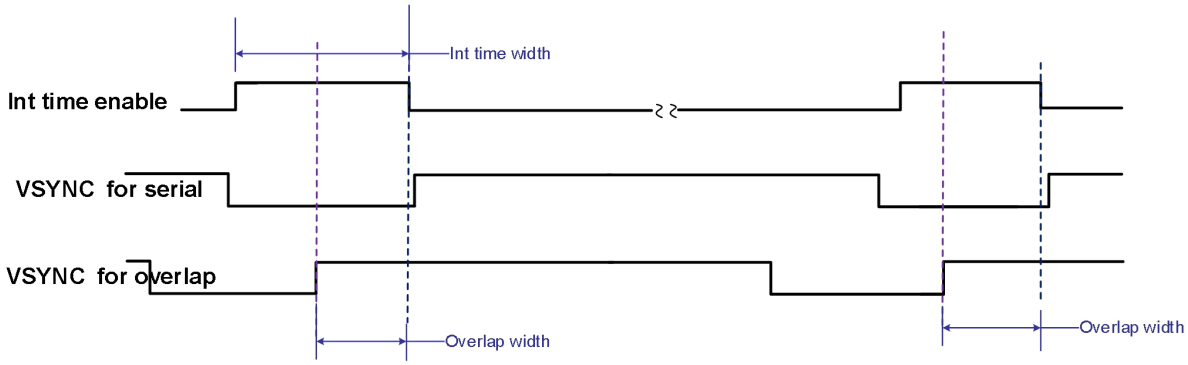


Figure 5-12 Different VSYNC output mode

5.12 Windowing

BF314C supports analog windowing and digital windowing. Analog windowing will change the line length and frame length. And digital windowing will not change the line length and frame length.

5.13 HDR

BF314C Supports two types of HDR mode：line overlap HDR and In-pixel double convert gain HDR. HDR refers to the improvement of the dynamic range of the image by combing multiple frames of the same scene, different exposure times, and different gains in one frame.

6. Specifications

6.1 Electrical Characteristics

6.1.1 Absolute Maximum Ratings

- Supply voltage (VDDIO): 1.7 ~ 3.2 V
- Supply voltage (VDDD): 1.2~ 1.4 V
- Supply voltage (VDD3A): 2.75~ 3.2 V
- Operating temperature: -40~105°C
- Storage temperature: -40~105°C
- ESD Rating, Human Body Mode: TBD

Caution: Stresses exceeding the absolute maximum ratings may induce failure.

Table 6- 1 Absolute maximum ratings[a]

Parameter	Name	Absolute maximum rating
ambient storage temperature	Storage	-50°C to +125°C
supply voltage	VDD3A	3.2V
	VDDIO	3.2V
	VDDD	1.4V
all input/output voltages (with respect to ground)		0.3V - VDDIO + 1V
I/O current on any input or output pin		±200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

6.1.2 DC Parameters

Table 6- 2 DC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
VDDIO	I/O power supply	V	1.7	1.8/2.8	2.0/3.2	1
VDDD	Digital power supply	V	1.2	1.25	1.4	2
VDD3A	Analog power supply	V	2.75	2.8	3.2	--
Vih	Input voltage logic "1"	V	0.7*VDDIO	--	--	--
Vil	Input voltage logic "0"	V	--	--	0.2*VDDIO	--
Voh	Output voltage logic "1"	V	0.9*VDDIO	--	--	--

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
Vol	Output voltage logic "0"	V	--	--	0.1*VDDIO	--
I_vddio	VDDIO supply current, normal operation mode	mA	0.1	22	--	2
I_vddd	VDDD supply current,	mA	-- --	30	70	2
I_vdd3a	VDD3A supply current,	mA	--	30	--	2

Note:

1. VDDIO=3.3V default or VDDIO=1.8V
2. The current of VDDD and VDDIO will have different value in MIPI mode and parallel mode, the Current of power is decided by the work mode, ex. Frequency of clock and output format. the Max. Current will not appear at the same time.

6.1.3 Clock Requirement

Table 6- 3 AC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
XCLK	External clock frequency	MHz	--	6~27	--	1
PCLK	Master clock	MHz	--	70.875	81	2
SCL	two-wire serial interface clock frequency	KHz	--	400	--	3

Note:

1. XCLK is the input clock and it is the input of PLL.
2. PCLK is the pixel clock of the system, and it can be generated by PLL. For MIPI output mode, the frequency will be higher.
3. SCL is driven by host processor. For the detail serial bus timing, refer to two-wire serial Interface section

6.2 Electro-Optical Characteristics

Clock frequency: 27MHz.

Operating voltage: VDDIO=1.8V, VDD3A=2.8V, VDDD=1.25V

Operating temperature: 25°C

Table 6- 4 Electro-Optical Characteristics

Parameter	Unit	Min.	Typ.	Max.	Notes
Sensitivity	V/Lux·sec	--	TBD		1
Dark current	mV/sec	--	TBD	--	2
S/N ratio	dB	--	TBD	--	--
Dynamic Range	dB	--	TBD	--	--
Frame Rate	fps	--	30	90@single frame	3

Notes:
1. With color filter, measured at 50 lux green light condition at room temperature.
2. Measured at dark condition for exposure time of 1s (25 Celsius).
3. With 1340×1020 window size at PCLK 70.875MHz for MIPI mode.

6.3 Timing

6.3.1 The Sensor-core Readout Mode

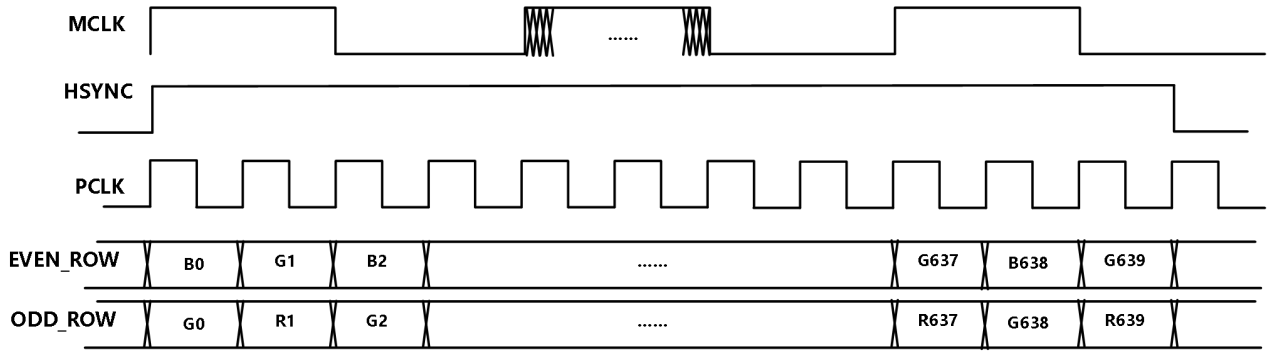


Figure 6- 1 Horizontal Timing Raw Bayer Data

6.3.2 The output Fame Timing

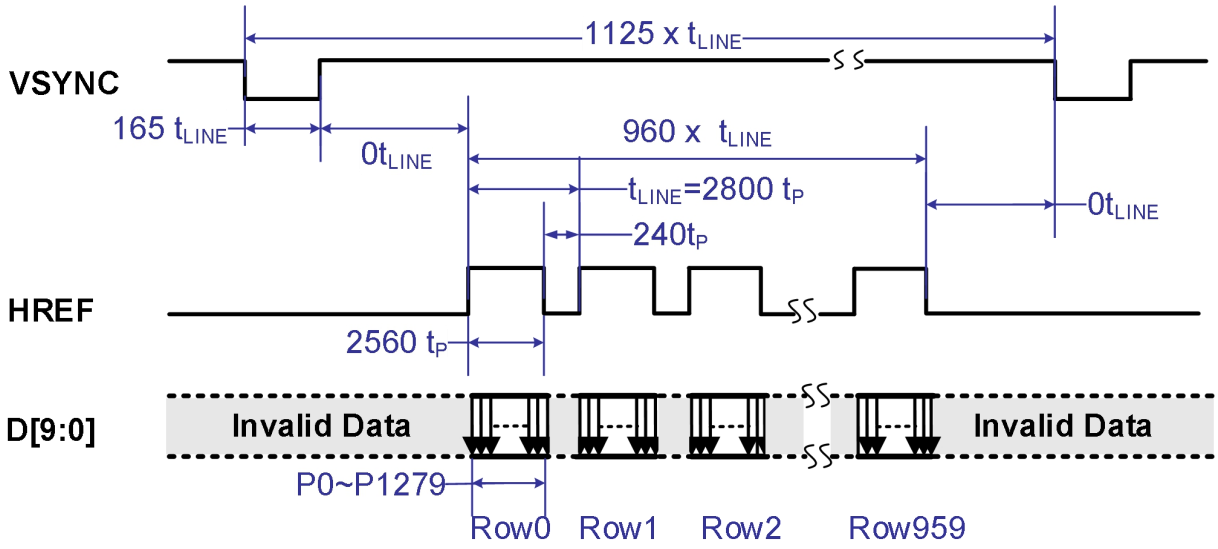


Figure 6- 2 Output Frame Timing for YUV mode

Table 6- 5 AC Characteristics

Symbol	Descriptions	Min.	Typ.	Max.	Unit
t_P	Pixel output clock period	10.4	10.58	--	ns
f_{VCLK}	Video Clock Frequency f_{VCLK} can be adjusted by PLL	--	94.5	108	MHz
t_{LINE}	Line length	--	2800 x t_P	--	ns

6.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below.

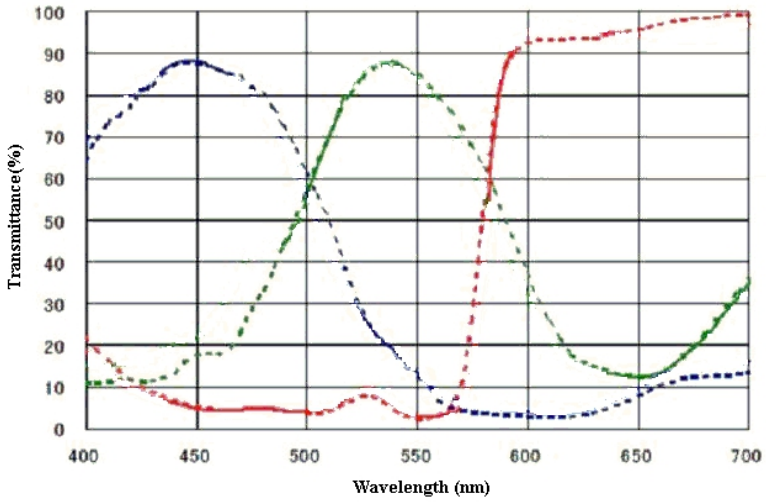


Figure 6- 3 Spectral Characteristics

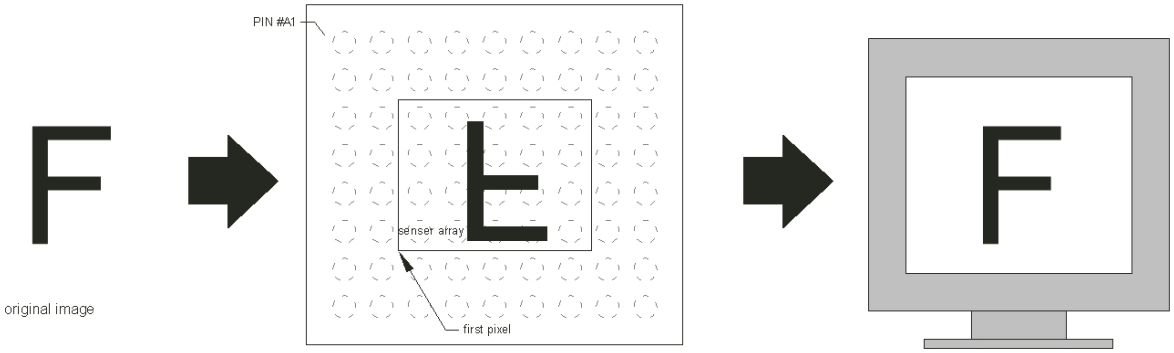


Figure 6- 5 final image output

6.5 CRA(Chief Ray Angle linear 20◦)

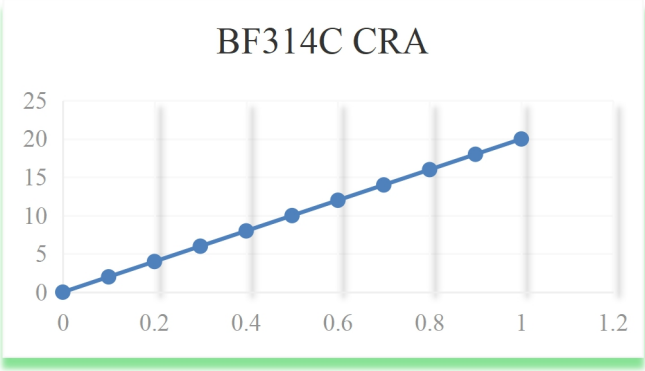


Figure 6- 6 CRA

Table 6- 6 CRA versus image height plot

Field(%)	Image Height(mm)	CRA(degree)
0	0.000	0
0.1	0.253	2
0.2	0.506	4
0.3	0.759	6
0.4	1.012	8
0.5	1.265	10
0.6	1.518	12
0.7	1.771	14
0.8	2.024	16
0.9	2.277	18
1	2.530	20

7. Two-wire serial interface& Register

7.1 Theory of Operation

The registers of BF314C are written and read through the two-wire serial interface. BF314C has two-wire serial interface slave. BF314C is controlled by the two-wire serial interface clock (SCL), which is driven by the two-wire serial interface master. Data is transferred into and out of BF314C through the two-wire serial interface data (SDA) line. The SCL and SDA lines are pulled up to VDDIO by a 2kΩ off-chip resistor. Either the slave or the master device can pull the lines down. The two-wire serial interface protocol determines which device is allowed to pull the two lines down at any given time.

Note: Two-wire serial interface device address of BF314C is 7'b1101110 (0X6e) or 7'b1101101 (0X6d),it can control by input ID_SEL PAD,it doesn't include W/R bit.

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A0 in the LSB of the address indicates write mode, and A1 indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The two-wire serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock: it can only change when the two-wire serial interface clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a write and a 1 indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The BF314C uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit

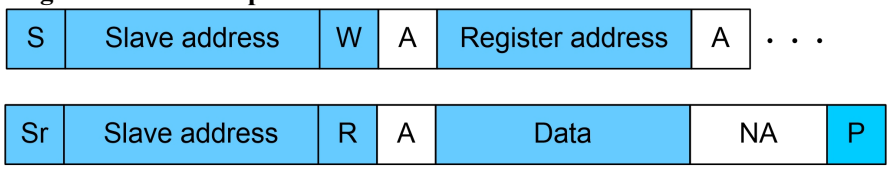
transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

7.2 Two-wire Serial Interface Functional Description

Single Write Mode Operation

Multiple Write Mode (Register address is increased automatically) [1] operation

Single Read Mode Operation



Multiple Read Mode (Register address is increased automatically) [1] Operation

From master to slave From slave to master
S: Start condition. Sr: Repeated Start (Start without preceding stop.)
Slave Address: for device address 7'b1101110 (0x6e)
write address = DCh = 11011100b
read address = DDh = 11011101b
Slave Address: for device address 7'b1101101 (0x6d)
write address = DAh = 11011010b
read address = DBh = 11011011b
R/W: Read/Write selection. High = read, LOW = write.
A: Acknowledge bit. NA: No Acknowledge.
Data: 8-bit data P: Stop condition
Note1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

7.3 The Two-wire Serial Interface Timing

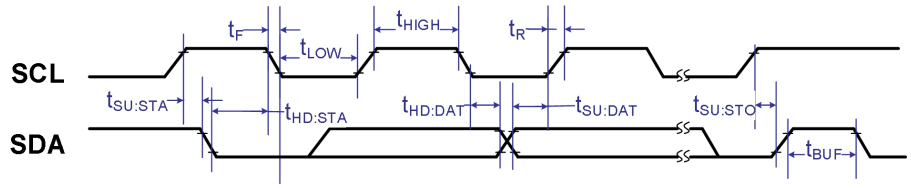


Figure 7- 1 Two-Wire Serial Interface Timing

Table 7- 1 AC Characteristics

Symbol	Descriptions	Min.	Typ.	Max.	Unit
t_R, t_F	two-wire serial interface rise/fall times	--	--	300	ns
t_{LOW}	Clock Low Period	1.3	--	--	us
t_{HIGH}	Clock High Period	600	--	--	ns
$t_{HD:STA}$	Start condition Hold Time	600	--	--	ns
$t_{SU:STA}$	Start condition Setup Time	600	--	--	ns
$t_{HD:DAT}$	Data-in Hold Time	0	--	--	ns
$t_{SU:DAT}$	Data-in Setup Time	100	--	--	ns
$t_{SU:STO}$	Stop condition Setup Time	600	--	--	ns

Table 7- 2 BF314C system control registers

8. Register Summary (full list)

8.1 Top Registers

Address	Name	Width	Default value	Description
f0h	***MODE_SEL***	8	01h	Bit[7]: Data format enable 1'b0: Enable; 1'b1: Disable; Bit[6]: HDR enable 1'b0: Enable; 1'b1: Disable; Bit[5]: AWB enable 1'b0: Enable; 1'b1: Disable; Bit[4]: SRAM2 enable 1'b0: Enable; 1'b1: Disable; Bit[3:1]: Reversed; Bit[0]: Mode select 1'b1: Output enable for tri I/O PAD; 1'b0: Input enable for tri I/O PAD;
f1h	***ISPBYPS***	8	00h	Bit[7]: Reversed; Bit[6]: Contrast enable 1'b0: Enable; 1'b1: Disable; Bit[5]: Saturation enable 1'b0: Enable; 1'b1: Disable; Bit[4]: Color space enable 1'b0: Enable; 1'b1: Disable; Bit[3]: Color Correction enable 1'b0: Enable; 1'b1: Disable; Bit[2]: Color Interpolation enable 1'b0: Enable; 1'b1: Disable; Bit[1]: Gamma Correction enable 1'b0: Enable; 1'b1: Disable; Bit[0]: Lens Correction enable 1'b0: Enable; 1'b1: Disable;
f2h	***SCCB_RRST_REG***	1	0h	Bit[0]: SCCB reset,register reset 1'b1: On; 1'b0: Off;
f3h	***PDA***	1	0h	Bit[0]: PDA 1'b0: Work normal; 1'b1: Standby mode;
f4h	***HVFLIP***	2	00h	Bit[1]: Hflip_en 1'b0: Normal; 1'b1: Flip mode; Bit[0]: Vflip_en 1'b0: Normal; 1'b1: Flip mode;
fah	***SRAM_STATE***	8	RO	Bit[7]: Fixed to 0; Bit[6]: TEST_DONE for SRAM1; Bit[5]: TEST_DONE for SRAM2; Bit[4]: TEST_DONE for SRAM3; Bit[3]: Fixed to 0; Bit[2]: TEST_FAIL for SRAM1; Bit[1]: TEST_FAIL for SRAM2; Bit[0]: TEST_FAIL for SRAM3;
fch	***PIDH_BME***	8	31h(RO)	Product ID MSB;
fdh	***PIDL_BME***	8	4ch(RO)	Product ID LSB;
feh	***REGFE***	2	00h	Bit[1:0]: I2C Page selection 2'b00: Page 0; 2'b01: Page 1; 2'b10: Page 2;

8.2 CLK Control Registers

Page	Address	Name	Width	Default value	Description
2	e3h	***REG_COM3***	8	a9h	Bit[4]: Clk_AD1: 1'b1: Powerdown PLL; 1'b0: Work; Bit[3:0]: Sel for PLL2 Pre-DIV[3:0] x=Bit[3:0]=1~15, (4'1000,Default) (x=16@4'b0000); Fref=Fin/x;

Page	Address	Name	Width	Default value	Description
	e4h	***REG_COM4***	8	bdh	Main loop freq div: 8'b10111101 default;

8.3 Sensor Control Registers

Page	Address	Name	Width	Default value	Description
0	06h	***VBLANK_PIX_L***	8	7dh	LSB of min dummy line;
	07h	***VBLANK_PIX_H***	8	00h	HSB of min dummy line;
	0bh	***LINE_LREG_LOCK***	8	78h	Bit[7:0]: LINE_LENGTH[7:0];
	2ch	***FRAME_LENGTH_L***	8	97h	LSB of FRAME_LENGTH_DEFAULT;
	2dh	***FRAME_LENGTH_H***	8	00h	HSB of FRAME_LENGTH_DEFAULT;
	30h	***DCG_LINE_REG_L***	8	d4h	Bit[7:0]: LINE_LENGTH[7:0] for DCG;
	31h	***DCG_LINE_REG_H*** ***LINE_HREG_LOCK***	8	15h	Bit[7]: HDR0_MODE; Bit[6:4]: LINE_LENGTH[10:8] for DCG; Bit[3:0]: LINE_LENGTH[11:8];

8.4 Black Control Registers

Page	Address	Name	Width	Default value	Description
0	50h	***FRAME_AVER_TH***	8	10h	Used as black level update threshold when multi frame is enable;
	51h	***MODE_CNTL1***	8	1fh	Bit[7]: AHD_720P_EN: 1'b1: On; 1'b0: Off; Bit[6:5]: TEST_PATTERN: 2'b0x: Close test_pattern; 2'b10: Use fixed value for test mode; 2'b11: Use counter value for test mode; Bit[4]: LAST_EN: Remove single bad pixel; 1'b1: Enable; 1'b0: Disable; Bit[2]: DARK_OUT_MODE 1'b1: Mode1 output DatIn0Dly1[10:1]; 1'b0: Mode2 output {DatIn0Dly1[10],DatIn0Dly1[8:0]}; Bit[1]: MUL_FRAME_EN; 1'b1: Use multiframe black level average as AVER; 1'b0: Use current frame black level as AVER; Bit[0]: SINGLE_FILT_EN: Use single frame filt before multiframe; 1'b1: Enable; 1'b0: Disable;
	52h	***AVER_LOCK_SUB***	2	00	Bit[7]: AVER_LOCK1: {AVER_LOCK[7:4],AVER_LOCK_SUB[1],1'b0}; Bit[6]: AVER_LOCK2: {AVER_LOCK[3:0],AVER_LOCK_SUB[0]}.
	53h	***DARKE0_L_AVER[9:8]*** ***DARKO0_L_AVER[9:8]*** ***DARKE1_L_AVER[9:8]*** ***DARKO1_L_AVER[9:8]***	8	RO	Bit[7:6]: Current frame BLC value for E row E col; Bit[5:4]: Current frame BLC value for E row O col; Bit[3:2]: Current frame BLC value for O row E col; Bit[1:0]: Current frame BLC value for O row O col;
	54h	***DARKE0_L_AVER***	8	RO	Current frame BLC value for E row E col;
	55h	***DARKO0_L_AVER***	8	RO	Current frame BLC value for E row O col;
	56h	***DARKE1_L_AVER***	8	RO	Current frame BLC value for O row E col;
	57h	***DARKO1_L_AVER***	8	RO	Current frame BLC value for O row O col;

Page	Address	Name	Width	Default value	Description
	58h	***DARKE0_L_AVER[10]*** ***DARKO0_L_AVER[10]*** ***DARKE1_L_AVER[10]*** ***DARKO1_L_AVER[10]*** ***DARKE0_M_AVER[10]*** ***DARKO0_M_AVER[10]*** ***DARKE1_M_AVER[10]*** ***DARKO1_M_AVER[10]***	8	RO	Bit[7]: Current frame BLC value for E row E col; Bit[6]: Current frame BLC value for E row O col; Bit[5]: Current frame BLC value for O row E col; Bit[4]: Current frame BLC value for O row O col; Bit[3]: Current frame BLC value for E row E col; Bit[2]: Current frame BLC value for E row O col; Bit[1]: Current frame BLC value for O row E col; Bit[0]: Current frame BLC value for O row O col;
	59h	***DARKE0_M_AVER[9:8]*** ***DARKO0_M_AVER[9:8]*** ***DARKE1_M_AVER[9:8]*** ***DARKO1_M_AVER[9:8]***	8	RO	Bit[7:6]: Current frame BLC value for E row E col; Bit[5:4]: Current frame BLC value for E row O col; Bit[3:2]: Current frame BLC value for O row E col; Bit[1:0]: Current frame BLC value for O row O col;
	5ah	***DARKE0_M_AVER***	8	RO	Current frame BLC value for E row E col;
	5bh	***DARKO0_M_AVER***	8	RO	Current frame BLC value for E row O col;
	5ch	***DARKE1_M_AVER***	8	RO	Current frame BLC value for O row E col;
	5dh	***DARKO1_M_AVER***	8	RO	Current frame BLC value for O row O col;
	5eh	***DARKE0_S_AVER[10]*** ***DARKO0_S_AVER[10]*** ***DARKE1_S_AVER[10]*** ***DARKO1_S_AVER[10]***	4	RO	Bit[7]: Current frame BLC value for E row E col; Bit[6]: Current frame BLC value for E row O col; Bit[5]: Current frame BLC value for O row E col; Bit[4]: Current frame BLC value for O row O col; Bit[3]: Current frame BLC value for E row E col; Bit[2]: Current frame BLC value for E row O col; Bit[1]: Current frame BLC value for O row E col; Bit[0]: Current frame BLC value for O row O col;
	5fh	***DARKE0_S_AVER[9:8]*** ***DARKO0_S_AVER[9:8]*** ***DARKE1_S_AVER[9:8]*** ***DARKO1_S_AVER[9:8]***	8	RO	Bit[7:6]: Current frame BLC value for E row E col; Bit[5:4]: Current frame BLC value for E row O col; Bit[3:2]: Current frame BLC value for O row E col; Bit[1:0]: Current frame BLC value for O row O col;
	60h	***DARKE0_S_AVER***	8	RO	Current frame BLC value for E row E col;
	61h	***DARKO0_S_AVER***	8	RO	Current frame BLC value for E row O col;
	62h	***DARKE1_S_AVER***	8	RO	Current frame BLC value for O row E col;
	63h	***DARKO1_S_AVER***	8	RO	Current frame BLC value for O row O col;
	64h	***AVER_TAR_L_E0***	8	00h	Black level target for E row E col;
	65h	***AVER_TAR_L_O0***	8	00h	Black level target for E row O col;
	66h	***AVER_TAR_L_E1***	8	00h	Black level target for O row E col;
	67h	***AVER_TAR_L_O1***	8	00h	Black level target for O row O col;
	68h	***AVER_TAR_L_E0[9:8]*** ***AVER_TAR_L_O0[9:8]*** ***AVER_TAR_L_E1[9:8]*** ***AVER_TAR_L_O1[9:8]***	8	00h	Bit[7:6]: Black level target for even col and even row; Bit[5:4]: Black level target for odd col and even row; Bit[3:2]: Black level target for even col and odd row; Bit[1:0]: Black level target for odd col and odd row;
	69h	***AVER_TAR_M_E0***	8	00h	Black level target for E row E col;
	6ah	***AVER_TAR_M_O0***	8	00h	Black level target for E row O col;
	6bh	***AVER_TAR_M_E1***	8	00h	Black level target for O row E col;
	6ch	***AVER_TAR_M_O1***	8	00h	Black level target for O row O col;
	6dh	***AVER_TAR_M_E0[9:8]*** ***AVER_TAR_M_O0[9:8]*** ***AVER_TAR_M_E1[9:8]*** ***AVER_TAR_M_O1[9:8]***	8	00h	Bit[7:6]: Black level target for even col and even row; Bit[5:4]: Black level target for odd col and even row; Bit[3:2]: Black level target for even col and odd row; Bit[1:0]: Black level target for odd col and odd row;
	6eh	***AVER_TAR_S_E0***	8	00h	Black level target for E row E col;
	6fh	***AVER_TAR_S_O0***	8	00h	Black level target for E row O col;
	70h	***AVER_TAR_S_E1***	8	00h	Black level target for O row E col;
	71h	***AVER_TAR_S_O1***	8	00h	Black level target for O row O col;
	72h	***AVER_TAR_S_E0[9:8]*** ***AVER_TAR_S_O0[9:8]*** ***AVER_TAR_S_E1[9:8]*** ***AVER_TAR_S_O1[9:8]***	8	00h	Bit[7:6]: Black level target for even col and even row; Bit[5:4]: Black level target for odd col and even row; Bit[3:2]: Black level target for even col and odd row; Bit[1:0]: Black level target for odd col and odd row;
	73h	***AVER_LOCK***	8	21h	Bit[7:4]: lock value to update with current frame black level; Bit[3:0]: lock value to update with previous frame black level +1 / -1;

Page	Address	Name	Width	Default value	Description
	74h	***MODE_CNTL***	8	23h	Bit[7]: BYPASS_BC 1'b1: Bypass digital black control; 1'b0: Don't bypass digital black control; Bit[5:4]: DARKROW_SEL; 2'b00: Select 1~16 of the 16 dark rows; 2'b01: Select 1~8 of the 16 dark rows; 2'b10: Select 5~12 of the 16 dark rows; 2'b11: Select 9~16 of the 16 dark rows; Bit[3]: DGAD_MODE 1'b1: Use this frame black level as AVER; 1'b0: Use last frame black level variety 1 as AVER; Bit[1]: MODE_CTL 1'b1: Auto; 1'b0: Manual; Bit[0]: DIG_MODE_CTL 1'b1: When the black aver is adjust inside the lock, then adjust one more step; 1'b0: When the black aver is adjust inside the lock, then keep the value;
	75h	***AVER_L_E0***	8	RO	Read out black aver for E row E col, this value has been adjusted;
	76h	***AVER_L_O0***	8	RO	Read out black aver for E row O col, this value has been adjusted;
	77h	***AVER_L_E1***	8	RO	Read out black aver for O row E col, this value has been adjusted;
	78h	***AVER_L_O1***	8	RO	Read out black aver for O row O col, this value has been adjusted;
	79h	***AVER_L_E0[9:8]*** ***AVER_L_O0[9:8]*** ***AVER_L_E1[9:8]*** ***AVER_L_O1[9:8]***	8	RO	Bit[7:6]: Read out black level for even col and even row; Bit[5:4]: Read out black level for odd col and even row; Bit[3:2]: Read out black level for even col and odd row; Bit[1:0]: Read out black level for odd col and odd row;
	7ah	***AVER_L_E0[10]*** ***AVER_L_O0[10]*** ***AVER_L_E1[10]*** ***AVER_L_O1[10]***	4	RO	Bit[7]: Read out black level for even col and even row; Bit[6]: Read out black level for odd col and even row; Bit[5]: Read out black level for even col and odd row; Bit[4]: Read out black level for odd col and odd row;
	7bh	***AVER_M_E0***	8	RO	Read out black aver for E row E col, this value has been adjusted;
	7ch	***AVER_M_O0***	8	RO	Read out black aver for E row O col, this value has been adjusted;
	7dh	***AVER_M_E1***	8	RO	Read out black aver for O row E col, this value has been adjusted;
	7eh	***AVER_M_O1***	8	RO	Read out black aver for O row O col, this value has been adjusted;
	7fh	***AVER_M_E0[9:8]*** ***AVER_M_O0[9:8]*** ***AVER_M_E1[9:8]*** ***AVER_M_O1[9:8]***	8	RO	Bit[7:6]: Read out black level for even col and even row; Bit[5:4]: Read out black level for odd col and even row; Bit[3:2]: Read out black level for even col and odd row; Bit[1:0]: Read out black level for odd col and odd row;
	80h	***AVER_M_E0[10]*** ***AVER_M_O0[10]*** ***AVER_M_E1[10]*** ***AVER_M_O1[10]***	4	RO	Bit[7]: Read out black level for even col and even row; Bit[6]: Read out black level for odd col and even row; Bit[5]: Read out black level for even col and odd row; Bit[4]: Read out black level for odd col and odd row;
	81h	***AVER_S_O0***	8	RO	Read out black aver for E row E col, this value has been adjusted;
	82h	***AVER_S_E1***	8	RO	Read out black aver for E row O col, this value has been adjusted;
	83h	***AVER_S_O1***	8	RO	Read out black aver for O row E col, this value has been adjusted;
	84h	***AVER_S_E1***	8	RO	Read out black aver for O row O col, this value has been adjusted;
	85h	***AVER_S_E0[9:8]*** ***AVER_S_O0[9:8]*** ***AVER_S_E1[9:8]*** ***AVER_S_O1[9:8]***	8	RO	Bit[7:6]: Read out black level for even col and even row; Bit[5:4]: Read out black level for odd col and even row; Bit[3:2]: Read out black level for even col and odd row; Bit[1:0]: Read out black level for odd col and odd row;

Page	Address	Name	Width	Default value	Description
	86h	*AVER_S_E0[10]* *AVER_S_O0[10]* *AVER_S_E1[10]* *AVER_S_O1[10]*	4	RO	Bit[7]: Read out black level for even col and even row; Bit[6]: Read out black level for odd col and even row; Bit[5]: Read out black level for even col and odd row; Bit[4]: Read out black level for odd col and odd row;
	87h	*COEF*	8	80h	Black aver adjust coefficient;
	88h	*LM_Rate* *MS_Rate*	8	00h	Bit[7:4]: LM_Rate;When test pattern shift LM_Rate bit to the right on L; Bit[3:0]: MS_Rate;When test pattern shift MS_Rate bit to the right on M;

8.5 Lens Shading Correction Registers

Page	Address	Name	Width	Default value	Description
0	e0h	*OFFSET_REG*	8	00h	Bit[7:0]: Lens shading offset value;
	e1h	*LENS_CTR1*	8	cah	Bit[7]: VFLIP mode control; Bit[6]: HFLIP mode control; Bit[5:3]: Center Y coordinate MSB; Bit[2:0]: Center X coordinate MSB;
	e2h	*Y*	8	e8h	Center Y coordinate LSB;
	e3h	*X*	8	a0h	Center X coordinate LSB;
	e4h	*R_COEF*	8	0fh	Lens shading gain of R;
	e5h	*G_COEF*	8	0fh	Lens shading gain of RG;
	e6h	*B_COEF*	8	0fh	Lens shading gain of B;
	e7h	*G0_COEF*	8	0fh	Lens shading gain of BG;

8.6 Gamma Correction Registers

Page	Address	Name	Width	Default value	Description
1	00h	*XY0*	8	00h	Gamma correction slope coefficients 0;
	01h	*XY1*	8	08h	Gamma correction slope coefficients 1;
	02h	*XY2*	8	10h	Gamma correction slope coefficients 2;
	03h	*XY3*	8	20h	Gamma correction slope coefficients 3;
	04h	*XY4*	8	2ch	Gamma correction slope coefficients 4;
	05h	*XY5*	8	38h	Gamma correction slope coefficients 5;
	06h	*XY6*	8	4dh	Gamma correction slope coefficients 6;
	07h	*XY7*	8	60h	Gamma correction slope coefficients 7;
	08h	*XY8*	8	71h	Gamma correction slope coefficients 8;
	09h	*XY9*	7	82h	Gamma correction slope coefficients 9;
	0ah	*XY10*	7	91h	Gamma correction slope coefficients 10;
	0bh	*XY11*	7	a0h	Gamma correction slope coefficients 11;
	0ch	*XY12*	7	adh	Gamma correction slope coefficients 12;
	0dh	*XY13*	7	bah	Gamma correction slope coefficients 13;
	0eh	*XY14*	7	c6h	Gamma correction slope coefficients 14;

Page	Address	Name	Width	Default value	Description
	0fh	***XY15***	7	d2h	Gamma correction slope coefficients 15;
	10h	***XY16***	7	ddh	Gamma correction slope coefficients 16;
	11h	***XY17***	7	e9h	Gamma correction slope coefficients 17;
	12h	***XY18***	8	00h	Gamma correction slope coefficients 18;
	13h	***COM1***	8	80h	Bit[7]: High bit of Gamma correction slop coefficients; Bit[6:0]: The manual written gamma offset;

8.7 Denoise/BP/EE Registers

Page	Address	Name	Width	Default value	Description
0	98h	***SwiCtr1***	8	0fh	Bit[7]: Stop_Sram--SRAM Control; 1'b0: Enable SRAM; 1'b1: Disable SRAM; Bit[6:4]: Reserved; Bit[3]: Edge_Switch--Edge Enhancement Control; 1'b0: Disable edge enhancement; 1'b1: Enable edge enhancement; Bit[2]: Clu_Switch--Cluster Correction Control; 1'b0: Disable cluster correction; 1'b1: Enable cluster correction; Bit[1]: Bp_Switch-- Bad Pixel Correction Control; 1'b0: Disable bad pixel correction; 1'b1: Enable bad pixel correction; Bit[0]: NR_Switch--Noise Reduction Control; 1'b0: Disable noise reduction; 1'b1: Enable noise reduction;
	99h	***SwiCtr2***	8	0ah	Bit[7]: Cross Talk Correction Control 1; 1'b0: Disable cross talk correction in vertical direction; 1'b1: Enable cross talk correction in vertical direction; Bit[6]: Cross Talk Correction Control 2; 1'b0: Disable cross talk correction in horizontal direction; 1'b1: Enable cross talk correction in horizontal direction; Bit[5]: Proraw_Switch--select mipi signal; 1'b0: Mipi for rawdata; 1'b1: Mipi for RGB; Bit[4]: Raw_Switch--select the rawdata output format; 1'b0: The rawdata processed by BP and NR; 1'b1: Input rawdata; Bit[3]: G_Balance_En--Green Balance Correction Control; 1'b0: Disable green balance; 1'b1: Enable green balance; Bit[2]: S_Area_Show--Show S and VS Area; 1'b0: Normal data; 1'b1: Only S and VS area; Bit[1]: Spot_Noise_Reduction; 1'b0: Disable; 1'b1: Enable; Bit[0]: Bound_Show--Show Edge; 1'b0: Disable; 1'b1: Enable;
	9ah	***BpcCtr***	8	4fh	Bit[7:4]: Bp_TH--threshold for badpixel detection; Bit[3:2]: Clu_Sel(Parameter1) - The Gain Value for Cluster Correction; 2'b00: 1/4; 2'b01: 3/8; 2'b10: 1/2; 2'b11: 3/4; Bit[1:0]: Reserved;

Page	Address	Name	Width	Default value	Description
	9bh	***NRCtr1***	8	18h	Bit[7]: Reserved; Bit[6]: EE_LIMIT_BYPASS; 1'b0: Enable edge enhancement limit; 1'b1: Disable edge enhancement limit; Bit[5]: GAIN_WEAK_EE_BYPASS; 1'b0: Enable weak edge enhancement according to gain; 1'b1: Disable weak edge enhancement according to gain; Bit[4]: BRIGHT_NR_MODSEL; 1'b0: Stronger NR according to current value minus average luminance; 1'b1: Stronger NR according to average luminance minus current value; Bit[3]: BRIGHT_S_ONLY; 1'b0: When enable bright area stronger NR, all bright area stronger NR; 1'b1: When enable bright area stronger NR, only S and VS area stronger NR;
					Bit[2]: BRIGHT_NR_BYPASS; 1'b0: Enable bright area stronger NR; 1'b1: Disable bright area stronger NR; Bit[1]: INTTIME_NR_BYPASS; 1'b0: Enable adaptive NR according to integration time; 1'b1: Disable adaptive NR according to integration time; Bit[0]: GAIN_NR_BYPASS; 1'b0: Enable adaptive NR according to gain; 1'b1: Disable adaptive NR according to gain;
	9ch	***NRCtr2***	8	50h	Bit[7:6]: GAIN_COEF--the Speed of Noise Reduction and Edge Enhance According to Gain_difference with Limit; 2'b00: 0;5x; 2'b01: 1x; 2'b10: 2x; 2'b11: 4x; Bit[5:4]: GAIN_NR_COEF--the Speed of Noise Reduction and Edge Enhance According to Gain_difference without Limit; 2'b00: 0;5x; 2'b01: 1x; 2'b10: 1;5x; 2'b11: 2x; Bit[3:2]: GAIN_ALL_SEL-- the range of Noise Reduction and Edge Enhance According to gain; 2'b00: Start point ~ 255; 2'b01: Start point ~ 511; 2'b10: Start point ~ 1023; 2'b11: Start point ~ 2047; Bit[1:0]: Reserved;
	9dh	***NRCtr3***	8	00h	Bit[7:6]: Int_Tim_COEF--Parameter for Noise Reduction Outdoor - Gain Value of Integration Time; 2'b00: 1/16; 2'b01: 1/8; 2'b10: 1/4; 2'b11: 1/2; Bit[5:0]: Int_tim_th--Parameter for Noise Reduction Outdoor - Integration Time to Judge Outdoor (*32);
	9eh	***NRCtr4***	6	00h	Bit[7:0]: Base_Gl_Gain--the Start Point of Gain for Noise Reduction and Edge Enhance;
	9fh	***NRCtr5***	8	9fh	Bit[7:5]: G_Balance_TH--Threshold for Green Balance(*8); Bit[4:0]: Y_AVER_TH--Y_AVER Threshold for Bright Area NR(*8); When 9b[4]=0, Y_AVER-Y_AVER_TH; When 9b[4]=1, Y_AVER+Y_AVER_TH;
	a0h	***NRCtr6***	8	04h	Bit[7:6]: BRIGHT_NR_COEF--Coefficient of Bright Area NR; 2'b00: 1/4; 2'b01: 1/2; 2'b10: 3/4; 2'b11: 1; Bit[5:4]: Reserved; Bit[3:0]: BRIGHT_Th--Threshold for Bright Area NR(*4), the Larger This Value Is, the Less Intensity of NR for Bright Area;
	a1h	***IntCtr***	8	cfh	Bit[7:4]: Flat_TH--Threshold for Flat Field(*4); Bit[3:0]: Edge_TH--Threshold for Edge Detection(*2);

Page	Address	Name	Width	Default value	Description
	a2h	***EdgCtr1***	8	02h	Bit[7]: Gray_Judge--Gray Area Judge; 1'b0: Disable gray area judge; 1'b1: Enable gray area judge; Bit[6:3]: Reserved; Bit[2]: Edge_Quarter--Quantity of Edges; 1'b0: Quadruple HV edges; 1'b1: Normal quantity of edges; Bit[1:0]: Edg_En_Max--Edge Enhancement Limit; 2'b00: 1/8*Y_CEN; 2'b01: 1/4*Y_CEN; 2'b10: 1/4*Y_CEN; 2'b11: 1/2Y_CEN;
	a3h	***EdgCtr2***	8	33h	Bit[7:4]: Edg_Offset--Intensity Offset of Edge Enhancement at Flat Area; Bit[3:0]: Edge_Base--Intensity of Edge Enhancement; 4'b0000:1/16; 4'b0001:2/16; 4'b0010:3/16; 4'b0011:4/16; 4'b0100:5/16; 4'b0101:6/16; 4'b0110:7/16; 4'b0111:8/16; 4'b1000:9/16; 4'b1001:10/16; others:11/16;
	a4h	***MacCtr1***	8	00h	Bit[7:0]: NR_BASE--Base Intensity of Noise Reduction(*2);
	a5h	***MacCtr2***	8	00h	Bit[7:4]: NR_STRONG--Stronger NR; Bit[3:0]: NR_WEAK--Weaker NR;

8.8 AE Control Registers

Page	Address	Name	Width	Default value	Description
1	61h	***DCG_RATE1*** ***DCG_RATE2***	8	11h	Bit[7:4]: DCG_RATE1; Bit[3:0]: DCG_RATE2;
	62h	***TRI_EXPO_MODE*** ***STEP_NUM***	8	6h	Bit[7]: DCG_MODE ON or OFF; Bit[6:4]:Reserved; Bit[3:0]: Int_time adjust step every frame;
	63h	***GAIN_SEL***	8	01h	Bit[7:1]: Reserved; Bit[0]: GLB_GAIN_L or GLB_GAIN_M for GAIN_ALL;
	64h	***DIG_TAR_MEN*** ***Y_Tar_DG***	8	40h	Bit[7]: Digital gain target modify switch 1'b0: Off; 1'b1: On; Bit[6:0]: Digital gain target(Y_Tar_DG*2);
	65h	***BW_GAIN_TH***	8	10h	Bit[7:0]: BW_GAIN_TH the threshold of change to black and white mode, when glb_gain >bw_th+BW_CONTROL(0x70[3:0]) && int_tim=int_max, will switch to black_white mode;
	66h	***COM8***	8	35h	Bit[7]: 1'b1: AE_TAR; 1'b0: AE_TAR_MODIFY (decrease the target brightness based on the number of over exposure pixels); Bit[6]: 1'b0: Digital gain disable; 1'b1: Digital gain enable; Bit[5]: The high Bit of INT_STEP_60; Bit[4]: The high Bit of INT_STEP_50; Bit[3]: GLB_GAIN0 written is effective when AGC disable; 1'b0: GLB_GAIN0 written disable; 1'b1: GLB_GAIN0 written enable; Bit[2]: 1'b1: AGC Enable; 1'b0: AGC disable; Bit[1]: Group switch 1'b1: On; 1'b0: Off; Bit[0]: AEC Enable control; 1'b0: Disable; 1'b1: Enable;

Page	Address	Name	Width	Default value	Description
	67h	***COM1***	8	8ah	Bit[7]: Reserved; Bit[6]: Minimum STEP control: 1'b1: 2 steps; 1'b0: 1 step; Bit[5:4]: WINDOW_SEL center window select; 2'b00: ROW*12/16 COL*12/16; 2'b01: ROW*10/16 COL*10/16; 2'b10: ROW*8/16 COL*8/16; 2'b11: ROW*6/16 COL*6/16; Bit[3]: Control the adjusting speed of digital gain 1'b0: Y_DIFF_D[7:1] (1times); 1'b1: Y_DIFF_D (2 times); Bit[2:0]: WEIGHT_SEL; 3'b000: 4/8*center+4/8*border; 3'b001: 5/8*center+3/8*border; 3'b010: 6/8*center+2/8*border; 3'b011: 7/8*center+1/8*border; 1'b100~111: Center 100%;
	68h	***Y_AVER***	8	RO	Bit[7:0]: The Y_aver of the current frame;
	69h	***P_PIXEL_OE***	8	RO	Bit[7:0]: The number of the over exposure pixels used to modify the target brightness and the adjusting speed;
	6ah	***GLB_GAIN_L_POST***	8	18h	Bit[7:0]: GLB_GAIN_L_POST register;
	6bh	***INT_TIM_L_POST[15:8]***	8	01h	Bit[7:0]: Real integration time MSB;
	6ch	***INT_TIM_L_POST[7:0]***	8	52h	Bit[7:0]: Real integration time LSB;
	6dh	***DIG_GAIN***	8	10h	Bit[7:0]: The value of DIG_GAIN;
	6eh	***DIG_GAIN_MAX***	8	a4h	Bit[7:4]: The smallest value the target brightness can achieve; (AE_TAR_M=AE_TAR*TAR_BASE1[3:0]/16); The smaller TAR_BASE1[3:0] is, the quicker the AE adjusting, to calculate AE_TAR_M; Bit[3:0]: DIG_GAIN_MAX[3:0]*16 as the limit of DIG_GAIN;
	6fh	***AE_TAR1***	8	4fh	Bit[7]: Reserved; Bit[6:0]: Y target value;Actually,{0x04[6:0],1'b0} is used;
	70h	***BW_ENABLE*** ***BW_CONTROL***	8	15h	Bit[7]: BW_ENABLE(RO); Bit[6]: Reserved; Bit[5:4]: BW_CONTROL2 2'b00: Output the black_white mode automatically; 2'b01: For INFRA_ON control (external hardware control); 2'b10: Show colorized; 2'b11: Show black and white; Bit [3:0]: The gain bound for BW switch(use with 0x65);
	71h	***AE_LOC***	8	88h	Bit[7:4]: Lock for AEC; Bit[3:0]: Lock for AGC;
	72h	***AE_MODE***	8	dah	Bit[7]: AE test mode control 1'b1: Normal; 1'b0: Test mode; Bit[6]: 1'b0: AE adjusts every two frames; 1'b1: AE adjusts every frame enable; Bit[5:4]: G_MIN_SLOPE When INT_TIM >INT_MID; Gain Coefficients: 2'b00: 0; 2'b01: 1; 2'b10: 2; 2'b11: 3; Bit[3:2]: P_OE_SEL (what is P_OE_SEL); 2'b00: /2^15; 2'b01: /2^16; 2'b10: /2^17; 2'b11: /2^18; Bit[1]: 1'b0: Choose 60HZ step; 1'b1: Choose 50HZ step; Bit[0]: AE is adjusted by men; Effective when test mode(0x72[7]==1'b0);
	73h	***AE_SPEED***	8	00h	Bit[7:4]: The speed of adjusting from light to dark; Bit[3:0]: The speed of adjusting from dark to light;

Page	Address	Name	Width	Default value	Description
	74h	***INT_MAX_I2C***	8	88h	Bit[7]: Switch for select the speed when AE adjust form bright to dark; 1'b1: Fast; 1'b0: Slow;(disable in PAL mode) Bit[6]: Reserved; Bit[5:0]: INT_MAX the MAX steps of integral time;
	75h	***INT_MID_I2C***	8	45h	Bit[7:4]: The lock(Bit[7:4]*4) threshold for when the next frame's P_PIXEL_OE is larger than the former frame's P_PIXEL_OE, then update the P_PIXEL_OE value; Bit[3:0]: INT_MID: The integral time when the GLB_MIN begin to become larger in order to adjust the picture more fast;
	76h	***INT_MIN***	8	81h	Bit[7]: 1'b0: One step is the least integration time step; 1'b1: INT_MIN is Bit[6:0]; Bit[6:0]: INT_MIN;
	77h	***INT_STEP_50***	8	52h	Bit[7:0]: The low 8 Bits of the minimum integral time for every step to avoid flicker for 50HZ light, Bit[8] is in 0x66[4] (COM8[4]);
	78h	***INT_STEP_60***	8	1ah	Bit[7:0]: The low 8 Bits of the minimum integral time for every step to avoid flicker for 60HZ light , Bit[8] is in 0x66[5] (COM8[5]);
	79h	***YAVER_LOCK***	8	c0h	Bit[7:0]: YAVER_LOCK: Threshold for AE adjust from bright to dark;
	7ah	***DIG_LOCK_TH*** ***Y_OV_TH***	8	82h	Bit[7:4]: DIG_LOCK_TH, lock for DIG_GAIN; Bit[3:0]: Y_OV_TH, When (Y_AVER-AE_TAR) > Y_OV_TH[3:0]*16, if AE adjusts every frame enabled,it will adjusts every frame;
	7bh	***TAR_BASE0***	8	03h	Bit[7:4]: (192+Bit[7:4]*4) as threshold to judge one pixel whether to be over exposure pixel; Bit[3:0]: used to control the start of AE;
	7ch	***TAR_BASE1***	8	84h	Bit[7:4]: Is used to modify the difference of Y_AVER and modified AE_TAR); The smaller TAR_BASE1[7:4] is, the slower the AE adjusting; Bit[3:0]: It is set to limit the speed of AE to avoid over adjusting; The bigger it is, the quicker the AE adjusting;
	7dh	***YBRIGHT_TH***	8	b5h	Bit[7:4]: The speed of AE to adjust from dark to bright; The bigger it is, the quicker the AE adjusting; Bit[3:0]: YBRIGHT_TH[3:0]*16 as the threshold for Y_AVER to judge outdoor scene;
	7eh	***INT_TIM_TH***	8	50h	Bit[7:0]: Threshold for INT_TIME to judge outdoor scene;
	7fh	***GAIN_ALL***	8	RO	GAIN_ALL=GLOBE_GAIN*DIG_GAIN;
	80h	***GLB_GAIN_L_POST***	8	18h	Bit[7:0]: The value of gain_or_last to get the GLB_GAIN_L through some operation;
	81h	***GLB_MIND1***	8	18h	Bit[7:0]: GLB_MIN1 8 Bits;
	82h	***GLB_MAXD1***	8	4bh	Bit[7:0]: GLB_MAX1 8 Bits;
	83h	***GLB_MIND2***	8	4bh	Bit[7:0]: GLB_MIN2 8 Bits;
	84h	***GLB_MAXD2***	8	6bh	Bit[7:0]: GLB_MAX2 8 Bits;
	85h	***GLB_MAXD3***	8	ffh	Bit[7:0]: GLB_MAX3 8 Bits;
	86h	***INT_S_MAX***	8	08h	Bit[7:6]: Reserved; Bit[5:0]: INT_S_MAX;
	87h	***Mgain_MAX***	8	7fh	Bit[7:0]: Mgain_MAX 8 Bits;
	88h	***Mgain_MIN***	8	10h	Bit[7:0]: Mgain_MIN 8 Bits;
	89h	***LM_Rate*** ***MS_Rate***	8	44h	Bit[7:4]: LM_Rate 4 Bits 0X to FX (actually :1X to 16X); Bit[3:0]: MS_Rate 4 Bits 0X to FX (actually :1X to 16X);
	8ah	***INT_M_MAX***	8	40h	Bit[7]: Reserved; Bit[6:0]: INT_M_MAX 7 Bits;
	8bh	***Sgain_MAX***	8	7fh	Bit[7:0]: Sgain_MAX 8 Bits;
	8ch	***Sgain_MIN***	8	10h	Bit[7:0]: Sgain_MIN 8 Bits;

Page	Address	Name	Width	Default value	Description
	8dh	***INT_TIM_M_POST***	8	40h	Bit[7]: Reserved; Bit[6:0]: INT_TIM_M 7 Bits;
	8eh	***INT_TIM_S_POST***	8	08h	Bit[7:6]: Reserved; Bit[5:0]: INT_TIM_S_POST;
	8fh	***GLB_GAIN_M_POST***	8	19h	Bit[7:0]: GLB_GAIN_M_POST 8 Bits;
	90h	***GLB_GAIN_S_POST***	8	28h	Bit[7:0]: GLB_GAIN_M_POST 8 Bits;
	91h	***HDR_RATE1_POST*** ***HDR_RATE2_POST***	8	22h	Bit[7:4]: HDR_RATE1_POST 4 Bits for HDR; Bit[3:0]: HDR_RATE2_POST 4 Bits for HDR;
	92h	***RATE_ADD*** ***RAW_AE_EN*** ***AE_AUTO***	8	89h	Bit[7:4]: RATE_ADD 4 Bits RATE1 add RATE 2; Bit[3:2]: RAW_AE_EN 2 Bits Y_AVER DataIn sel: 2'b00: Y_inD; 2'b10: Y_inL; 2'b01: Y_inC; 2'b11: Y_YUV_IN; Bit[1:0]: AE_AUTO 2 Bits, AE ON or OFF (Control inside the AE Module);

8.9 AWB Control Registers

Page	Address	Name	Width	Default value	Description
1	a0h	***AWB_CTR_SET***	8	08h	Bit[7]: For Manual Write RGAIN/BGAIN Mode: 1'b0: RGAIN/BGAIN can be writed no matter AWB_EN=0 strides over VSYNC's negedge or not; 1'b1: RGAIN/BGAIN can't be writed, if AWB_EN=0 doesn't stride over VSYNC's negedge; Bit[6]: 1'b0: Wipe off gain's infection or not base on the condition controlled by Bit[5] and Bit[4]: 1'b1: Select the pixels wiped off gain's infection to do white balance; Bit[5]: 1'b0: When r_aver>g_aver&&r_gain>base_r_gain or b_aver<g_aver&&b_gain<base_b_gain and |r_aver-g_aver|>limit, select r wiped off gain's infection to do white balance, the same to b; 1'b1: Select the pixels not wiped off gain's infection to do white balance, no matter the condition accords with the setting or not; Bit[4]: 1'b0: When white pixel amount doesn't achieve the limit, select the pixels wiped off gain's infection to do white balance;
					1'b1: Select the pixels not wiped off gain's infection to do white balance, no matter the condition accords with the setting or not; Bit[3]: PURE_EN 1'b0: Disable; 1'b1: Enable; Bit[2]: ADJ_MODEL; 1'b1: Add offset; 1'b0: Without offset; Bit[1:0]: Auto white balance update speed;
	a1h	***AWB_TH1_SET***	8	03h	Bit[7:4]: Reserved; Bit[3:0]: AWB_LOCK, Auto white balance lock boundary;
	a2h	***BLU_GAIN_TH1***	8	0eh	Bit[7:6]: Reserved; Bit[5:0]: Minimum blue gain for indoor scene;
	a3h	***BLU_GAIN_TH2***	8	34h	Bit[7:6]: Reserved; Bit[5:0]: Maximum blue gain for indoor scene;
	a4h	***RED_GAIN_TH1***	8	08h	Bit[7:6]: Reserved; Bit[5:0]: Minimum red gain for indoor scene;
	a5h	***RED_GAIN_TH2***	8	21h	Bit[7:6]: Reserved; Bit[5:0]: Maximum red gain for indoor scene;
	a6h	***COUNT_EN***	8	04h	White pixels count threshold; '1' is equal to 1024 pixels;
	a7h	***BASE_B_GAIN***	8	20h	Bit[7:6]: Reserved; Bit[5:0]: Base B gain;

Page	Address	Name	Width	Default value	Description
	a8h	***BASE_R_GAIN***	8	14h	Bit[7:6]: Reserved; Bit[5:0]: Base R gain;
	a9h	***AWB_GB_LIM***	8	1fh	Bit[7]: Reserved; Bit[6:0]: AWB criterion: B, the threshold of |G-B|;
	aah	***AWB_GR_LIM***	8	1fh	Bit[7]: Reserved; Bit[6:0]: AWB criterion: R, the threshold of |G-R|;
	abh	***AWB_BR_LIM***	8	2fh	Bit[7:0]: AWB criterion: BR;
	ach	***AWB_Y_TH***	8	86h	Bit[7:4]: AWB criterion: AWB_Y_HIG; Bit[3:0]: AWB criterion: AWB_Y_LOW;
	adh	***CB_CR_PURE***	8	95h	Pure B or Pure R Threshold; Bit[7:4]: Pure b threshold; Bit[3:0]: Pure r threshold;
	aeh	***F_LIGHT_TH***	8	57h	Bit[7:4]: B limit to estimate F light; Bit[3:0]: R limit to estimate F light;
	afh	***DIG_SLOPE***	8	05h	Bit[7:5]: GAIN_offset; Bit[4:0]: Color gain slope;
	b0h	***BLUE_GAIN***	6	20h	Bit[7:6]: Reserved; Bit[5:0]: Blue gain;
	b1h	***RED_GAIN***	6	14h	Bit[7:6]: Reserved; Bit[5:0]: Red gain;
	b2h	***OUT_STATE*** ***IS_A_LIGHT*** ***Cb_pure*** ***Cr_pure*** ***AWB_ENABLE*** ***GN_GAIN***	8	09h	Bit[7]: Out_state symbol(RO); Bit[6]: A light symbol(RO); Bit[5]: B pure symbol(RO); Bit[4]: R pure symbol(RO); Bit[3]: AWB_ENABLE: 1'b1: Auto; 1'b0: Manual; Bit[2:0]: G Channel Gain (Bit[2:0] is used as Green Gain[5:3]);
	b3h	***GLGAINREG***	7	33h	Bit[7]: Reserved; Bit[6:4]: G1 Gain (Used as Green gain [2:0] of even column); Bit[3]: Reserved; Bit[2:0]: G2 Gain (Used as Green gain[2:0] of odd column);
	b4h	***F_OFFSET***	8	00h	The Offset of F Light; Bit[7]: Sign of blue offset: 1'b0: Minus blue gain; 1'b1: Add blue gain; Bit[6:4]: Blue offset; Bit[3]: Sign of red offset: 1'b0: Minus red gain; 1'b1: Add red gain; Bit[2:0]: Red offset;
	b5h	***NF_OFFSET***	8	00h	The Offset of non-F Light; Bit[7]: Sign of blue offset: 1'b0: Minus blue gain; 1'b1: Add blue gain; Bit[6:4]: Blue offset Bit[3]: Sign of red offset: 1'b0: Minus red gain; 1'b1: Add red gain; Bit[2:0]: Red offset;
	b6h	***OUTDOOR_EN*** ***DE_GAIN_EN_AUTO*** ***CBCR_EN*** ***GAIN_DIFF***	8	58h	Bit[7]: Outdoor_en, outdoor model control: 1'b0: Off; 1'b1: On; Bit[6]: Increase White Pixels: 1'b0: Disable; 1'b1: Enable; Bit[5]: Reserved; Bit[4:0]: Gain_diff (Used to wipe off gain function);
	b7h	***AVER_CBCR_LIM***	8	44h	Bit7:4]: The threshold of B_AVER-G_AVER to judge wipe off gain or not; If B_AVER-G_AVER>AVER_GB_LIM, don't wipe off gain (Used with 0xa0[5]); Bit3:0]: The threshold of R_AVER-G_AVER , The same as AVER_GB_LIM;

Page	Address	Name	Width	Default value	Description
	b8h	*B_GAIN_LOW_OUT*	6	0dh	Bit[7:6]: Reserved; Bit[5:0]: Minimum blue gain for outdoor scene;
	b9h	*B_GAIN_HIG_OUT*	6	16h	Bit[7:6]: Reserved; Bit[5:0]: Maximum blue gain for outdoor scene;
	bah	*R_GAIN_LOW_OUT*	6	09h	Bit[7:6]: Reserved; Bit[5:0]: Minimum red gain for outdoor scene;
	bbh	*R_GAIN_HIG_OUT*	6	1ah	Bit[7:6]: Reserved; Bit[5:0]: Maximum red gain for outdoor scene;
	bch	*PURE_PIXEL_TH1*	8	42h	Threshold for restraint the green and pure pixel;
	bdh	*PURE_PIXEL_TH2*	8	88h	Threshold for restraint the blue and yellow pixel;
	beh	*DAT_L_OFFSET*	8	00h	Long integral image offset in low light;
	bfh	*DAT_M_OFFSET*	8	00h	Middle integral image offset in low light;
	c0h	*DAT_S_OFFSET*	8	00h	Short integral image offset in low light;

8.10 Color Correction Registers

Page	Address	Name	Width	Default value	Description
1	2ch	*TARGET2*	8	93h	Bit[7:0]: TARGET2;
	2dh	*TARGET3*	8	04h	Bit[7:0]: TARGET3;
	2eh	*TARGET4*	8	87h	Bit[7:0]: TARGET4;
	2fh	*TARGET6*	8	88h	Bit[7:0]: TARGET6;
	30h	*TARGET7*	8	82h	Bit[7:0]: TARGET7;
	31h	*TARGET8*	8	8dh	Bit[7:0]: TARGET8;
	32h			01h	Bit[6]: DEC_CTRL[2], gain selection 1'b1: GAIN_ALL[9:2]; 1'b0: GAIN_ALL[8:1]; Bit[5:4]: DEC_CTRL[1], gain coef selection; 2'b00: GLB_GAIN_ABS; 2'b01: GLB_GAIN_ABS/2; 2'b1x: GLB_GAIN_ABS/4; Bit[1]: ADJ_EN, TARGET_ADJ_SEL coef; 1'b1: Disable; 1'b0: Enable; Bit[0]: COLOR_DIS, target selection; 1'b1: Outdoor target; 1'b0: Normal target;
	33h	*GLB_GAIN_TH*	4	04h	Bit[3:0]: Global gain threshold;
	34h	*TARGET2_OUT*	8	95h	Bit[7:0]: Outdoor TARGET2;
	35h	*TARGET3_OUT*	8	0Bh	Bit[7:0]: Outdoor TARGET3;
	36h	*TARGET4_OUT*	8	86h	Bit[7:0]: Outdoor TARGET4;
	37h	*TARGET6_OUT*	8	94h	Bit[7:0]: Outdoor TARGET6;
	38h	*TARGET7_OUT*	8	06h	Bit[7:0]: Outdoor TARGET7;
	39h	*TARGET8_OUT*	8	99h	Bit[7:0]: Outdoor TARGET8;

8.11 Saturation/Brightness Control Registers

Page	Address	Name	Width	Default value	Description
1	50h	***SAT_CTR1***	8	20h	Bit[7]: BRIGHT_EN 1'b1: Enable; 1'b0: Disable; Bit[6:0]: Y_PIXEL_TH, Y threshold;

Page	Address	Name	Width	Default value	Description
	51h	***SAT_CTR2***	8	8Fh	Bit[7:4]: YAVER_TH Bit[3:0]: GRAY_TH, Gray threshold;
	52h	***SAT_CTR3***	8	10h	Bit[4]: SAT_MODE, saturation mode selection; 1'b1: With Y coef; 1'b0: Without Y coef; Bit[3]: GRAY_DENOISE_SWITCH; 1'b1: {GRAY_SCALE[2:0],1'b0}; 1'b0: GRAY_SCALE[3:0]; Bit[2]: GRAY_EN 1'b1: Enable; 1'b0: Disable; Bit[1]: CB_COEF[8] Bit[0]: CR_COEF[8]
	53h	***CB_COEF_D***	8	80h	Bit[7:0]: CB_COEF[7:0]
	54h	***CR_COEF_D***	8	80h	Bit[7:0]: CR_COEF[7:0]
	55h	***Y_COEF***	8	40h	Bit[7:0]: Y_COEF, Y coefficient
	56h	***GAIN_TH***	7	40h	Bit[7:0]: GAIN_TH, gain threshold
	57h	***BRIGHT***	8	00h	Bit[7:0]: BRIGHT, signed value
	58h	***DARK_ADD_TH***	8	60h	Bit[7]: DARK_ADD_SWITCH 1'b1: Enable; 1'b0: Disable; Bit[6:0]: DARK_ADD_TH, dark threshold;

8.12 Output Data Format Registers

Page	Address	Name	Width	Default value	Description
1	c8h	***COM7***	8	00h	Bit[7:4]: LSB for VHREF; Bit[3]: RAW_TEST_EN, MIPI input selection: 1'b1: Raw Data; 1'b0: YUV; Bit[2]: BAYRAW_EN, raw data selection: 1'b1: Process data output; 1'b0: Bayer raw data output; Bit[1]: DOMAIN_SEL, Domain selection; Bit[0]: RAW_FLAG, raw data output enable: 1'b1: Enable; 1'b0: Disable; Declaration for reg: 3'b000: YUV; 3'b001: RAW; 3'b011: Y; 3'b101: Process Raw;

Page	Address	Name	Width	Default value	Description
	c9h	***COM10***	8	04h	Bit[7]: DAT_MODE, output data selection(use with MAN_VALU); 1'b1: MAN_VALU; 1'b0: Original data; Bit[6]: MAN_VALU; Bit[5]: SYNC_MODE, sync signals selection(use with MAN_VALU); 1'b1: MAN_VALU; 1'b0: Original data; Bit[4]: HREF_MODE 1'b1: There's href during Vblank; 1'b0: No href during Vblank; Bit[3]: HOUT_SEL, hsync output selection; 1'b1: HSYNC; 1'b0: HREF; Bit[2]: VOUT_SEL, vsync output selection; 1'b1: VSYNC; 1'b0: VSYNC_IMAGE; Bit[1]: The polarity of VSYNC; 1'b1: Active low; 1'b0: Active high; Bit[0]: The polarity of HSYNC; 1'b1: Active low; 1'b0: Active high;
	cfh	***COM3***	8	08h	Bit[7:6]: YUV_ORDER, the order of YUV output; 2'b00: YCbYCr; 2'b01: CbYCrY; 2'b10: YCrYCb; 2'b11: CrYCbY; Bit[5:4]: OUT_CTRL; 2'b00: Only parallel output; 2'b01: Only AHD output; 2'b1x: Both parallel & AHD output; Bit[3]: CBCR_SW, control MIPI C channel output; 1'b0: CR; 1'b1: CB; Bit[2]: CROSS_CTRL, control data during blank; Bit[1]: AE_OP_MARK, mark AE operation pixel; 1'b0: Disable; 1'b1: Enable; Bit[0]: WHITE_EN, mark white pixel; 1'b0: Disable; 1'b1: Enable;
	d0h	***COM4***	8	00h	Bit[7]: Manual data(use with MANU/MANV) 1'b0: Disable; 1'b1: Enable; Bit[6]: Inverse data 1'b0: Disable; 1'b1: Enable; Bit[5]: Signed data flag 1'b0: Disable; 1'b1: Enable; Bit[4]: BT656_EN 1'b0: Disable; 1'b1: Enable; Bit[3:0]: Skip frame counter;
	d1h	***MANU***	8	80h	Bit[7:0]: Manual U value;
	d2h	***MANV***	8	80h	Bit[7:0]: Manual V value;
	d3h	***NUMBER_CNTL0***	8	3Ch	Bit[7:0]: NUMBER_JUD of VSYNC_CNT;
	d2h	***NUMBER_CNTL1***	8	3Ch	Bit[7:0]: NUMBER_ADJ of VSYNC_CNT;

8.13 Windowing Registers

8.13.1 Analog Windowing Registers

Page	Address	Name	Width	Default value	Description
0	05h	***SC_CNTL5***	8	61h	Bit[0]: WIN_EN: 1'b1: Windows function on; 1'b0: Windows function off;
	14h	***WINX_ST_LOCK_L***	8	00h	LSB of control the window's edge x start;
	15h	***WINX_ED_LOCK_L***	8	9fh	LSB of control the window's edge x end;
	16h	***WINX_ED_LOCK_H*** ***WINX_ST_LOCK_H***	6	20h	Bit[5:4]: HSB of control the window's edge x end; Bit[1:0]: HSB of control the window's edge x start;
	17h	***WINY_ST_LOCK_L***	8	1eh	LSB of control the window's edge y start;
	18h	***WINY_ED_LOCK_L***	8	edh	LSB of control the window's edge y end;
	19h	***WINY_ED_LOCK_H*** ***WINY_ST_LOCK_H***	7	30h	Bit[6:4]: HSB of control the window's edge y end; Bit[2:0]: HSB of control the window's edge y start;

8.13.2 Digital Windowing Registers

Page	Address	Name	Width	Default value	Description
1	cah	***HSTART_H***	8	00h	Bit[7:0]: HSTART[10:3], Output Format-Horizontal Frame(HREF column)start;
	cbh	***HSTOP_H***	8	A0h	Bit[7:0]: HSTOP[10:3], Output Format-Horizontal Frame(HREF column)end;
	cch	***VSTART_H***	8	00h	Bit[7:0]: VSTART[10:3], Output Format-Vertical Frame(row)start;
	cdh	***VSTOP _H***	8	78h	Bit[7:0]: HSTOP[10:3], Output Format-Vertical Frame(row)end;

Page	Address	Name	Width	Default value	Description
	ceh	***VHREF***	8	00h	Bit[7:6]: MSB of VREF end low 2 bits(high 8 bits at VSTOP[7:0]); Bit[5:4]: MSB of VREF start low 2 bits(high 8 bits at VSTART[7:0]); Bit[3:2]: MSB of HREF end low 2 bits(high 8 bits at HSTOP[7:0]); Bit[1:0]: MSB of HREF start low 2 bits(high 8 bits at HSTART[7:0]);

8.14 HDR Registers

Page	Address	Name	Width	Default value	Description
2	4ah	***LDINT_bypass*** ***AE_DATA_SEL*** ***Multiple_Exposure_mode*** ***HDR_on_off***	8	00h	Bit[7:6]: Reserved Bit[5]: LDINT_bypass: 1'b0:LDINT is avail,1'b1:LDINT is bypass Bit[4]: AE_DATA_SEL: 1'b0: Y_aver is from bayer data, 1'b1: Y_aver is from Bright data Bit[1]: Multiple_Exposure_mode: 1'b0: two -exposure HDR, 1'b1: three-exposure HDR Bit[0]: HDR_on_off: 1'b0: HDR mode off, 1'b1:HDR mode on

Page	Address	Name	Width	Default value	Description
	4bh	***Exposure_rate_index2*** ***Exposure_rate_index1***	8	22h	Bit[7:4]: Exposure_rate2 Bit[3:0]: Exposure_rate1
	4ch	***Exposure_rate_Delay*** ***Exposure_rate_SEL***	8	00h	Bit[7:2]: Reserved Bit[1]: Exposure_rate_index frame delay 1'b0: No Frame delay, 1'b1: One Frame Delay Bit[0]: 1'b0: Auto rate;1'b1: Manual rate
	51h	***Ghost_remove_mode***	8	01h	Bit[7:2]: Reserved Bit[1:0]: 2'b00: L base 1, 2'b01: S base, 2'b10: L base 2
	52h	***Hstrength***	8	08h	Bit[7:6]: Reserved Bit[5:0]: Strength for radiance map, 0 ~ 1.111 range
	53h	***SetRmapMax_h***	8	00h	Bit[7:0]: Radiance Map Max value high byte
	54h	***SetRmapMax_m***	8	00h	Bit[7:0]: Radiance Map Max value middle byte
	55h	***SetRmapMax_l***	8	00h	Bit[7:0]: Radiance Map Max value low byte
	56h	***AutoSetRmapMax***	8	01h	Bit[7:0]: 1'b0: 0ff(manual), 1'b1: on(auto)
	57h	***SetRmapMin***	8	00h	Bit[7:0]: Set Radiance Map Min value
	58h	***COMREG58***	8	00h	Bit[7]: AutoShadowCompensation, Bit[6]: ShadowCompesationMode, Bit[5]: AutoHightlightCompensation, Bit[4]: HighlightCompesationMode, Bit[3]: 1'b0: L data bp is off, 1'b1: L data bp is on Bit[2]: 1'b0: M\S data bp is off, 1'b1: M\S data bp is on Bit[1:0]: RadianceMapMode 2'b00: Mode 0, 2'b01: Mode 1, 2'b10: Mode 2
	59h	***LPF_Strength***	8	03h	Bit[7:5]: Reserved Bit[3:0]: 2'b00: LPF off, 2'b01: low, 2'b10: middle, 2'b11: high
	5ah	***LPF_C_LINE***	8	00h	Bit[7:4]: Reserved Bit[2:0]: GLB_GAIN of LPF_ADJ 's mode, 000-111
	5bh	***SetShadowStrength***	8	00h	Bit[7:0]: 0 ~ 255, Shadow Strength input, 0~1.1111111 range
	5ch	***SetShadowRange***	8	20h	Bit[7:0]: 0 ~ 127, Shadow Range input
	5dh	***SetHighlitStrength***	8	00h	Bit[7:0]: 0 ~ 255, Highlight Strength input, 0~1.1111111 range
	5eh	***SetHighlitRange***	8	40h	Bit[7:0]: 0 ~ 127, Highlight Range input
	5fh	***ShadowStrengthMult***	8	10h	Bit[7:0]: Shadow Strength Multiply, 0 ~11.1111 range
	60h	***ShadowRangeMult***	8	10h	Bit[7:0]: Shadow Range Multiply, 0 ~11.1111 range
	61h	***HighlitStrengthMult***	8	10h	Bit[7:0]: Highlight Strength Multiply, 0 ~11.1111 range
	62h	***HighlitRangeMult***	8	10h	Bit[7:0]: Highlight Range Multiply, 0 ~11.1111 range
	63h	***Image_Select***	8	00h	Bit[7:2]: Reserved Bit[1:0]: 0: Channel 1 video of long exposure 1: Channel 2 video of short exposure 2: Channel 3 video of very short exposure 3: HDR
	64h	***ShadowStrength***	8	RO	Bit[7]: 10 ~ 255, Shadow Strength output, 0~1.1111111 range
	65h	***HighlightStrength***	8	RO	Bit[7:6]: 0 ~ 255, Highlight Strength output, 0~1.1111111 range

Page	Address	Name	Width	Default value	Description
	66h	***RmapMax***	8	RO	Bit[7:0]: Radiance Map Max value high byte
	67h	***RmapMax***	8	RO	Bit[7:0]: Radiance Map Max value middle byte
	68h	***RmapMax***	8	RO	Bit[7:0]: Radiance Map Max value low byte
	69h	***LPF_TH***	8	00h	Bit[7:0]: The threshold of LPF_ADJ
	6ah	***M_YAVER***	8	RO	Bit[7:0]: M_YAVER
	6bh	***M_Offset***	8	50h	Bit[7:0]: M_YAVER of M_S_Threshold_auto's offset
	6ch	***LPF_Strength_ADJ***	8	RO	Bit[7:0]: LPF_Strength of GLB_GAIN 's offset
	6dh	***WF_COEF_M*** ***WF_COEF_S***	8	44h	Bit[7:4]: WF_COEF_M, M_Y_AVER 's coef Bit[3:0]: WF_COEF_S, S_Y_AVER 's coef

8.15 Test Pattern Registers

Page	Address	Name	Width	Default value	Description
0	94h	***TEST_MODE***	8	00h	Bit[7:0]: 8'h00(default): Output normal data. Bit[7]: TEST_MODE_EN: 1'b0: Overlay mode; 1'b1: Test_mode. Bit[6:5]: Test Mode: 2'b00: Color bar pattern; 2'b01: Gradual pattern; 2'b10: Manual write R/G/B; 2'b11: Output normal data. Bit[4]: Pattern Direction: 1'b0: Vertical; 1'b1: Horizontal. Bit[3:0]: Gradual pattern mode control.
	95h	***MAN_R***	8	80h	Define R value.
	96h	***MAN_G***	8	80h	Define G value.
	97h	***MAN_B***	8	80h	Define B value.

9. Package Dimensions

(Unit: mm)

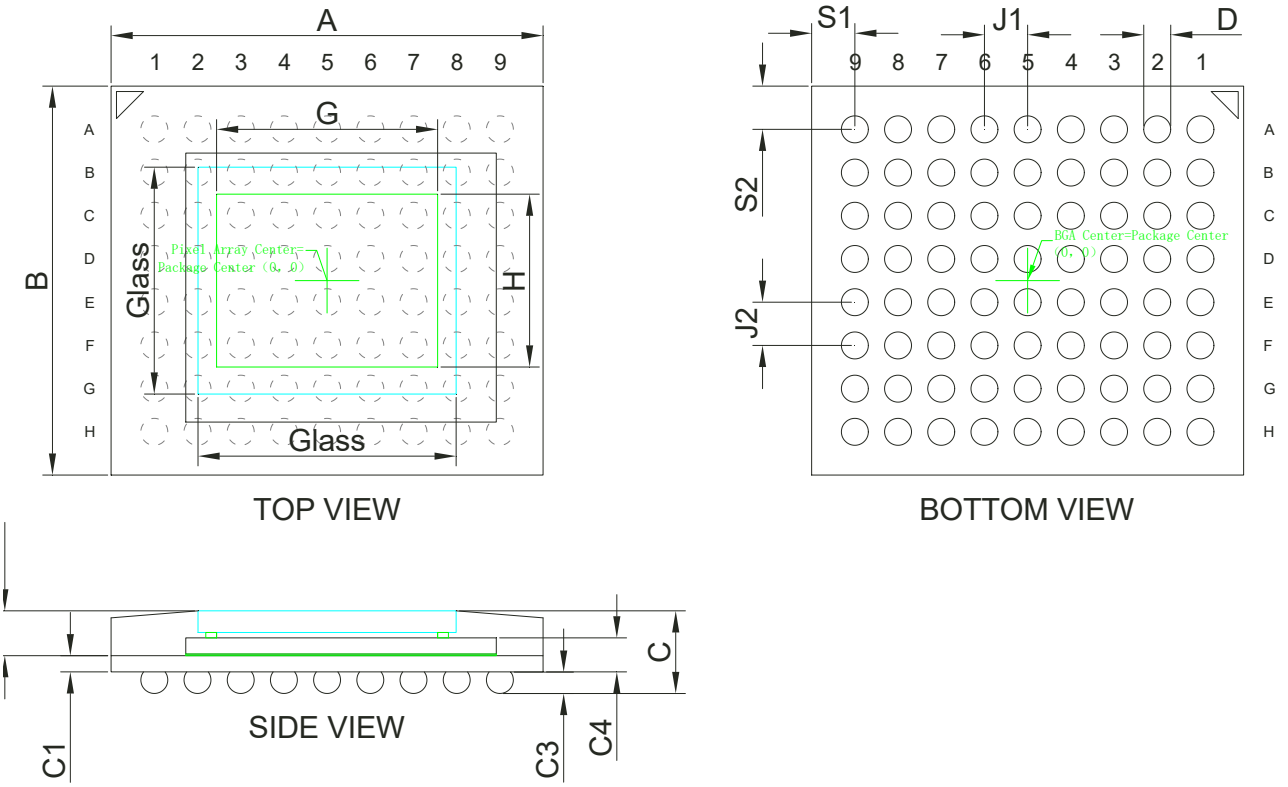


Figure 9- 1 imBGA dimension description

1. Glass Thickness:400 μ m
2. Pixcel Array Center=Package Center

Table 9- 1 imBGAP Pin Descriptions

Parameter	Symbol	Nominal	Min	Max
		Millimeters		
Substrate Dimension X	A	8.000	7.900	8.100
Substrate Dimension Y	B	7.200	7.100	7.300
Package Height	C	1.530	1.430	1.630
Substrate Thickness	C1	0.300	0.260	0.340
Thickness from top glass surface to substrate	C2	0.830	0.730	0.930
Ball Height	C3	0.400	0.350	0.450
Ball Diameter	D	0.500	0.450	0.550
Glass Dimension X	E	4.780	4.730	4.830
Glass Dimension Y	F	4.200	4.150	4.250

Parameter	Symbol	Nominal	Min	Max
		Millimeters		
Active area Dimension X	G	4.094	3.994	4.194
Active area Dimension Y	H	3.199	3.099	3.299
Total Ball Count	\	72.000	\	\
Ball Count X axis	\	9.000	\	\
Ball Count Y axis	\	8.000	\	\
Pins Pitch X axis	J1	0.800	0.790	0.810
Pins Pitch Y axis	J2	0.800	0.790	0.810
Edge to Ball Center Distance along X	S1	0.800	0.790	0.810
Edge to Ball Center Distance along Y	S2	0.800	0.790	0.810

Table 9- 2 Pin symbol

	1	2	3	4	5	6	7	8	9
A	VSSA	VSSA	MCU_SCL_M	MCU_SCL_S	SCL	VSSA	XPD	VSSA	VSSA
B	VDD3A	VDD3A	MCU_SDA_M	MCU_SDA_S	SDA	VDD3A	TM	VDD3A	VDD3A
C	VTN	ID_SEL	E2PROM_SEL	VSSD	VDDD	VDDPL	VCLK	DVP0/VSYNC	DVP1
D	VR	MASTER_EN	INTR	VSSD	VDDD	VDDD	FSYNC	DVP2	DVP3
E	VTOUT	VSSDAC	XRST	VSSD	VDDD	VDDD	HSYNC	DVP4	DVP5
F	VRH	VSSC	VDD3C	VSSD	VSSD	VDDD	VDDD	VSSD	XCLK
G	VDD3A	CVP_M	MDN1	MCN	MDN0	DVP8	DVP6	VDDIO	VDDIO
H	VSSD	CVP_P	MDP1	MCP	MDP0	DVP9	DVP7	VDDIO	VSSD

Table 9- 3 Pin Descriptions

Pin Number	Name	Pin Type	Function/Description
A1	VSSA	GROUND	Analog ground (2.8V)
A2	VSSA	GROUND	Analog ground (2.8V)
A3	MCU_SCL_M	I/O	MCU Master SCL
A4	MCU_SCL_S	I/O	MCU slave SCL
A5	SCL	I/O	IIC CLK
A6	VSSA	GROUND	Analog ground (2.8V)
A7	XPD	Input	External Power down signal
A8	VSSA	GROUND	Analog ground (2.8V)
A9	VSSA	GROUND	Analog ground (2.8V)
B1	VDD3A	POWER	Analog power (2.8V)
B2	VDD3A	POWER	Analog power (2.8V)
B3	MCU_SDA_M	I/O	MCU Master SDA
B4	MCU_SDA_S	I/O	MCU slave SDA
B5	SDA	I/O	IIC DATA

Pin Number	Name	Pin Type	Function/Description
B6	VDD3A	POWER	Analog power (2.8V)
B7	TM	I/O	TEST MODE
B8	VDD3A	POWER	Analog power (2.8V)
B9	VDD3A	POWER	Analog power (2.8V)
C1	VTN	Output	CP VTN output
C2	ID_SEL	Input	IIC address select
C3	E2PROM_SEL	Input	E2PROM address select
C4	VSSD	GROUND	Digital ground (1.2V）
C5	VDDD	POWER	Digital power (1.2V）
C6	VDDPL	POWER	PLL Digital power (1.2V）
C7	VCLK	I/O	clock output
C8	DVP0/VSYNC	Output	DVP bit 0/Vsync
C9	DVP1	Output	DVP bit 1
D1	VR	Output	Analog VREF output
D2	MASTER_E	Input	Master-Slave selection
D3	INTR	Input	Interrupt output
D4	VSSD	GROUND	Digital ground (1.2V）
D5	VDDD	POWER	Digital power (1.2V）
D6	VDDD	POWER	Digital power (1.2V）
D7	FSYNC	Output	Frame synchronization signal
D8	DVP2	Output	DVP bit 2
D9	DVP3	Output	DVP bit 3
E1	VTOUT	Output	TMUX output
E2	VSSDAC	GROUND	Analog ground (Video DAC)
E3	XRST	Input	External Reset Signal
E4	VSSD	GROUND	Digital ground (1.2V）
E5	VDDD	POWER	Digital power (1.2V）
E6	VDDD	POWER	Digital power (1.2V）
E7	HSYNC	I/O	Horizontal synchronization signal
E8	DVP4	Output	DVP bit 4
E9	DVP5	Output	DVP bit 5
F1	VRH	Output	Analog VPCP output
F2	VSSC	GROUND	CP GROUND (2.8V)
F3	VDD3C	POWER	CP Analog power (2.8V)
F4	VSSD	GROUND	Digital ground (1.2V）
F5	VSSD	GROUND	Digital ground (1.2V）
F6	VDDD	POWER	Digital power (1.2V）
F7	VDDD	POWER	Digital power (1.2V）

Pin Number	Name	Pin Type	Function/Description
F8	VSSD	GROUND	Digital ground (1.2V）
F9	XCLK	Input	system clock input
G1	VDD3A	POWER	Analog power (2.8V)
G2	CVP_M	Output	Differential AHD negative output signal
G3	MDN1	Output	MIPI negative output data 1
G4	MCN	Output	MIPI negative output clock
G5	MDN0	Output	MIPI negative output data 0
G6	DVP8	Output	DVP bit 8
G7	DVP6	Output	DVP bit 6
G8	VDDIO	POWER	I/O power (2.8/1.8V)
G9	VDDIO	POWER	I/O power (2.8/1.8V)
H1	VSSD	GROUND	Digital ground (1.2V）
H2	CVP_P	Output	Differential AHD positive output signal
H3	MDP1	Output	MIPI positive output data 1
H4	MCP	Output	MIPI positive output clock
H5	MDP0	Output	MIPI positive output data 0
H6	DVP9	Output	DVP bit 9
H7	DVP7	Output	DVP bit 7
H8	VDDIO	POWER	I/O power (2.8/1.8V)
H9	VSSD	GROUND	Digital ground (1.2V）

10. Application Timing Diagram

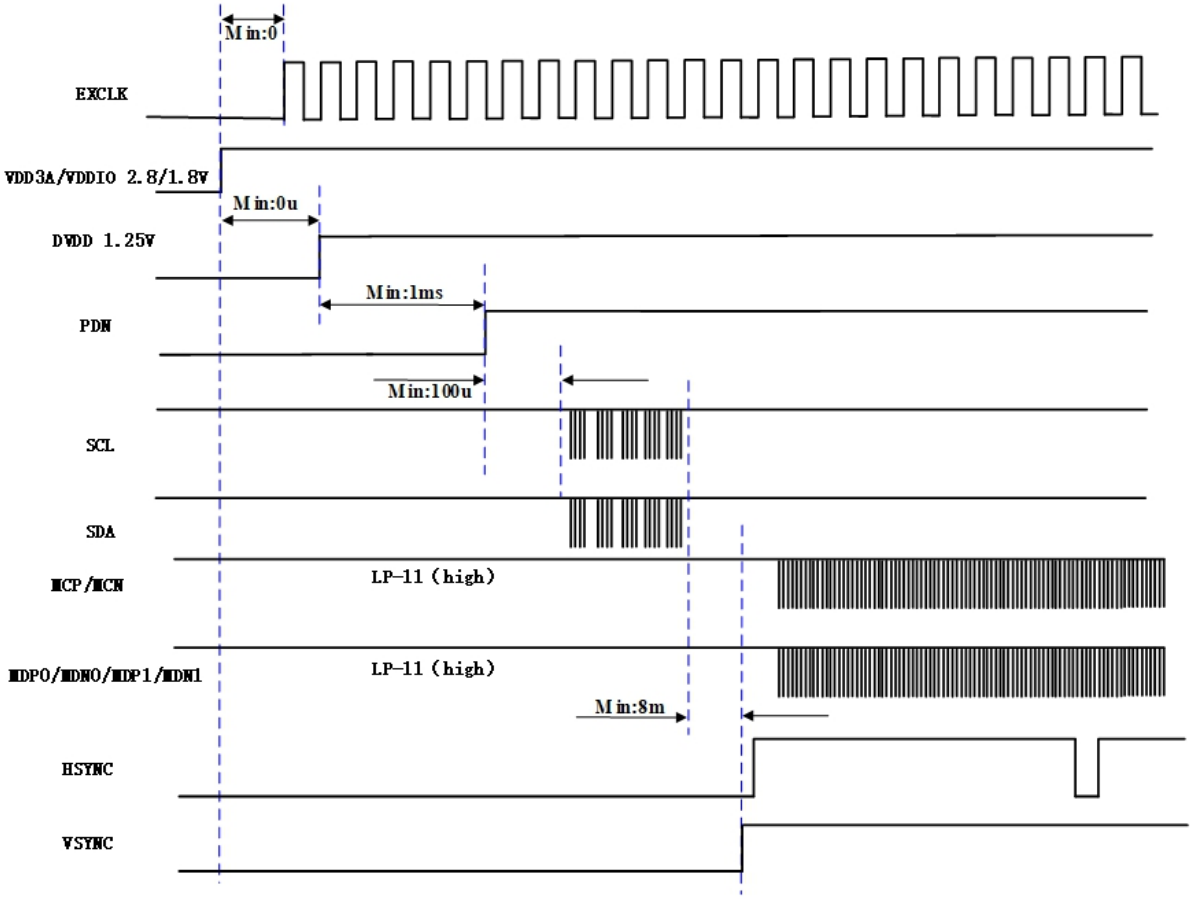


Figure 9- 1 Power-on Sequence

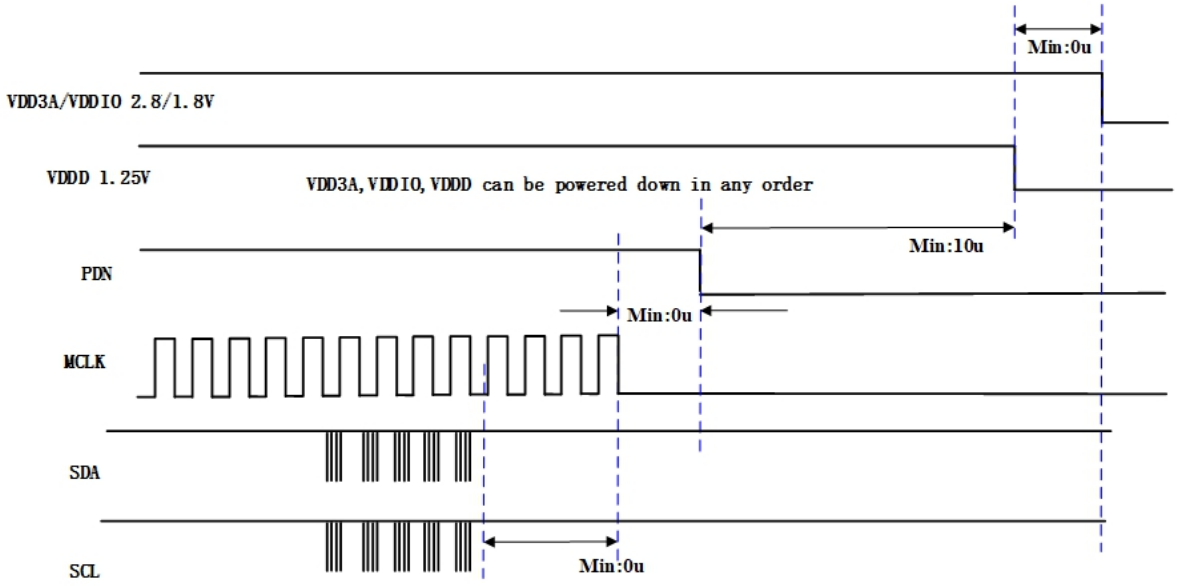


Figure 9- 2 Power-off Sequence

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