1/3.06″ 13Mega CMOS Image Sensor

BF2D31COB

Datasheet

Contents

1 General Description

The BF2D31COB is a 1/3.06 inch 13Mega CMOS Image Sensor which includes CMOS image sensor (CIS) and Sensor control. It is fabricated with the world's most advanced CMOS image sensor process to realize ultra-low dark noise, high sensitivity, high dynamic range and very low power imaging system. The sensor consists of a 4208×3120 pixel array which has an optical format of 1/3.06 inch. It has integrated noise canceling CDS (Correlated Double Sampling) circuits, analog global gain control, auto black level compensation, on-chip 10-bit ADC. It provides Bayer RGB data with serial MIPI interface. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

The product is capable of operating at up to 30 frames per second in 13Mega mode, with complete user control over image. All required sensor control functions, including Exposure control, Gain control, image size and so on, could be programmable through the two-wire serial bus.

2 Features

- 1/3.06 inch optical format
- 1.12um x1.12um BSI Pixel
- 30 frames/sec @13Mega
- 60 frames/sec @1080P
- Ultra-low dark noise at high temperature
- Ultra-Low power consumption
- Output formats: Raw Bayer (10bit)
- Output interface: MIPI 4-lane interface
- Horizontal /Vertical mirror
- Auto black level control
- Black sun cancellation, Window control, Exposure/Gain Control
- OTP support(4K bytes)
- 2 x 2 Binning
- Package: COB

3 Applications

- Cellular Phone Cameras
- Notebook PC cameras and IP cameras
- PDAs
- MP4
- Digital still cameras and camcorders
- Video telephony and conferencing equipment
- Industrial and environmental systems

4 Technical Specifications

- Optical Format 1/3.06 inch
- Active pixel array 4208×3120
- Pixel size 1.12um×1.12um
- Dark current TBD V/s at 25℃
- Power supply 1.7V~3.0V for VDDIO
  2.6V~3.0V for VDD3A/VDD3C
  1.15V~1.25V for VDDD
- Power consumption TBD
- Standby current TBD
- SNR(Max) TBD
- Dynamic range TBD
- Operating temperature -20~70℃
- Stable Image temperature 0~60℃
- Optimal lens chief ray angle 33.98°(Non-linear)
- Package type COB(150μm backgrinding)
- Input clock frequency 6~27MHz

5 Functional Overview

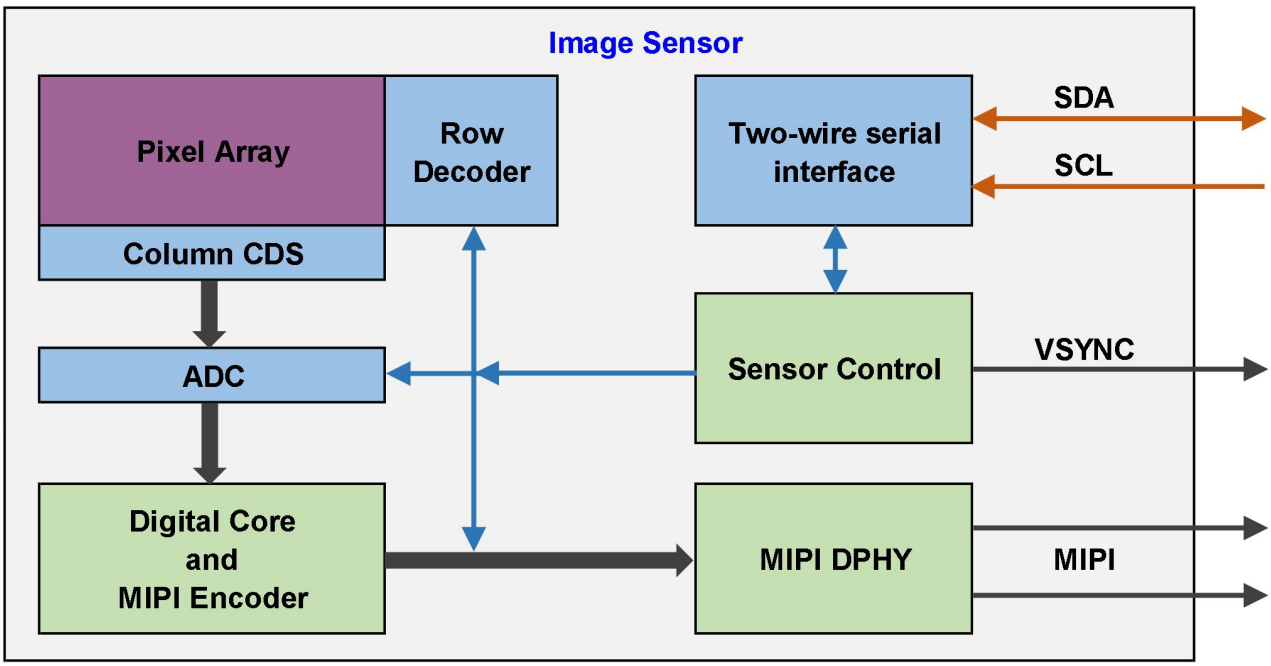


Figure 1 Block Diagram

BF2D31COB has an active image array of 4208x3120 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by A/D converter. It provides global gain to get accurate exposure under different light condition. The digital signals are controlled by Sensor control Block, including Exposure control, Gain control, Test pattern, Image size control and so on.

BF2D31COB has on-chip PLL, it can be used by via two-wire serial interface bus setting.

5.1 Pixel Array

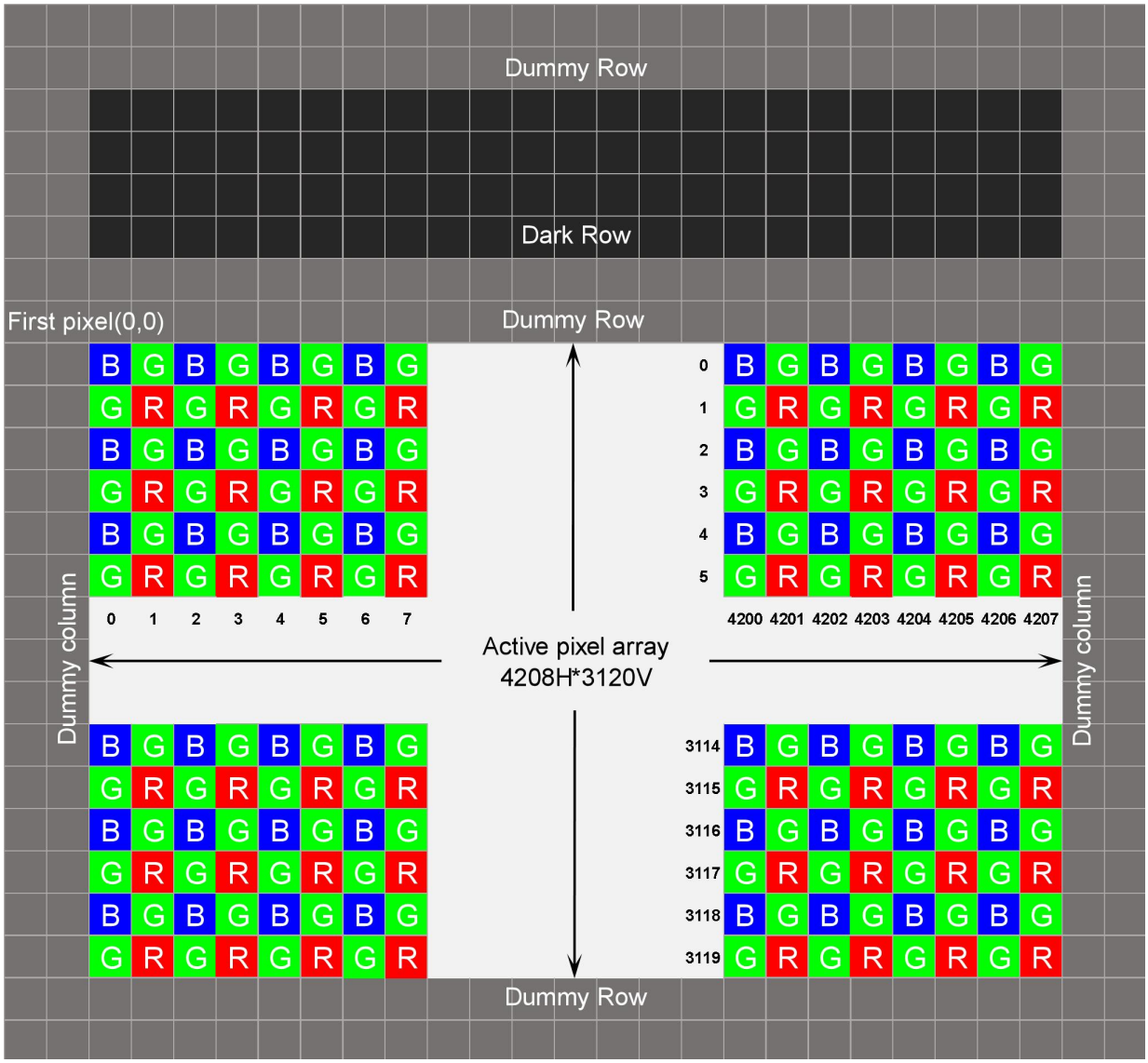


Figure 2 Sensor Array Region

The pixel array includes 4208×3120 effective pixels for imaging, whose address range is from (0, 0) to (4207, 3119). In order to improve the image uniformity, there are extra dummy rows and dummy columns around active array. And dark rows at the top side are for black level control.

Pixel array is covered by Bayer color filters as can be seen in the figure2. The primary color BG/GR array is arranged in line-alternating fashion. Since each pixel can have only one type of color filter on it, only one color component can be obtained by a pixel. BF2D31COB can provide the Raw Bayer data through an 10-bit output data bus. If flip or not in column, the output pixel color order is always the same.

Pixel array output order is always:

BGBGBG……

GRGRGR……

5.2 Lens Chief Ray Angle (CRA)

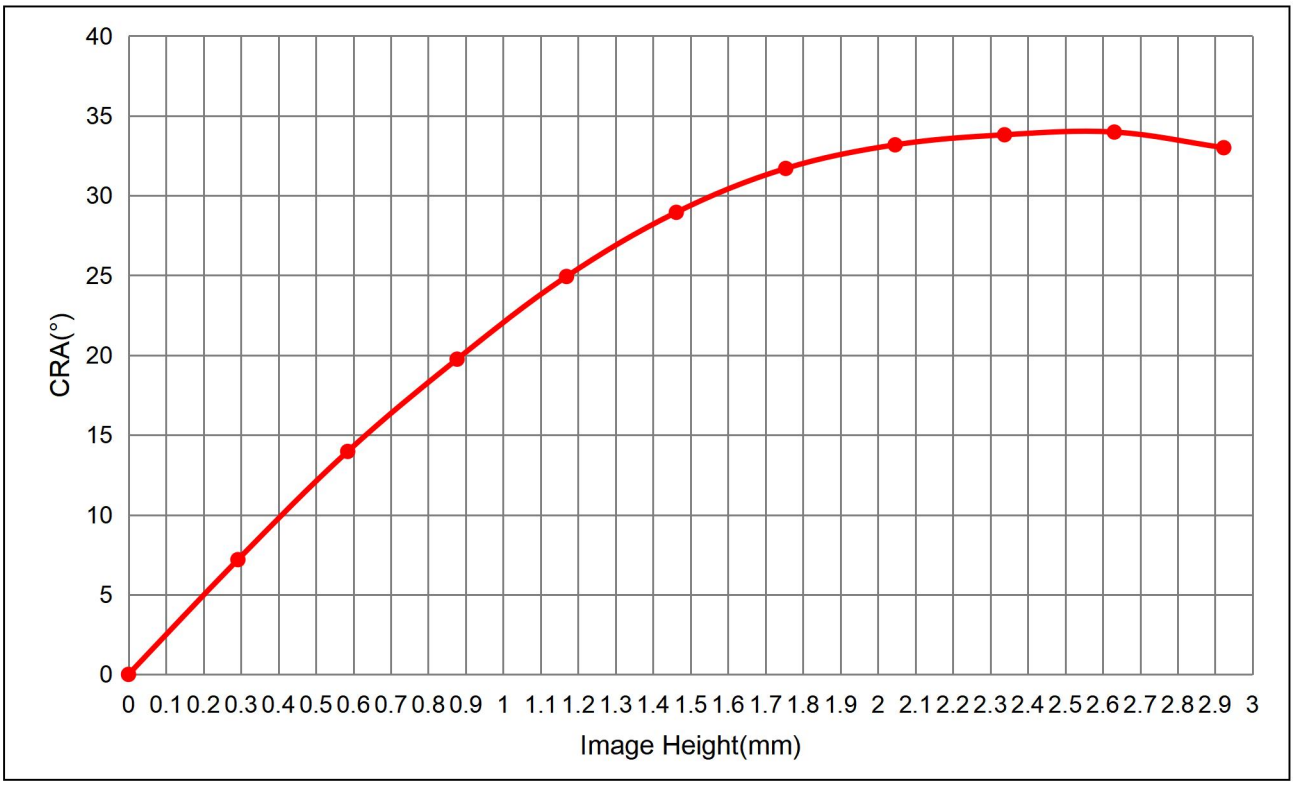


Figure 3 CRA Information

Table 1 CRA versus image height plot

Field(%)	Image Height(mm)	CRA(degree)
0	0	0
0.1	0.292	7.19
0.2	0.585	13.97
0.3	0.877	19.75
0.4	1.169	24.93
0.5	1.462	28.95
0.6	1.754	31.7
0.7	2.046	33.18
0.8	2.338	33.81
0.9	2.631	33.98
1.0	2.923	33

5.3 Column CDS

BF2D31COB has column/row driver circuits to read out the pixel data progressively. The CDS (Correlated Double Sampling) circuit reduces temporal noise and pixel level FPN (Fixed Pattern Noise). The unique patented column buffer and ADC circuit remove column level FPN caused by various sources of manufacturing process variations.

5.4 Sensor control

- Array control and frame generation
- Internal timing signal generation and distribution
- Exposure control, Gain control, Test pattern,
- Image size control
- Frame rate timing
- External timing outputs

5.5 A/D converter

The analog signals are converted to digital forms and data are streamed out column by column. BF2D31COB provides the 10-bit Raw Bayer data through an internal 10-bit data bus.

5.6 Automatic Black Control

The automatic black level control calculates the data of the dark row and controls the lowest black level for output image data.

6 Specifications

6.1 Electrical Characteristics

6.1.1 Absolute Maximum Ratings

- Supply voltage (VDDIO): 1.7 V~3.0 V
- Supply voltage (VDD3A/VDD3C): 2.6V~3.0 V
- Supply voltage (VDDD): 1.15V~1.25V
- Operating temperature: -20~70℃
- Stable Image temperature: 0~60℃
- ESD Rating, Human Body mode: 2000V

Caution: Stresses exceeding the absolute maximum ratings may induce failure.

6.1.2 DC Parameters

Table 2 DC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
VDDIO	I/O power supply	V	1.7	1.8	3.0	1
VDD3A/3C	Analog power supply	V	2.6	2.8	3.0	--
VDDD	Core power supply	V	1.15	1.2	1.25	2
Vih	Input voltage logic “1”	V	0.7*VDDIO	--	--	--
Vil	Input voltage logic “0”	V	--	--	0.2*VDDIO	--
Voh	Output voltage logic “1”	V	0.9*VDDIO	--	--	--
Vol	Output voltage logic “0”	V	--	--	0.1*VDDIO	--
I_vddio	VDDIO supply current, normal operation mode	mA	--	TBD		3
I_vddd	VDDD supply current	mA	--	TBD		3
I_vdd3a_3c	VDD3A supply current	mA	--	TBD		3

Notes：

1. Typical VDDIO is 1.8V for 30 fps.

2. VDDD is the supply for core.
3. The Current of power is decided by the work mode, ex. Frequency of clock and output format. The Max. Current will not appear at the same time.

6.1.3 Clock Requirement

Table 3 AC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
XCLK	External clock frequency	MHz	--	6~27	--	1
PCLK	Pixel clock of the system	MHz	--	120	--	2
SCLK	two-wire serial interface clock frequency	KHz	--	400	--	3

Notes:

1. XCLK is the input clock and it is the input of PLL.
2. PCLK is the master clock of the system, and it can be generated by PLL.
3. SCLK is driven by host processor. For the detail serial bus timing, refer to two-wire serial Interface section.

6.2 Electro-Optical Characteristics

Clock frequency: 120MHz

Operating voltage: VDDIO=1.8V, VDDD=1.2V, VDD3A/VDD3C=2.8V

Operating temperature: 25°C

Table 4 Electro-Optical Characteristics

Parameter	Unit	Min.	Typ.	Max.	Notes
Dark current	mV/sec	--	TBD	--	1
S/N ratio	dB	--	TBD	--	--
Dynamic Range	dB	--	TBD	--	--
Frame Rate	fps	--	TBD	30	2

Notes:

1. Measured at dark condition for exposure time of 1s (25 Celsius).
2. 4208×3120 size at PCLK 120MHz.

6.3 MIPI output Timing

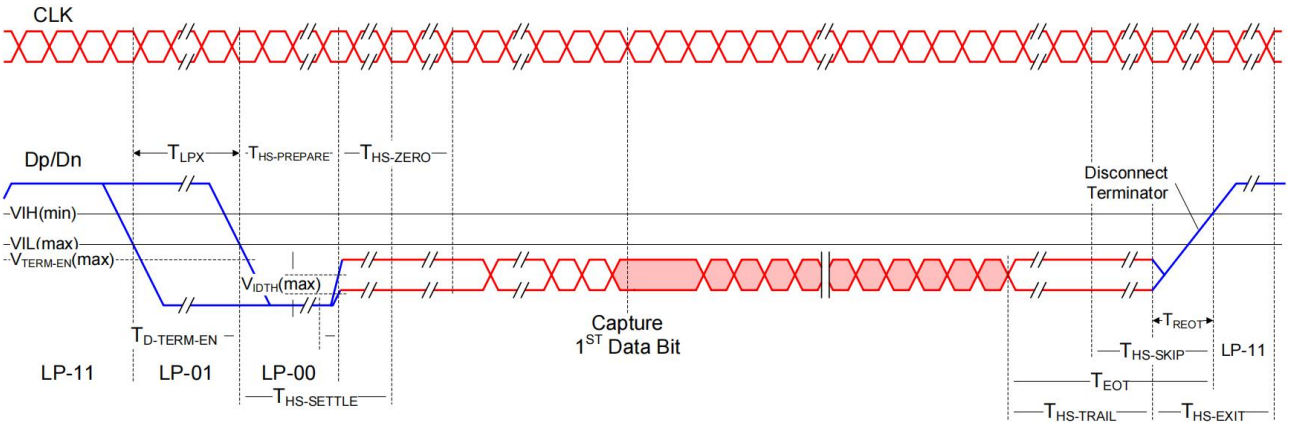


Figure 4 High-Speed Data Transmission in Bursts

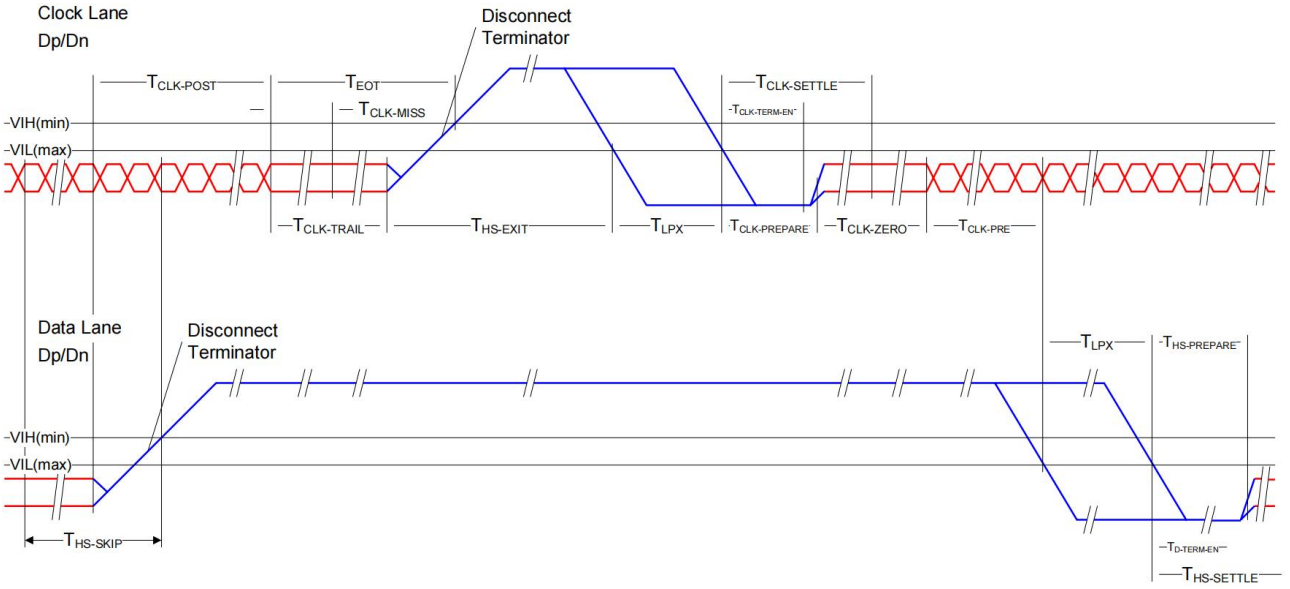


Figure 5 Switching the Clock Lane between Clock Transmission and Low-Power Mode

6.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below.

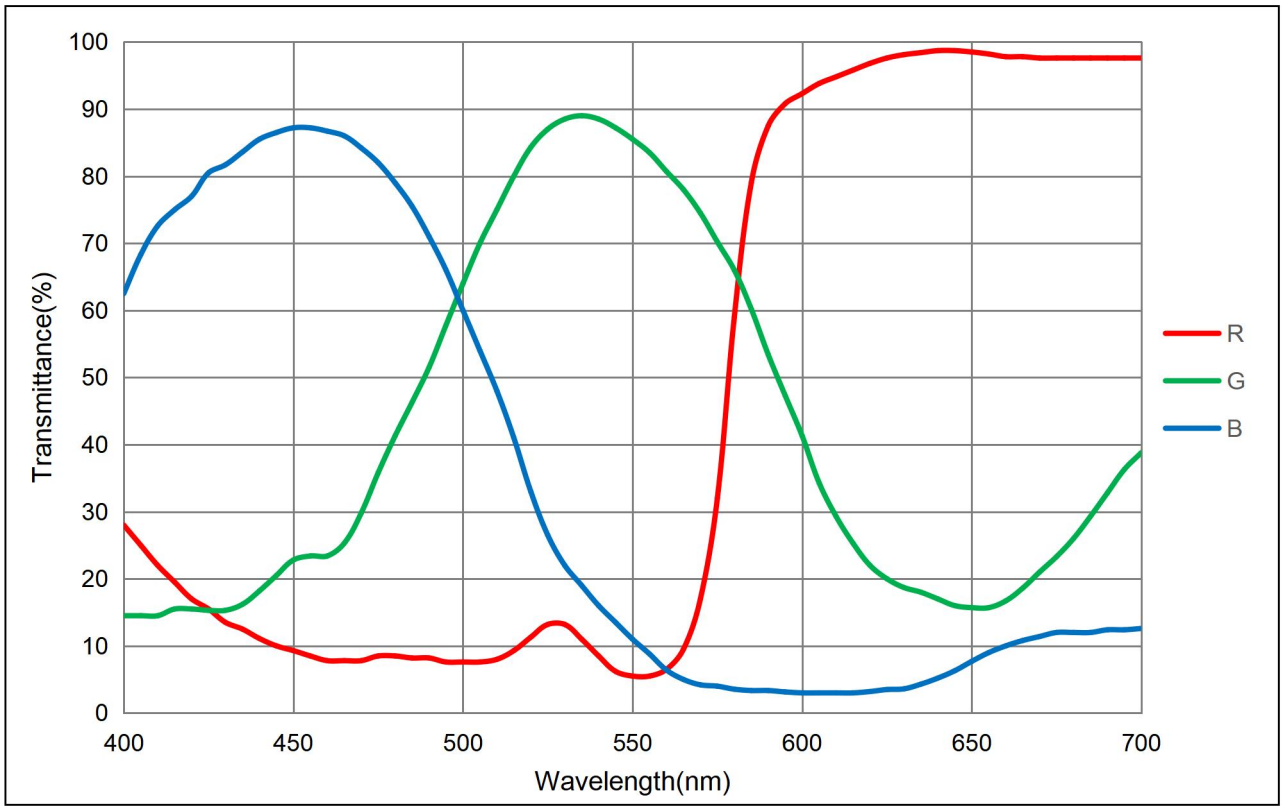


Figure 6 Spectral Characteristics

7 Two-wire serial interface& Register

7.1 Theory of Operation

The registers of BF2D31COB are written and read through the two-wire serial interface. BF2D31COB has two-wire serial interface slave. BF2D31COB is controlled by the two-wire serial interface clock (SCLK), which is driven by the two-wire serial interface master. Data is transferred into and out of BF2D31COB through the two-wire serial interface data (SDA) line. The SCL and SDA lines are pulled up to VDDIO by a 2kΩ off-chip resistor. Either the slave or the master device can pull the lines down. The two-wire serial interface protocol determines which device is allowed to pull the two lines down at any given time.

Note: Two-wire serial interface device address of BF2D31COB is7'b0111110 (ID_SEL=Low, 0x3e)/7'b1101110 (ID_SEL=High, 0x6e), it doesn't include W/R bit.

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A0 in the LSB of the address indicates write mode, and A1 indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The two-wire serial interface clock pulse is provided by the

master. The data must be stable during the HIGH period of the two-wire serial interface clock: it can only change when the two-wire serial interface clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a write and a 1 indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The BF2D31COB uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

7.2 Two-wire Serial Interface Functional Description

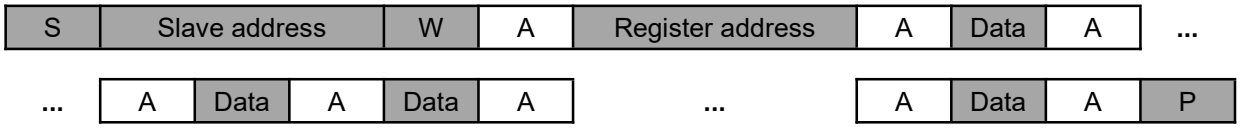
BF2D31COB Device Address:

Table 5 Device Address

ID_SEL	Slave address write mode	Slave address read mode
0(default)	0x7c	0x7d
1	0xdc	0xdd

Single Write Mode Operation

Multiple Write Mode (Register address is increased automatically) [1] Operation



Single Read Mode Operation

Multiple Read Mode (Register address is increased automatically) [1] Operation

S	Slave address	W	A	Register address	A	...
Sr	Slave address	R	A	Data	A	Data	A	...
...	A	Data	A	Data	NA	P

From master to slave

From slave to master

S: Start condition.

Sr: Repeated Start (Start without preceding stop.)

A: Acknowledge bit.

NA: No Acknowledge.

Data: 8-bit data

P: Stop condition

R/W: Read/Write selection. High = read, LOW = write.

Note1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

7.3 The Two-wire Serial Interface Timing

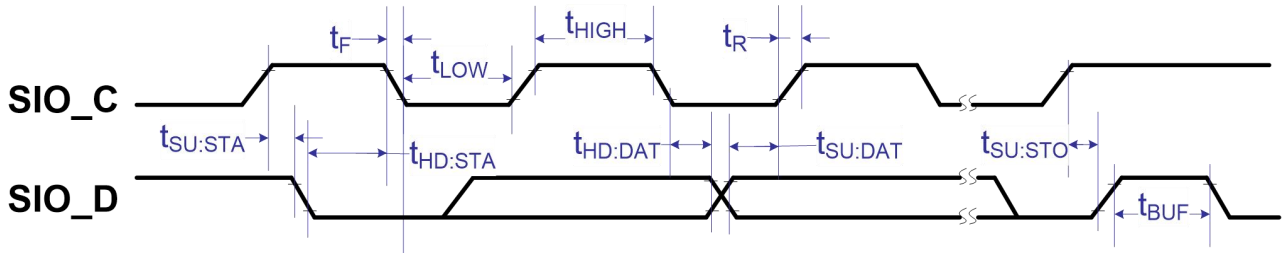


Figure 7 Two-Wire Serial Interface Timing

Table 6 AC Characteristics

Symbol	Descriptions	Min.	Typ.	Max.	Unit
t_R, t_F	two-wire serial interface rise/fall times	--	--	300	ns
t_{LOW}	Clock Low Period	1.3	--	--	us
t_{HIGH}	Clock High Period	600	--	--	ns
$t_{HD:STA}$	Start condition Hold Time	600	--	--	ns
$t_{SU:STA}$	Start condition Setup Time	600	--	--	ns
$t_{HD:DAT}$	Data-in Hold Time	0	--	--	ns
$t_{SU:DAT}$	Data-in Setup Time	100	--	--	ns
$t_{SU:STO}$	Stop condition Setup Time	600	--	--	ns

8 Register Summary

Table 7 BF2D31COB Registers Lists

Address	Name	Width	Default value	Description
01h	SC_CNTL1	8	42h	Bit[7]:Soft Power Down sync enable. Bit[6]:VBLANK update sel. Bit[5]:GLB_GAIN_IN delay sel. Bit[4]:Reserved. Bit[3]:Pixel array reset sel. Bit[2:0]:HREF delay sel.
02h	SC_CNTL2	8	8ch	Reserved
03h	SC_CNTL3	8	40h	Bit[7:6]:Reserved Bit[5]: FSYNC IO enable, Bit[4]: Master sync enable. Bit[3]: FSIN signal mode control. Bit[2]: Reserved. Bit[1]: Dynamic sync mode sel; Bit[0]: Dual sync delay sel;
04h	SC_CNTL4	8	00h	Dual sync offset
05h	DSYNC_OFFSET [7:0]	8	00h	Sync offset;
06h	VBLANK_PIX	8	0ah	Dummy line low 8 Bits
07h	VBLANK_PIX[15:8]	8	00h	Dummy line high 8 Bits
08h	HSYST_LOCK	8	10h	HSYNC rising edge low 8 Bits
09h	HSYEN_LOCK	8	80h	HSYNC falling edge low 8 Bits
0ah	H_HSYNC_EDGE_LOCK	8	06h	Bit[7:4]: HSYNC rising edge[11:8]; Bit[3:0]: HSYNC falling edge[11:8];
0bh	LINE_LREG_LOCK	8	1ch	Bit[7:0]: LINE_LENGTH[7:0].
2ch	FRAME_LENGTH_OUT	8	bch	Bit[7:0]: FRAME_LENGTH_DEFAULT[7:0].
2dh	FRAME_LENGTH_OUT[15:8]	8	09h	Bit[7:0]: FRAME_LENGTH_DEFAULT[15:8].
30h	MIPI_STEN	8	08h	Control VSYNC_MIPI falling edge.
31h	LINE_HREG_LOCK	8	07h	Bit[7:4]: Reserved. Bit[3:0]: LINE_LENGTH[11:8].
4fh	SH_Timing	8	02h	Control the falling edge of SET_RAMP
50h	FRAME_AVER_TH	8	20h	Used as black level update threshold when multi frame is enable.

51h	MODE_CNTL1	8	13h	Bit[7]: SINGLE_PATH_EN; Bit[6:5]: SINGLE_PATH_SEL; Bit[4]: LAST_EN; Bit[1:0]: MFRAME Sel ;
52h	AVER_LOCK_SUB BIN_MODE_CNTL	8	06h	Bit[7:6]: AVER_LOCK_SUB Bit[2:0]: BIN_MODE_CNTL
53h	DARKE0_AVER[9:8] DARKO0_AVER[9:8] DARKE1_AVER[9:8] DARKO1_AVER[9:8]	8	RO	Bit[7:6]: Current frame black level for E row E col; Bit[5:4]: Current frame black level for E row O col; Bit[3:2]: Current frame black level for O row E col; Bit[1:0]: Current frame black level for O row O col;
54h	DARKE0_AVER	8	RO	Current frame black level for E row E col;
55h	DARKO0_AVER	8	RO	Current frame black level for E row O col;
56h	DARKE1_AVER	8	RO	Current frame black level for O row E col;
57h	DARKO1_AVER	8	RO	Current frame black level for O row O col;
58h	AVER_TAR_E0	8	00h	Black level target for E row E col;
59h	AVER_TAR_O0	8	00h	Black level target for E row O col;
5ah	AVER_TAR_E1	8	00h	Black level target for O row E col;
5bh	AVER_TAR_O1	8	00h	Black level target for O row O col;
5ch	AVER_LOCK	8	21h	Bit[7:4]: Lock value to update sel1; Bit[3:0]: Lock value to update sel2;
5dh	MODE_CNTL	8	23h	Bit[7]: BYPASS_BC. Bit[6:4]: DARKROW_SEL. Bit[3]: DGAD_MODE. Bit[2]: PATH_CHANGE. Bit[1]: MODE_CTL. Bit[0]: DIG_MODE_CTL.
5eh	AVER_E0	8	RO	Read out black aver for E row E col,this value has been adjusted.
5fh	AVER_O0	8	RO	Read out black aver for E row O col,this value has been adjusted.
60h	AVER_E1	8	RO	Read out black aver for O row E col,this value has been adjusted.
61h	AVER_O1	8	RO	Read out black aver for O row O col,this value has been adjusted.
62h	AVER_TAR_E0[9:8] AVER_TAR_O0[9:8] AVER_TAR_E1[9:8] AVER_TAR_O1[9:8]	8	00h	Bit[7:6] : Black level target for even col and even row. Bit[5:4] : Black level target for odd col and even row. Bit[3:2] : Black level target for even col and odd row. Bit[1:0] : Black level target for odd col and odd row.
64h	Y_AVER	8	RO	The Y_aver of the current frame
65h	UPDATE_EN	2	80h	Bit[7]: Global Switch. 1'b0:on 1'b1:off. Bit[6:1]: Reserved Bit[0]: Group Switch. 1'b0:off 1'b1:on.
66h	R_GAIN	8	80h	Red Gain.

67h	B_GAIN	8	80h	Blue Gain.
68h	G0_GAIN	8	80h	Green0(GB) Gain
69h	G1_GAIN	8	80h	Green1(GR) Gain.
6ah	GLB_GAIN_I2C	8	0fh	Global Gain.
6bh	INT_TIME_H	8	02h	Real integration time MSB.
6ch	INT_TIME_L	8	0fh	Real integration time LSB.
6dh	GLB_GAIN_MIN	8	0fh	The limit of the global gain.
6eh	COLORGAIN_LSB	8	00h	Color Gain LSB.
6fh	DIG_GAIN_I2C_M	3	00h	DIG_GAIN MSB
70h	DIG_GAIN_I2C_L	8	40h	DIG_GAIN LSB
7bh	DGCTRL	2	0h	Bit[1]: Bypass module. Bit[0]: OFFSET Sel.
7ch	OFFSET_ME	8	00h	Bit[7:0]: The manual written digital gain offset.
7dh	OFFSET_MO	8	00h	Bit[7:0]: The manual written digital gain offset.
7eh	COMP_GAIN	6	00h	Bit[7:6]: Reserved. Bit[5:0]: COMP_GAIN,LSB control.
80h	D_LPX	8	08h	Bit[7:0]: The length of LPX
81h	HS_PREPARE	8	05h	Bit[7:0]: The length of HS_PREPARE
82h	HS_ZERO	8	10h	Bit[7:0]: The length of HS_ZERO
83h	HS_TRAIL	8	07h	Bit[7:0]: The length of HS_TRAIL
84h	Clk_LPX	8	08h	Bit[7:0]: The length of Clk_LPX
85h	Clk_PREPARE	8	06h	Bit[7:0]: The length of Clk_PREPARE
86h	Clk_ZERO	8	1eh	Bit[7:0]: The length of Clk_ZERO
87h	Clk_PRE	8	01h	Bit[7:0]: The length of Clk_PRE
88h	Clk_POST	8	0ch	Bit[7:0]: The length of Clk_POST
89h	Clk_TRAIL	8	07h	Bit[7:0]: The length of Clk_TRAIL
8ah	MIPI_CNTL0	8	2bh	Bit[7:6]: VC,Virtual Channel Identifier. Bit[5:0]: Image_type.
8bh	Frame_num_max_H	8	00h	High Byte of Max Frame_Counter of Frame Sync Short Packet
8ch	Frame_num_max_L	8	00h	Low Byte of Max Frame_Counter of Frame Sync Short Packet
8dh	MIPI_CNTL1	8	1fh	Bit[7:5]: Control the ECC Generation. Bit[4]: 1'b1:MIPI enable ; 1'b0:MIPI disable. Bit[3]: DAT_Lane_en23=1, DAT_LP={2{DAT_Lane23_DIS_LP}}; Bit[2]: DAT_Lane_en01=1, DAT_LP={2{DAT_Lane01_DIS_LP}}; Bit[1]: 1'b1: Clock lane enable; 1'b0: Data lane disable. Bit[0]: 1'b0: Continuous clock mode; 1'b1: Non-continuous clock mode.

8eh	MIPI_CNTL2	8	90h	Bit[7]: 0: 2-Lane system; 1: 4-Lane system. Bit[6]: Fix data output 1'b1: The fix data is FIX_data; 1'b0: Normal data output. Bit[5]:1'b0:When MIPI disable and PW_ST_CNTL==0, LP is 11; 1'b1:When MIPI disable and PW_ST_CNTL==0, LP is 00. Bit[4]: Raw10 enable. Bit[3]:1'b1: LS and LE will be output; 1'b0: LS and LE didn't be output. Bit[2]:1'b0: WC in LS and LE is always 0; 1'b1: WC in LS and LE isn't 0; Bit[1]:1'b0: WC in FS and FE is always 0; 1'b1: WC in FS and FE isn't 0 . Bit[0]:1'b0: VSYNC_IMAGE is be packed; 1'b1: VSYNC_DAT is be packed.
8fh	MIPI_CNTL3	8	05h	Bit[7]: 1'b1: The state of the DP and DN is HS. 1'b0: The state of the DP and DN is LP. Bit[6]: 1'b1: Enable clock lane ULPS state; 1'b0: Disable clock lane ULPS state; Bit[5]: 1'b1: Enable data lane 23 ULPS state; 1'b0: Disable data lane 23 ULPS state; Bit[4]: 1'b1: Enable data lane 01 ULPS state; 1'b0: Disable data lane 01 ULPS state; Bit[3:0]: The mode enter into ULPS mode at this time.
90h	MIPI_CNTL4	8	30h	Bit[7:6]: FIX_DATA[9:8]; Bit[5:4]: When CLK_Lane_en=1, LK_LP=CLK_Lane_DIS_LP; Bit[3:2]: Reserved. Bit[1:0]: Reserved.
91h	FIX_data_L	8	00h	Bit[7:0]: FIX_DATA[7:0];
92h	MIPI_CNTL5	8	f1h	Bit[7]: 1'b1: Data lane 3 enable; 1'b0: Data lane disable. Bit[6]: 1'b1: Data lane 2 enable; 1'b0: Data lane disable. Bit[5]: 1'b1: Data lane 1 enable; 1'b0: Data lane disable. Bit[4]: 1'b1: Data lane 0 enable; 1'b0: Data lane disable. Bit[3]: EO_MODE; Bit[2]: PWDN_LP_EN; Bit[1]: SRAM_A_ON; Bit[0]: 1'b0:MASK_1ST_EN ;
93h	MIPI_CNTL6	8	00h	Bit[7:4]: SRAM_TEST Bit[3]: Reserved; Bit[2]: PW_ST_CNTL; Bit[1:0]: ECC[7:6].

94h	TEST_MODE	8	00h	Bit[7:0]: 8'h00: Normal output; 8'hxx: Test_pattern output; Bit[7]: 1'b0: Overlay output; 1'b1: Test_mode output; Bit[6:5]: 2'h00: output bar pattern; 2'h01: output gradual pattern; 2'h10: output manual pattern; 2'h11: output auto scan mode(speed is controlled by Bit[4:0]); Bit[4]: 1'b0:Vertical pattern; 1'b1: Horizontal pattern; Bit[3:0]: Gradual gray pattern mode control.
95h	MAN_R	8	80h	Manual R value.
96h	MAN_G	8	80h	Manual G value.
97h	MAN_B	8	80h	Manual B value.
98h	BP_COM	8	80h	Bit[7]: BP_ENABLE, 1'b0: BP disable 1'b1: BP enable Bit[6:5]: Reserved; Bit[4]: DAT_EXCH 1'b0: Do not exchange EO data 1'b1: EO data exchange Bit[3:0]: Reserved;
99h	EFUSE_ADDRH	4	00h	OTP high address
9ah	EFUSE_ADDRL	8	00h	OTP low address
9bh	EFUSE_DIN	8	00h	OTP Write Data
9ch	EFUSE_RD_CTR, EFUSE_WE_CTR	2	0h	Bit[7]: OTP Read enable; Bit[6]: OTP Write enable; Bit[5:0]: Reserved.
9dh	EFUSE_DOUT_S	8	RO	OTP Read Data
9eh	TSPPGAVDDD	8	10h	Bit[7:6]: Test Command 2'b00: Normal; 2'b01: Blank Check; 2'b10: TESTDEC; 2'b11: WRTEST; Bit[5:4]: Reserved Bit[3]: Program fall flag Bit[2]: Blank check test flag Bit[1]: TESTDEC main array test flag Bit[0]: TESTDEC redundant array test flag
9fh	ADD_MODE SRAM_TEST_OKD OTP_AVTIVE CEB_SRAM_SEL NP	8	15h	Bit[7]: OTP Continuous Write/Read enable Bit[6]: 1,b0:SRAM Write/Read test fail 1,b1:SRAM Write/Read test pass Bit[5]: OTP busy sign Bit[4]: CEB pin mode Bit[3:0]: Maximum number of additional programming pulses

a0h	BINNING_SEL	8	06h	Bit[7:3]: Reserved; Bit[2]: Binning mode sel: 1'b0: Average mode; 1'b1: Summation mode; Bit[1]: Binning mode sel: 1'b0: Average mode; 1'b1: Summation mode; Bit[0]: Binning mode sel: 1'b0: Tri pixel mode; 1'b1: Dual pixel mode;
ach	SC_CNTLMD	8	41h	Bit[7:6]: Reserved. Bit[5]: Binning mode enable. Bit[4]: Binning mode sel. Bit[3:0]: Reserved.
c0h	AVER_E0[9:8] AVER_O0[9:8] AVER_E1[9:8] AVER_O1[9:8]	8	RO	Bit[7:6]: Read out black level for even col and even row. Bit[5:4]: Read out black level for odd col and even row. Bit[3:2]: Read out black level for even col and odd row. Bit[1:0]: Read out black level for odd col and odd row.
c1h	AVER_E0[10] AVER_O0[10] AVER_E1[10] AVER_O1[10]	4	RO	Bit[7]: Read out black level for even col and even row. Bit[6]: Read out black level for odd col and even row. Bit[5]: Read out black level for even col and odd row. Bit[4]: Read out black level for odd col and odd row.
c2h	COEF	8	80h	Black aver adjust coefficient.
c9h	COM0	8	00h	Bit[7]: Output Bypass Bit[6:4]: Test sel. Bit[3:2]: Output sel. Bit[1]: Reserved. Bit[0]: HREF mode.
cah	HWIN	8	c0h	Bit[7:4]: High 4 bits of HSTOP Bit[3:0]: High 4 bits of HSTART
cbh	VWIN	8	90h	Bit[7:4]: High 4 bits of VSTOP Bit[3:0]: High 4 bits of VSTART
cch	HSTART	8	00h	Window Horizontal start low 8-bits (High 4 bits are at HWIN[3:0])
cdh	HSTOP	8	c0h	Window Horizontal stop low 8-bits (High 4 bits are at HWIN[7:4])
ceh	VSTART	8	00h	Window vertical start low 8-bits (High 4 bits are at VWIN[3:0])
cfh	VSTOP	8	90h	Window vertical stop low 8-bits (High 4 bits are at VWIN[74])
d0h	SKIP_CTR	8	00h	Bit[7]: DARK_SEL,Dark row selection. Bit[6]: The LSB selection. 1'b0: 1/8 module; 1'b1: 1/4 module; Bit[4:0]: Skip frame counter; If SKIP_CTR=0, don't skip frame; Else skip as many as SKIP_CTR frames;

ddh	REG_SEL1	8	24h	Bit[7:6]: Binning Ctrl. Bit[5:3]: Reserved. Bit[2:0]: Voltage of LVDS. 3'b000:488.8mV. 3'b001:469.6mV. 3'b010:449.2mV. 3'b011:427.8mV. 3'b100:405.0mV (default) 3'b101:380.9mV. 3'b110:355.3mV. 3'b111:328.1mV.
deh	REG_SEL2	8	00h	Adjust the phase of MDP and MDN
dfh	REG_SEL3	8	55h	Adjust the Rout of MDP and MDN.
e0h	REG_SEL4	8	01h	Bit[7:1]: Reserved. Bit[0]: LP OEN. 1'b0: Hiz. 1'b1: Enable.
e1h	REG_SEL5	8	8bh	Bit[7:4]: VPCP Sel. Bit[3:0]: VNCP Sel.
e2h	REG_SEL6	8	92h	DAC Sel.
e5h	REG_COM0	8	98h	Bit[7]: PLL1 Loop DIV[8](1'b1 default). Bit[6]: CLK_PLL1 Bypass. Bit[5:4]: Sel for PLL1 VCO. Bit[3:0]: Sel for PLL1 Pre-DIV[3:0]
e6h	REG_COM1	8	c5h	Bit[7:0]: PLL1 Loop DIV[7:0].
e9h	REG_COM4	8	4bh	Bit[7:0]: PLL2 Loop DIV[7:0].
ech	REG_COM7	8	08h	CLK Sel.
edh	REG_COM8	8	02h	CLK Sel.
eeh	REG_COM9	8	01h	Bit[7]: Reserved. Bit[6:5]: Sel for I2C SDA drive. Bit[4:3]: Sel for FSYNC drive. Bit[2]: DR0. Bit[1]: FSYNC input enable. Bit[0]: FSYNC output enable.
efh	REG_OTP	8	3dh	Bit[7:5]: CP_TRIM[2:0]. 3'b001, default. Bit[4]: {REG_OTP[4],REG_PLL[5]} for RDAPVFY_TRIM[1:0] 2'b10: Default. Bit[3:0]: IPGM_TRIM[3:0] 4'b1101: Default.
f0h	REGF0	2	0h	Bit[1]:READ_C_EN,read in serial mode. 1'b0: Off(OTP compatible) 1'b1: On Bit[0]:SCCB_RESET 1'b0: No change 1'b1: Resets all registers to default values.
f1h	REGF1	1	1h	SOFT_PD_REG.
f2h	V/H FLIP	2	0h	Vertical Flip/ Mirror Control: Bit[1]: Mirror, 0: Normal image, 1: Mirror image; Bit[0]: Vertical Flip, 0: Normal image, 1: Vertically flip image;
fbh	VER_BME	3	RO	Version of product

fch	PIDH_BME	8	RO	MSB for product ID
fdh	PIDL_BME	8	RO	LSB for product ID

9 Pad Configuration

9.1 Pad Diagram

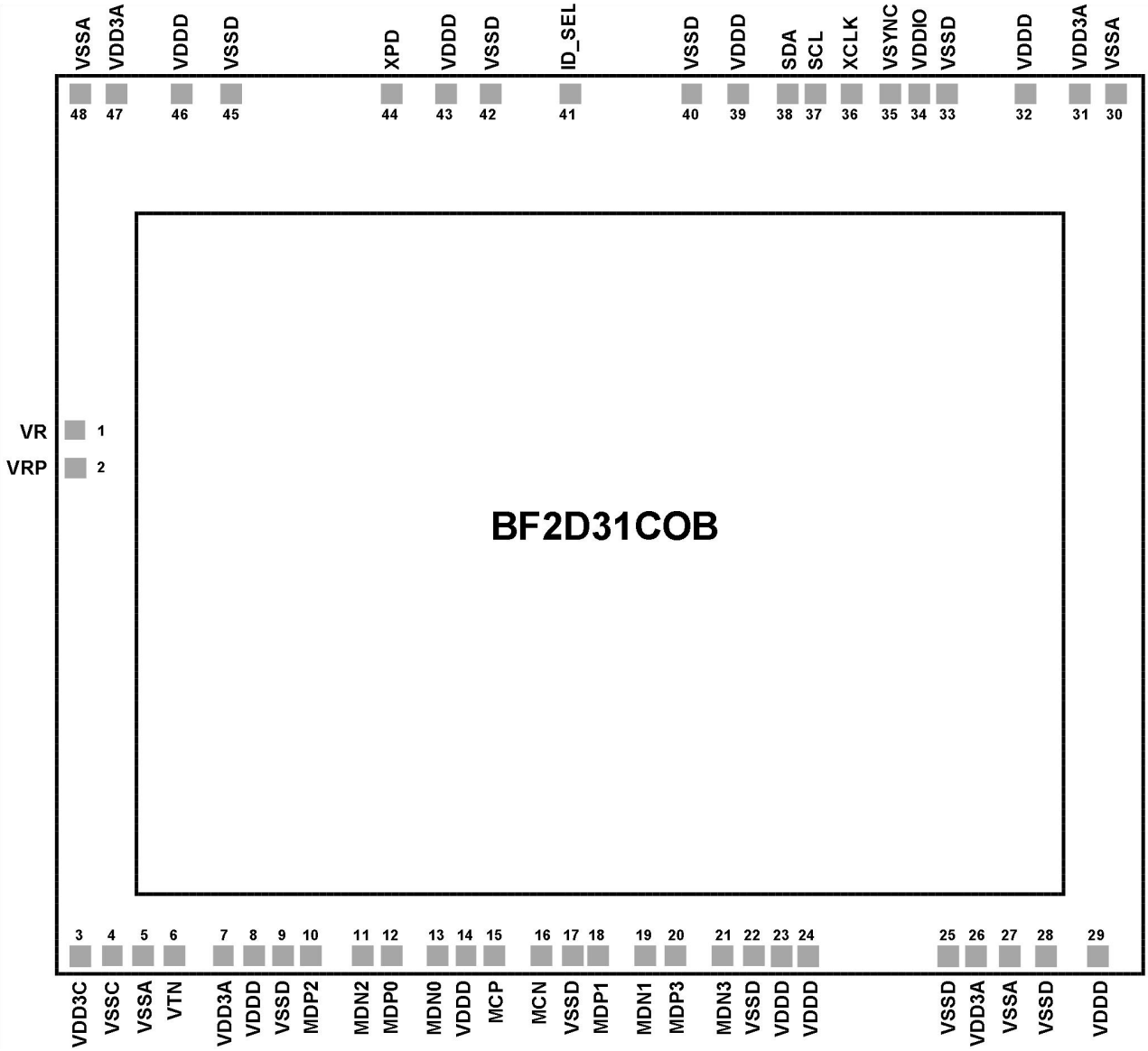


Figure 8 Pad Diagram

9.2 Pad Description

Table 8 Pad Description

Pad Number	X(μm)	Y(μm)	Name	Pin Type	Function/Description
1	-2689.0	484.3	VR	I/O	Inner analog voltage

2	-2689.0	277.9	VRP	I/O	Inner analog voltage
3	-2657.0	-2213.0	VDD3C	Supply	Analog power supply: 2.6V~3.1V
4	-2482.6	-2213.0	VSSC	Ground	Analog ground
5	-2342.6	-2213.0	VSSA	Ground	Analog ground
6	-2182.6	-2213.0	VTN	I/O	Inner analog voltage
7	-1924.5	-2213.0	VDD3A	Supply	Analog power supply: 2.6V~3.1V
8	-1753.6	-2213.0	VDDD	Supply	Digital core power supply: 1.15V~1.25V
9	-1613.6	-2213.0	VSSD	Ground	Digital ground
10	-1473.6	-2213.0	MDP2	I/O	Pos Data lane2 of MIPI
11	-1229.1	-2213.0	MDN2	I/O	Neg Data lane2 of MIPI
12	-1068.1	-2213.0	MDP0	I/O	Pos Data lane0 of MIPI
13	-823.5	-2213.0	MDN0	I/O	Neg Data lane0 of MIPI
14	-683.5	-2213.0	VDDD	Supply	Digital core power supply: 1.15V~1.25V
15	-543.5	-2213.0	MCP	I/O	Pos Clock lane of MIPI
16	-299.0	-2213.0	MCN	I/O	Neg Clock lane of MIPI
17	-159.0	-2213.0	VSSD	Ground	Digital ground
18	-19.0	-2213.0	MDP1	I/O	Pos Data lane1 of MIPI
19	225.5	-2213.0	MDN1	I/O	Neg Data lane1 of MIPI
20	385.5	-2213.0	MDP3	I/O	Pos Data lane3 of MIPI
21	630.1	-2213.0	MDN3	I/O	Neg Data lane3 of MIPI
22	770.1	-2213.0	VSSD	Ground	Digital ground
23	910.1	-2213.0	VDDD	Supply	Digital core power supply: 1.15V~1.25V
24	1050.1	-2213.0	VDDD	Supply	Digital core power supply: 1.15V~1.25V
25	1751.9	-2213.0	VSSD	Ground	Digital ground
26	1913.8	-2213.0	VDD3A	Supply	Analog power supply: 2.6V~3.1V
27	2093.9	-2213.0	VSSA	Ground	Analog ground
28	2264.8	-2213.0	VSSD	Ground	Digital ground
29	2525.4	-2213.0	VDDD	Supply	Digital core power supply: 1.15V~1.25V
30	2625.4	2213.0	VSSA	Ground	Analog ground
31	2445.3	2213.0	VDD3A	Supply	Analog power supply: 2.6V~3.1V
32	2161.1	2213.0	VDDD	Supply	Digital core power supply: 1.15V~1.25V
33	1766.6	2213.0	VSSD	Ground	Digital ground
34	1616.6	2213.0	VDDIO	Supply	I/O power supply: 1.7V~3.1V
35	1466.6	2213.0	VSYNC	I/O	Frame Sync
36	1267.6	2213.0	XCLK	Input	System input clock
37	1090.6	2213.0	SCL	Input	SCCB serial interface clock input
38	950.6	2213.0	SDA	I/O	SCCB serial interface data inout
39	706.1	2213.0	VDDD	Supply	Digital core power supply: 1.15V~1.25V

40	458.3	2213.0	VSSD	Ground	Digital ground
41	-159.0	2213.0	ID_SEL	Input	I2C Address Selection. 0: 0x7c/0x7d; 1: 0xdc/0xdd.
42	-543.5	2213.0	VSSD	Ground	Digital ground
43	-791.4	2213.0	VDDD	Supply	Digital core power supply: 1.15V~1.25V
44	-1068.1	2213.0	XPD	Input	Power Down Mode Selection. 0: Power down mode; 1: Normal mode.
45	-1874.3	2213.0	VSSD	Ground	Digital ground
46	-2123.2	2213.0	VDDD	Supply	Digital core power supply: 1.15V~1.25V
47	-2454.6	2213.0	VDD3A	Supply	Analog power supply: 2.6V~3.1V
48	-2647.1	2213.0	VSSA	Ground	Analog ground

9.3 Chip Center and Optical Center

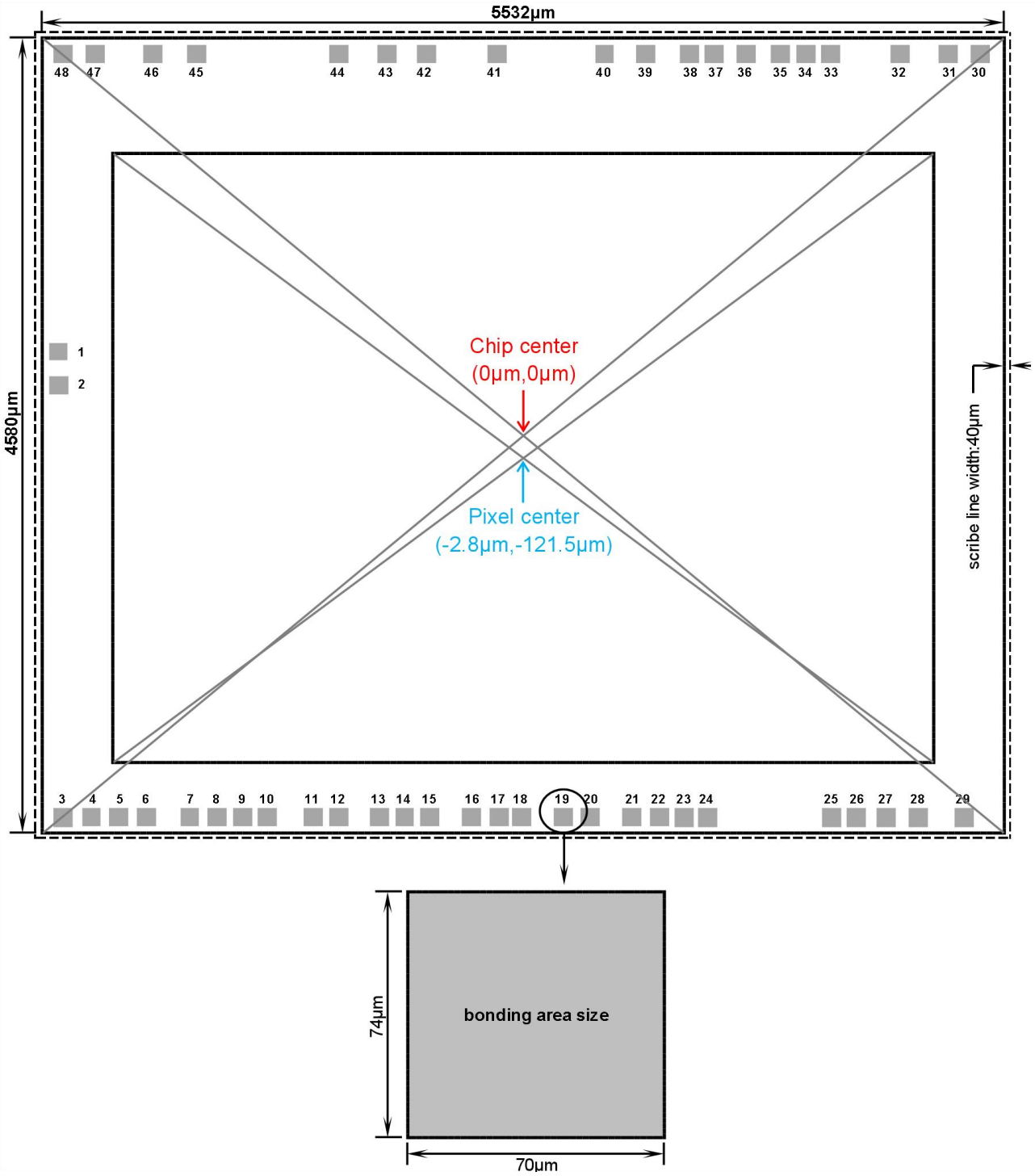


Figure 9 Chip Center and Optical Center(unit:μm)

10 Reference Design Schematic

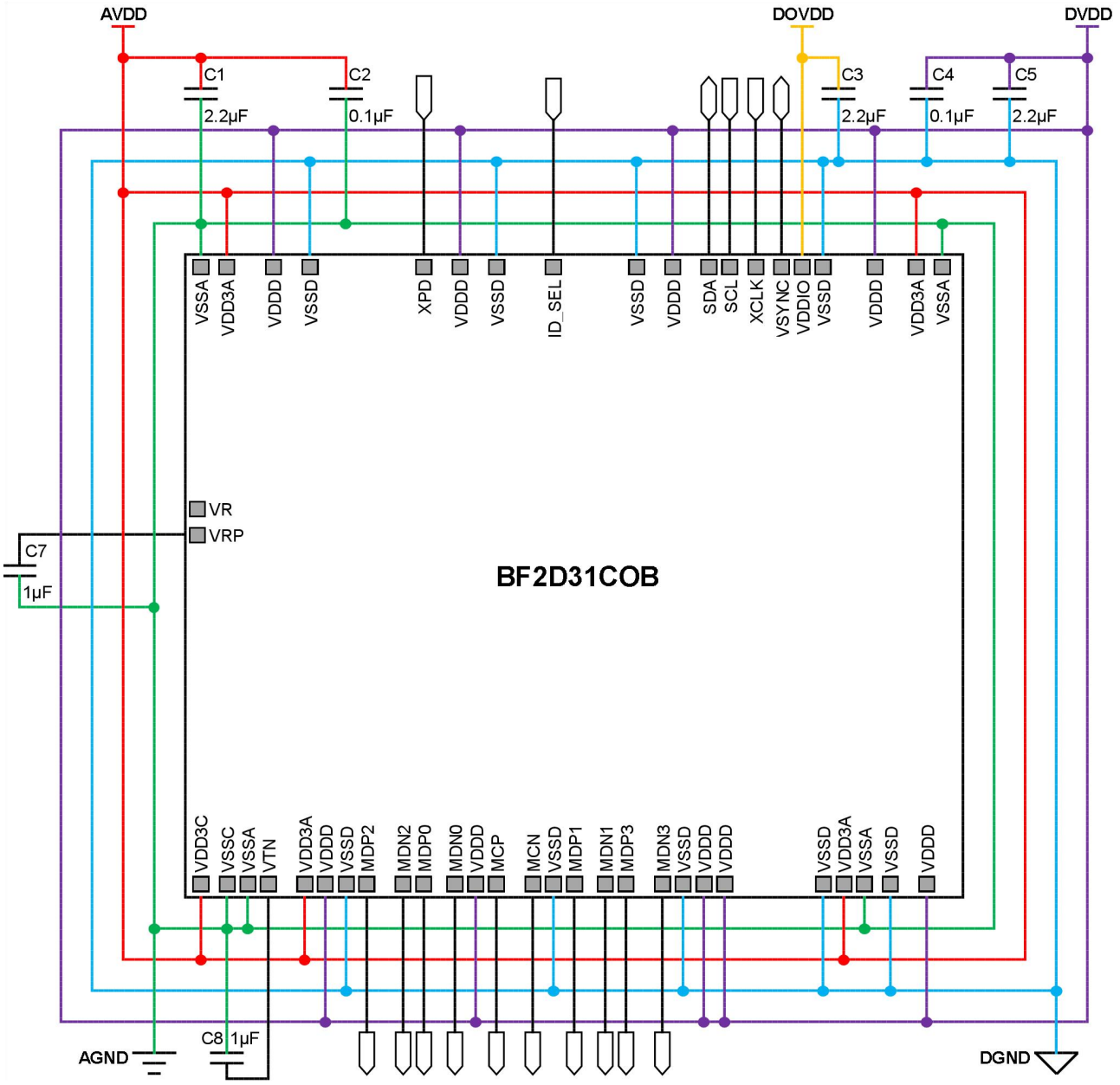


Figure 9 Reference design schematic

Notes:

1. Traces of MCP,MCN,MDPx and MDPx should have the same or similar length. Differential impedance of the clock pair and data pair transmission lines should be controlled at 100 ohm.
2. ID_SEL pin should be pulled low for device address 0x7c/0x7d and pulled high for device address 0xdc/0xdd.

11 Application Timing

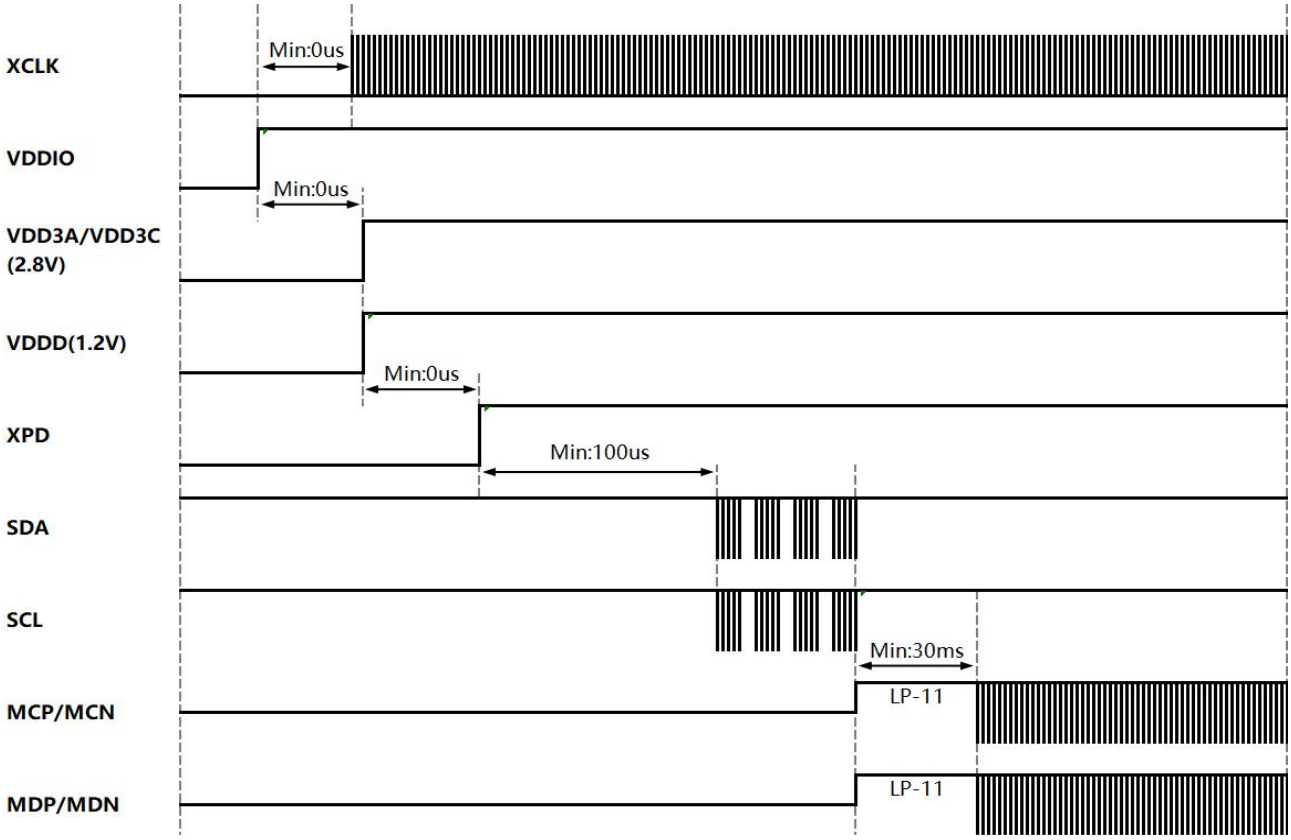


Figure 10 Power On Sequence

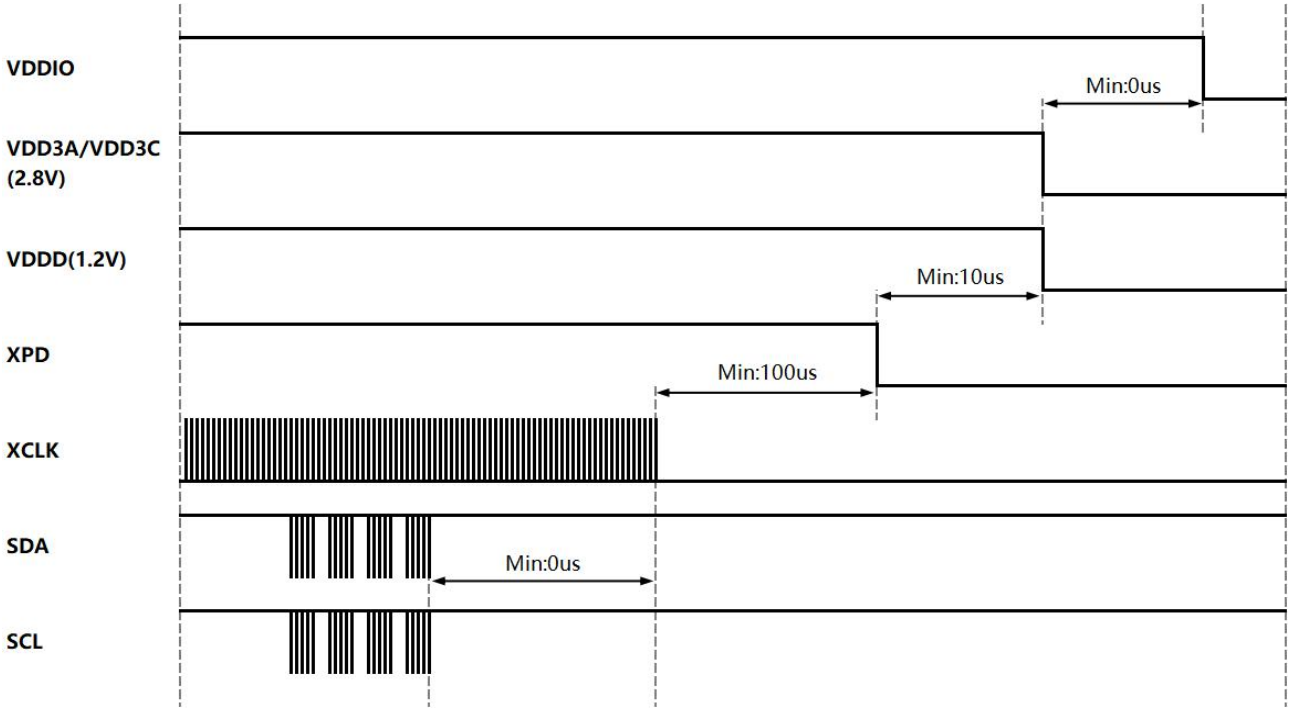


Figure 11 Power Off Sequence

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